

F100150 Hex D Latch

General Description

The F100150 contains six D-type latches with true and complement outputs, a pair of common Enables ($\bar{E}_a$ and $\bar{E}_b$), and a common Master Reset (MR). A Q output follows its D input when both $\bar{E}_a$ and $\bar{E}_b$ are LOW. When either $\bar{E}_a$ or $\bar{E}_b$ (or both) are HIGH, a latch stores the last valid data present on its D input before $\bar{E}_a$ or $\bar{E}_b$ went HIGH. The MR input

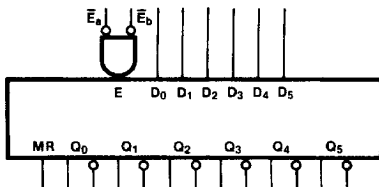
overrides all other inputs and makes the Q outputs LOW. All inputs have 50 k Ω pull-down resistors.

Refer to the F100350 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (–4.2V to –5.7V)

Ordering Code: See Section 8

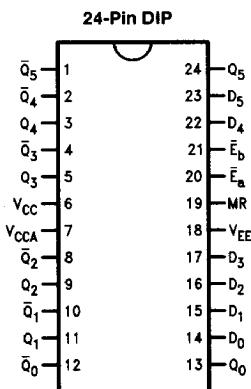
Logic Symbol



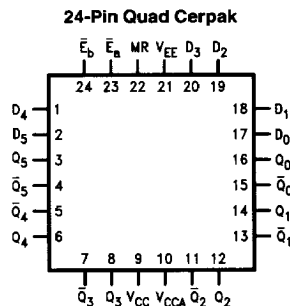
TL/F/9858–3

Pin Names	Description
D ₀ –D ₅	Data Inputs
$\bar{E}_a$, $\bar{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q ₀ –Q ₅	Data Outputs
$\bar{Q}_0$ – $\bar{Q}_5$	Complementary Data Outputs

Connection Diagrams

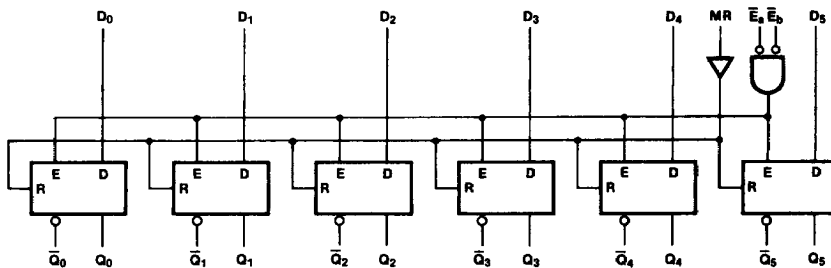


TL/F/9858–1



TL/F/9858–2

Logic Diagram



TL/F/9858-5

Truth Tables (Each Latch)

Latch Operation

Inputs				Outputs
D_n	$\bar{E}_a$	$\bar{E}_b$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched*
X	X	H	L	Latched*

*Retains data present before E positive transition

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Asynchronous Operation

Inputs				Outputs
D_n	$\bar{E}_a$	$\bar{E}_b$	MR	Q_n
X	X	X	H	L

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
 Input Voltage (DC) V_{EE} to $+0.5\text{V}$
 Output Current (DC Output HIGH) -50 mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1810	−1705	−1620			
V _{OHC}	Output HIGH Voltage	−1035			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1610			
V _{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)		
V _{OH}	Output HIGH Voltage	−1020		−870	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V	
V _{OL}	Output LOW Voltage	−1810		−1605				
V _{OHC}	Output HIGH Voltage	−1030			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V	
V _{OLC}	Output LOW Voltage			−1595				
V _{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs		
V _{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs		
I _{II}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)		

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1035		−880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1830		−1620			
V _{OHC}	Output HIGH Voltage	−1045			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1610			
V _{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I _{II}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical CharacteristicsV_{EE} = -4.2V to -4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

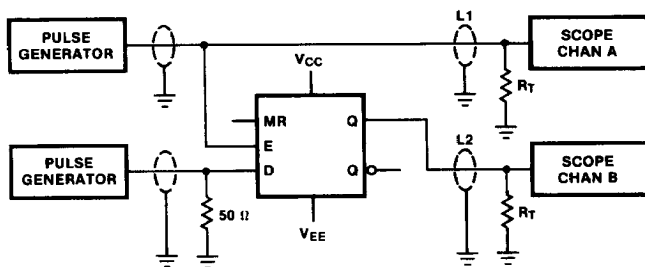
Symbol	Parameter	Min	Typ	Max	Units	Conditions
I _{IH}	Input HIGH Current MR D _n E _a , E _b			450 340 520	μA	V _{IN} = V _{IH} (Max)
I _{EE}	Power Supply Current	-159	-113	-79	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical CharacteristicsV_{EE} = -4.2V to -4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T _C = 0°C		T _C = +25°C		T _C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay D _n to Output (Transparent Mode)	0.45	1.50	0.50	1.40	0.50	1.50	ns	Figures 1 and 2
t _{PLH} t _{PHL}	Propagation Delay E _a , E _b to Output	0.75	2.05	0.75	1.85	0.75	2.05	ns	
t _{PLH} t _{PHL}	Propagation Delay MR to Output	0.80	2.40	0.90	2.40	0.90	2.60	ns	Figures 1 and 3
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.60	ns	Figures 1 and 2
t _s	Setup Time D ₀ -D ₅ MR (Release Time)	0.70 2.10		0.70 2.10		0.70 2.10		ns	Figures 3 and 4
t _h	Hold Time, D ₀ -D ₅	0.70		0.70		0.70		ns	Figure 4
t _{pw(L)}	Pulse Width LOW E _a , E _b	2.00		2.00		2.00		ns	Figure 2
t _{pw(H)}	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	Figure 3

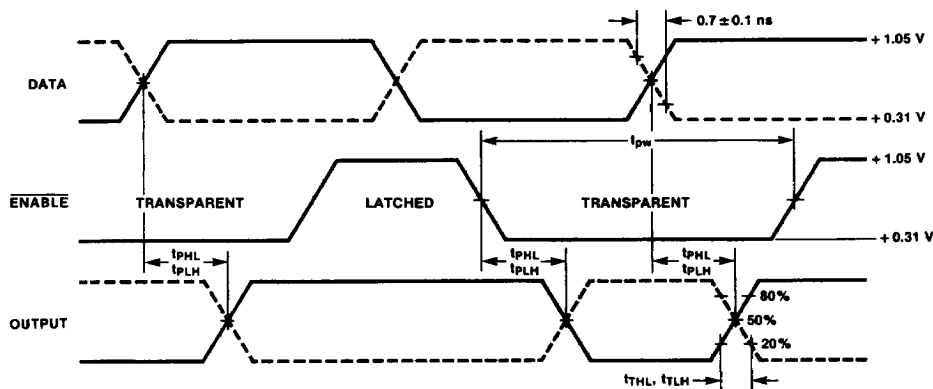
Cerpak AC Electrical CharacteristicsV_{EE} = -4.2V to -4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T _C = 0°C		T _C = +25°C		T _C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay D _n to Output (Transparent Mode)	0.45	1.30	0.50	1.20	0.50	1.30	ns	Figures 1 and 2
t _{PLH} t _{PHL}	Propagation Delay E _a , E _b to Output	0.75	1.85	0.75	1.65	0.75	1.85	ns	
t _{PLH} t _{PHL}	Propagation Delay MR to Output	0.80	2.20	0.90	2.20	0.90	2.40	ns	Figures 1 and 3
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.50	ns	Figures 1 and 2
t _s	Setup Time D ₀ -D ₅ MR (Release Time)	0.60 2.00		0.60 2.00		0.60 2.00		ns	Figures 3 and 4
t _h	Hold Time, D ₀ -D ₅	0.60		0.60		0.60		ns	Figure 4
t _{pw(L)}	Pulse Width LOW E _a , E _b	2.00		2.00		2.00		ns	Figure 2
t _{pw(H)}	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	Figure 3

**Notes:**

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/9858-6

FIGURE 1. AC Test Circuit

TL/F/9858-7

FIGURE 2. Enable Timing

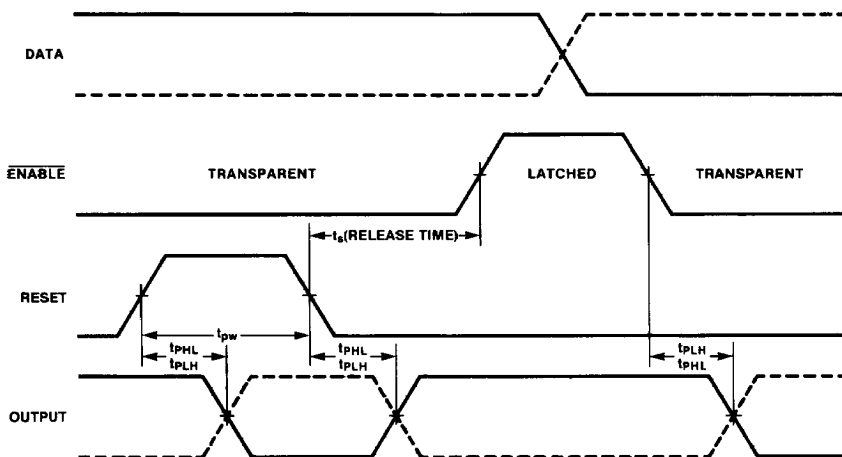
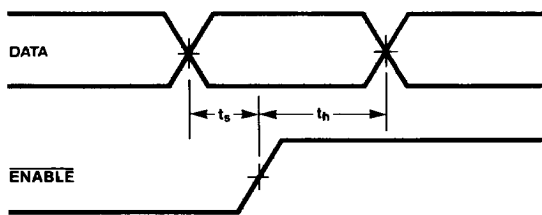


FIGURE 3. Reset Timing

TL/F/9858-8



TL/F/9858-9

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.
 t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

FIGURE 4. Data Setup and Hold Time