



F100160 Dual Parity Checker/Generator

General Description

The F100160 is a dual parity checker/generator. Each half has nine inputs; the output is HIGH when an even number of inputs are HIGH. One of the nine inputs (I_a or I_b) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits.

The F100160 also has a Compare ($\bar{C}$) output which allows the circuit to compare two 8-bit words. The $\bar{C}$ output is LOW when the two words match, bit for bit. All inputs have 50 k Ω pulldown resistors.

Refer to the F100360 datasheet for:

PCC packaging

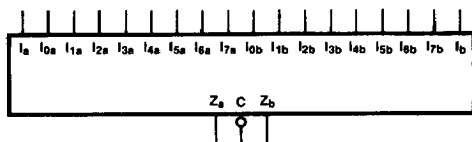
Lower power

Military versions

Extended voltage specs ($-4.2V$ to $-5.7V$)

Ordering Code: See Section 8

Logic Symbol

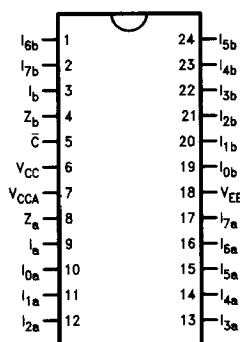


TL/F/9863-3

Pin Names	Description
I_a, I_b, I_{0a}, I_{0b}	Data Inputs
Z_a, Z_b	Parity Odd Outputs
$\bar{C}$	Compare Output

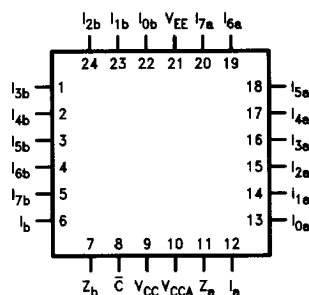
Connection Diagrams

24-Pin DIP



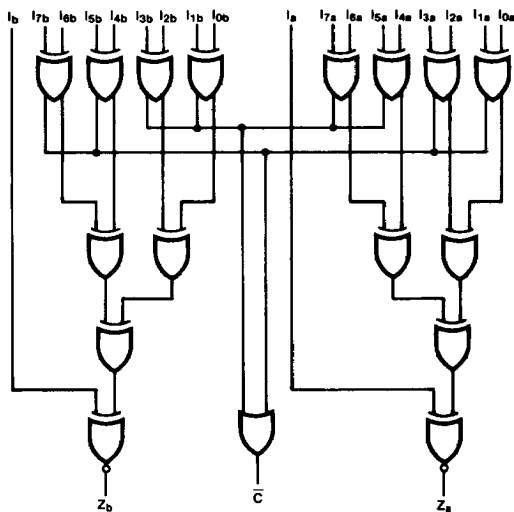
TL/F/9863-1

24-Pin Quad Cerpak



TL/F/9863-2

Logic Diagram



TL/F/9863-5

Truth Table (Each Half)

Sum of HIGH Inputs	Output Z
Even	HIGH
Odd	LOW

Comparator Function

$$\begin{aligned} \bar{C} = & (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + \\ & (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + \\ & (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b}) \end{aligned}$$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
 Input Voltage (DC) V_{EE} to $+0.5\text{V}$
 Output Current (DC Output HIGH) -50mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1810	−1705	−1620			
V _{OHC}	Output HIGH Voltage	−1035			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1610			
V _{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	− 1020		− 870	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to − 2.0V
V _{OL}	Output LOW Voltage	− 1810		− 1605			
V _{OHC}	Output HIGH Voltage	− 1030			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to − 2.0V
V _{OLC}	Output LOW Voltage			− 1595			
V _{IH}	Input HIGH Voltage	− 1150		− 870	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	− 1810		− 1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	− 1035		− 880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to − 2.0V
V _{OL}	Output LOW Voltage	− 1830		− 1620			
V _{OHC}	Output HIGH Voltage	− 1045			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to − 2.0V
V _{OLC}	Output LOW Voltage			− 1610			
V _{IH}	Input HIGH Voltage	− 1165		− 880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	− 1830		− 1490	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current I_{a, I_b} I_{na, I_nb}			340 240	μA	$V_{IN} = V_{IH} (Max)$
I_{EE}	Power Supply Current	-115	-82	-57	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na, I_nb} to Z_a, Z_b	1.30	4.30	1.30	4.10	1.30	4.30	ns	<i>Figures 1 & 2</i>
t_{PLH} t_{PHL}	Propagation Delay I_{na, I_nb} to $\bar{C}$	1.20	3.30	1.20	3.10	1.20	3.30	ns	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.60	0.50	1.50	0.50	1.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na, I_nb} to Z_a, Z_b	1.30	4.10	1.30	3.90	1.30	4.10	ns	<i>Figures 1 & 2</i>
t_{PLH} t_{PHL}	Propagation Delay I_{na, I_nb} to $\bar{C}$	1.20	3.10	1.20	2.90	1.20	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.40	0.50	1.30	0.50	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	

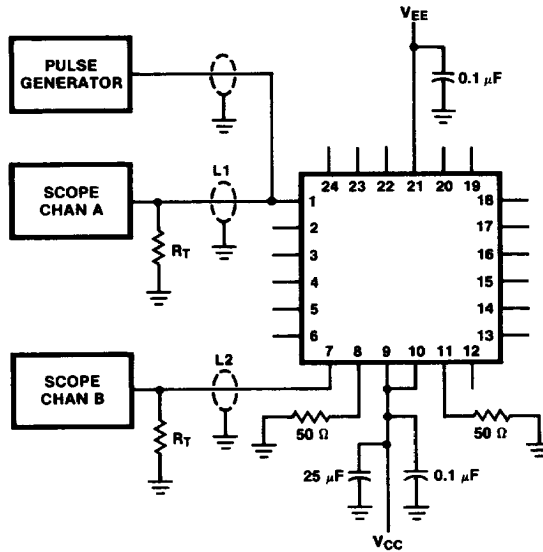


FIGURE 1. AC Test Circuit

TL/F/9863-6

Notes: $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$ $L1$ and $L2$ = equal length 50Ω impedance lines $R_T = 50\Omega$ terminator internal to scopeDecoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE} All unused outputs are loaded with 50Ω to GND C_L = Fixture and stray capacitance $\leq 3 pF$

Pin numbers shown are for flatpak; for DIP see logic symbol

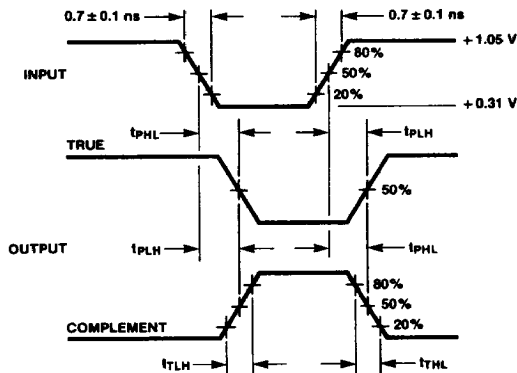


FIGURE 2. Propagation Delay and Transition Times

TL/F/9863-7