National Semiconductor

Not Intended For New Designs

T-52-30-07

100250
Quint Full Duplex Line Transceiver

General Description

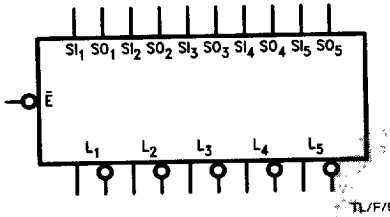
The 100250 is a quint line transceiver capable of simultaneously transmitting and receiving differential mode signals on a twisted pair line. Each transceiver has a signal input S_{IN}, a signal output S_{OUT} and two differential line inputs/outputs L and $\overline{L}$. Signals received from the lines L and $\overline{L}$ can be stored in an internal latch. The line outputs are designed to drive twisted pair lines. The $\overline{ENABLE}$ input is common to all five transceivers.

Features

- Full duplex operation
- Common mode noise immunity of ±1V

Ordering Code: See Section 6

Logic Symbol



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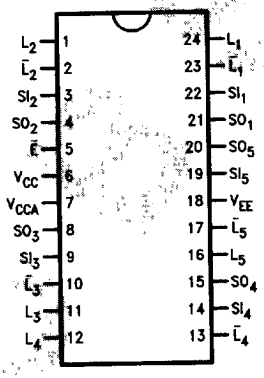
Pin Names	Description
$\overline{E}$	Common Enable
S_{In}	100K Signal Inputs
S_{On}	100K Signal Outputs
L_n, $\overline{L}_n$	Differential Line Inputs/Outputs

Connection Diagrams

24-Pin DIP



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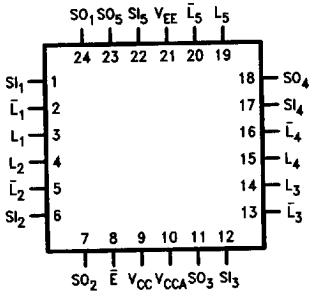
24-Pin Quad Cerpak



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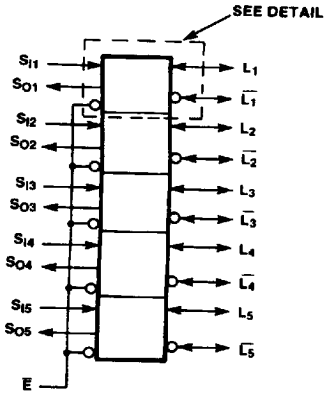
Logic Diagram



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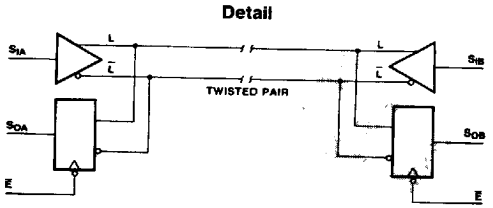

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FIGURE 1. Interconnection of Two 100250 Circuits, Duplex Mode Operation

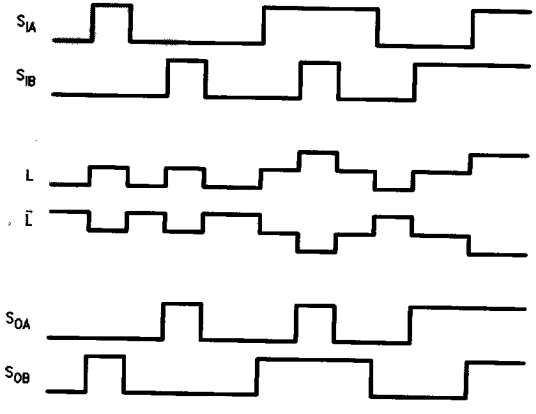
Truth Table

$\overline{E}$	S_{IA}	S_{IB}	S_{OA}	S_{OB}	L	$\overline{L}$
H	X	X	$S_{OA}(n-1)$	$S_{OB}(n-1)$	*	*
L	L	L	L	L	U_L	U_H
L	L	H	H	L	$(U_L + U_H)/2$	$(U_L + U_H)/2$
L	H	L	L	H	$(U_L + U_H)/2$	$(U_L + U_H)/2$
L	H	H	H	H	U_H	U_L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
n−1 = Previous State
* = Dependent on S_{IA} and S_{IB}

$U_L \approx -1.27V$
$U_H \approx -0.27V$
$(U_L + U_H)/2 \approx -0.77V$

Functional Waveform



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100250

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current S_{In}			200	μA	V_{IN} = $V_{IH(Max)}$
	$\overline{E}$			250	μA	
I_{EE}	Power Supply Current	−300		−180	mA	Inputs Open

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{KH}	Line Output HIGH Voltage	−370		−220	mV	No Load	
V_{KL}	Line Output LOW Voltage	−1400		−1090	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605	mV		
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OLC}	Output LOW Voltage			−1595	mV		
V_{KH}	Line Output HIGH Voltage	−350		−200	mV	No Load	
V_{KL}	Line Output LOW Voltage	−1300		−990	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

$V_{EE} = -4.8V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620	mV		
V_{OHC}	Output HIGH Voltage	−1045			mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{KH}	Line Output HIGH Voltage	−400		−250	mV	No Load	
V_{KL}	Line Output LOW Voltage	−1500		−1190	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL(Min)}$	

Note 1: Unless specified otherwise on individual data sheet

Note 2: Parametric values specified at −4.2V to −4.8V

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$

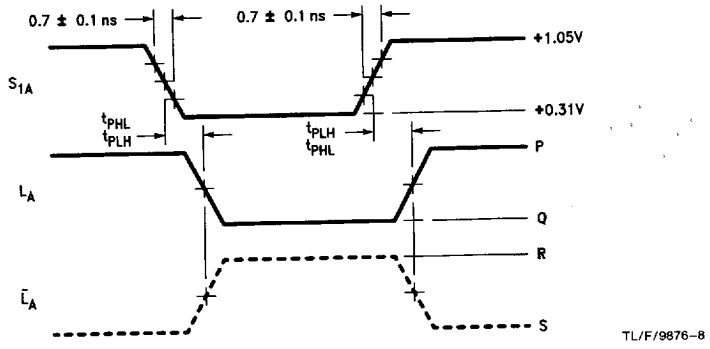
Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_I to L, $\overline{L}$	1.1	2.4	1.1	2.4	1.2	2.6	ns	*Figures 2* and *4*
t_{PLH} t_{PHL}	Propagation Delay L, $\overline{L}$ to S_O	1.2	2.8	1.2	2.9	1.3	3.0	ns	*Figures 3* and *5*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to S_O	1.2	2.6	1.2	2.7	1.3	2.9	ns	*Figures 3* and *5*
t_{THL} t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.5	2.0	0.5	2.0	0.5	2.0	ns	
t_S	Setup Time L, $\overline{L}$	1.3		1.3		1.5		ns	*Figure 3*
t_H	Hold Time L, $\overline{L}$	1.3		1.3		1.5		ns	

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$

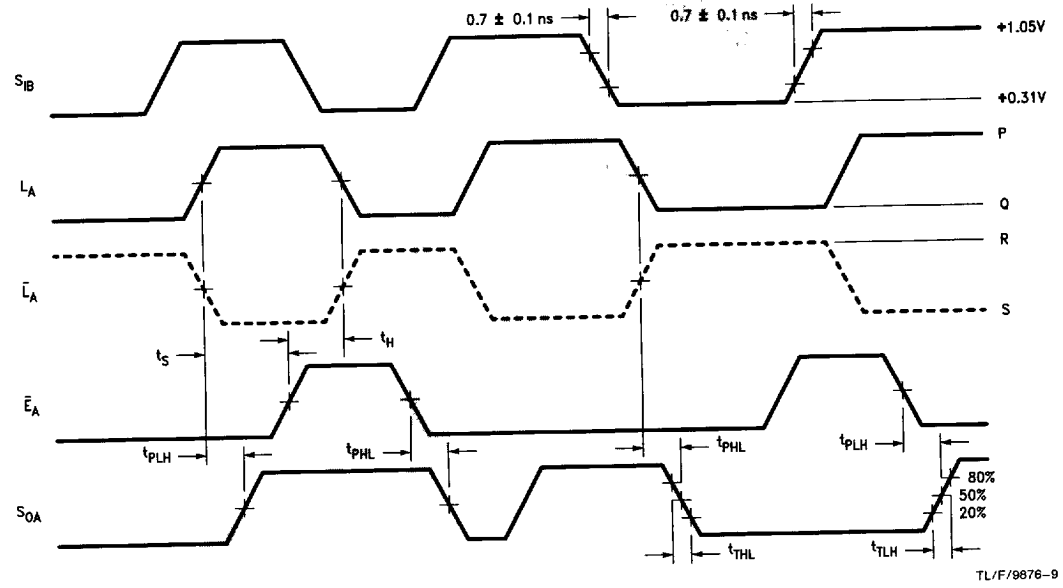
Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_I to L, $\overline{L}$	1.1	2.2	1.1	2.2	1.2	2.4	ns	*Figures 2* and *4*
t_{PLH} t_{PHL}	Propagation Delay L, $\overline{L}$ to S_O	1.2	2.6	1.2	2.7	1.3	2.8	ns	*Figures 3* and *5*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to S_O	1.2	2.4	1.2	2.5	1.3	2.7	ns	*Figures 3* and *5*
t_{THL} t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.5	1.9	0.5	1.9	0.5	1.9	ns	
t_S	Setup Time L, $\overline{L}$	1.3		1.3		1.5		ns	*Figure 3*
t_H	Hold Time L, $\overline{L}$	1.3		1.3		1.5		ns	

Switching Waveforms



Notes: S_{IB} = L then P = $(U_L + U_H)/2$, Q = U_L, R = U_H, S = $(U_L + U_H)/2$
S_{IB} = H then P = U_H, Q = $(U_L + U_H)/2$, R = $(U_L + U_H)/2$, S = U_L
} L, $\bar{L}$ loaded with another F100250

FIGURE 2. S_I to Differential Line



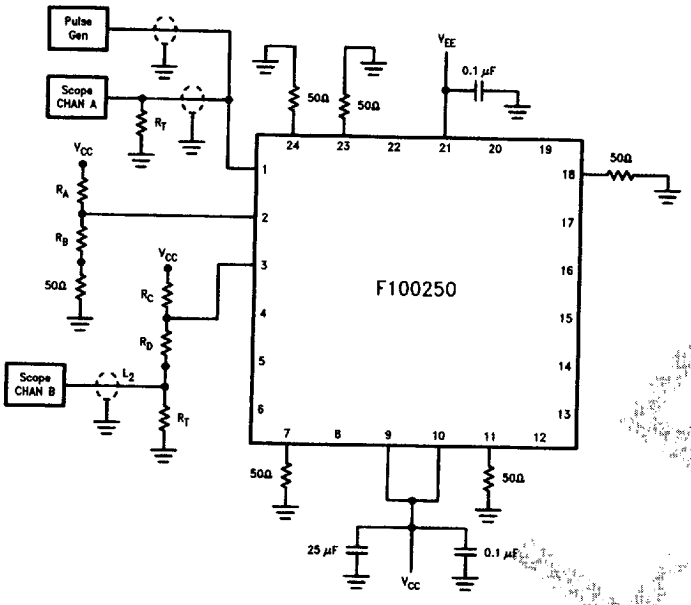
Notes: S_{IA} = L then P = $(U_L + U_H)/2$, Q = U_L, R = U_H, S = $(U_L + U_H)/2$
S_{IA} = H then P = U_H, Q = $(U_L + U_H)/2$, R = $(U_L + U_H)/2$, S = U_L
} L, $\bar{L}$ loaded with another F100250

t_S is the minimum time before the transition of the enable that information must be present at the data input

t_H is the minimum time before the transition of the enable that information must remain unchanged at the data input

FIGURE 3. Differential Line to S_O

Test Circuitry



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND
C_L = fixture and stray capacitance ≤ 3 pF.
L and L terminated by 100250 or Thevenin equivalent.
Signal levels will be a percentage of full swing if using equivalent network.
R_A = 91Ω, R_B = 500Ω, R_C = 220Ω, R_D = 71.5Ω for S_{IB} = L.
R_A = 220Ω, R_B = 71.5Ω, R_C = 91Ω, R_D = 500Ω for S_{IB} = H.

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FIGURE 4. AC Test Circuit SI to Differential Line

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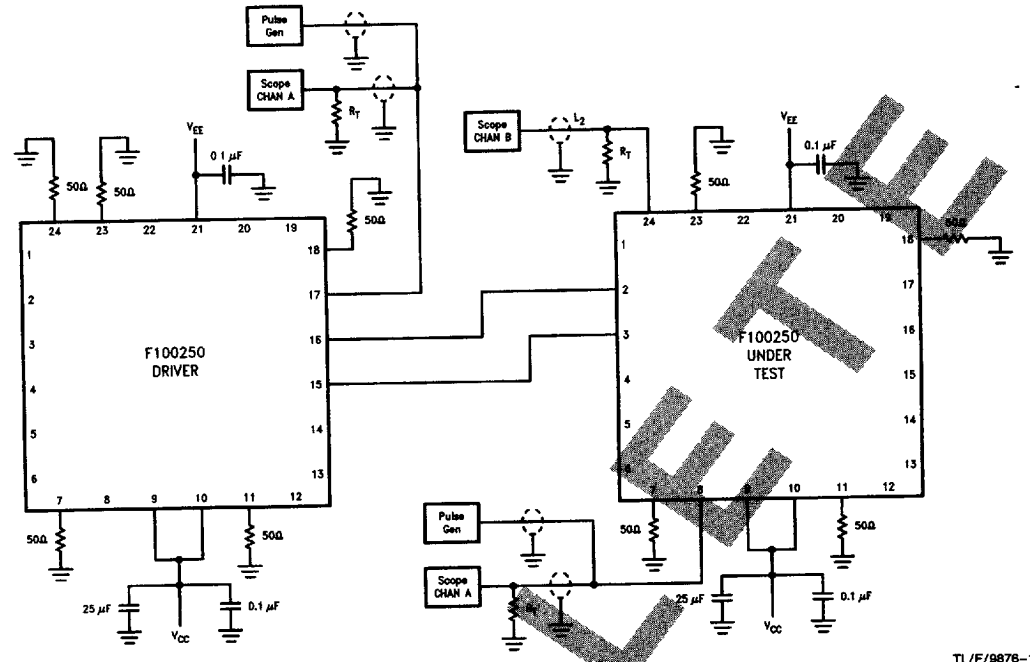

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND.
C_L = fixture and stray capacitance ≤ 3 pF.

FIGURE 5. AC Test Circuit Differential Line to S_O and $\overline{E}$ to S_O