T-46-07-11

National Semiconductor

100350
Low Power Hex D-Latch

General Description

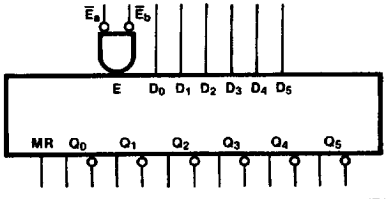
The 100350 contains six D-type latches with true and complement outputs, a pair of common Enables ($\overline{E}_a$ and $\overline{E}_b$), and a common Master Reset (MR). A Q output follows its D input when both $\overline{E}_a$ and $\overline{E}_b$ are LOW. When either $\overline{E}_a$ or $\overline{E}_b$ (or both) are HIGH, a latch stores the last valid data present on its D input before $\overline{E}_a$ or $\overline{E}_b$ went HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Features

- 20% power reduction of the 100150
- 2000V ESD protection
- Pin/function compatible with 100150
- Voltage compensated operating range = −4.2V to −5.7V

Ordering Code: See Section 6

Logic Symbol

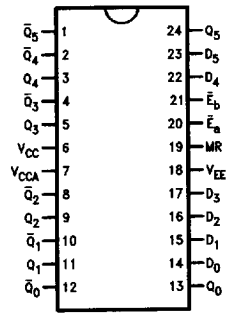


TL/F/9884–10

Pin Names	Description
D_0–D_5	Data Inputs
$\overline{E}_a$, $\overline{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

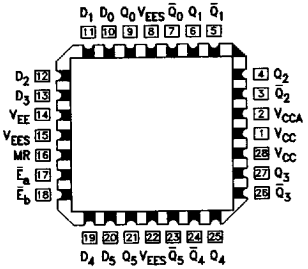
Connection Diagrams

24-Pin DIP



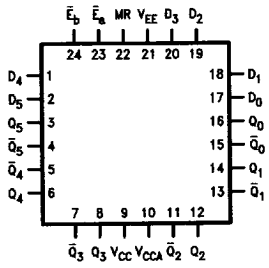
TL/F/9884–1

28-Pin PCC



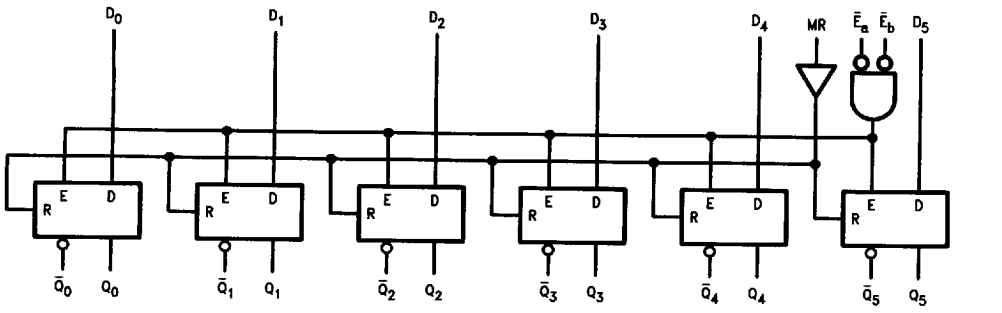
TL/F/9884–3

24-Pin Quad Cerpak



TL/F/9884–2

Logic Diagram



TL/F/9884–4

Truth Tables (Each Latch)

Latch Operation

Inputs				Outputs
D_n	$\bar{E}_a$	$\bar{E}_b$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched*
X	X	H	L	Latched*

*Retains data present before $\bar{E}$ positive transition

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Asynchronous Operation

Inputs				Outputs
D_n	$\bar{E}_a$	$\bar{E}_b$	MR	Q_n
X	X	X	H	L

2

100350

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.5V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current MR D_n $\overline{E}_a$, $\overline{E}_b$			 240 240 240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current	−89 −93		−44 −44	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

DIP AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.40	0.50	1.40	0.50	1.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	1.85	0.75	1.85	0.75	2.05	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.90	2.10	0.90	2.10	0.90	2.10	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.30	0.35	1.30	0.35	1.30	ns	*Figures 1* and *2*
t_s	Setup Time D_0–D_5 MR (Release Time)	1.00 1.60		1.00 1.60		1.00 1.60		ns	*Figures 3* and *4*
t_h	Hold Time, D_0–D_5	0.40		0.40		0.40		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*

PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.20	0.50	1.20	0.50	1.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	1.65	0.75	1.65	0.75	1.85	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.90	1.90	0.90	1.90	0.90	1.90	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	*Figures 1* and *2*
t_s	Setup Time D_0–D_5 MR (Release Time)	0.90 1.50		0.90 1.50		0.90 1.50		ns	*Figures 3* and *4*
t_h	Hold Time, D_0–D_5	0.30		0.30		0.30		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*

100350

Military Version—Preliminary

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH}(Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH}(Min) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		1, 2, 3
I_{IH}	Input HIGH Current MR D_n $\overline{E}_a$, $\overline{E}_b$		300 250 520	μA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		1, 2, 3
	MR D_n $\overline{E}_a$, $\overline{E}_b$		450 350 750	μA	−55°C			
I_{EE}	Power Supply Current	−138	−64	mA	−55°C to +125°C	Inputs Open		1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version-Preliminary (Continued)

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.45	1.50	0.50	1.40	0.50	1.50	ns	*Figures 1* and *2*	1, 2, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	2.05	0.75	1.85	0.75	2.05	ns		
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.40	0.90	2.40	0.90	2.60	ns	*Figures 1* and *3*	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*	
t_S	Setup Time D_0-D_5 MR (Release Time)	 0.70 2.10		 0.70 2.10		 0.70 2.10		ns	*Figures 1* and *2*	
t_H	Hold Time, D_0-D_5	0.70		0.70		0.70		ns	*Figure 4*	4
t_{pw}(L)	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*	
t_{pw}(L)	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*	

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

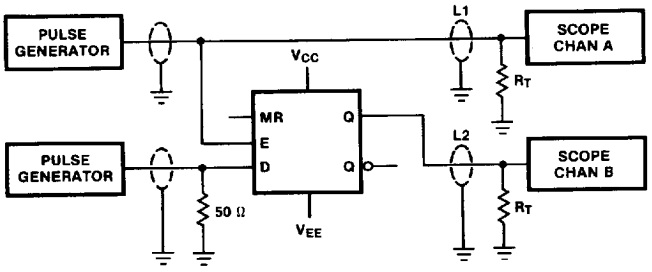
Note 2: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each Mfg. lot at +25°C, Subgroup A9, and at +125°C, and −55°C temp., Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

100350

Test Circuit



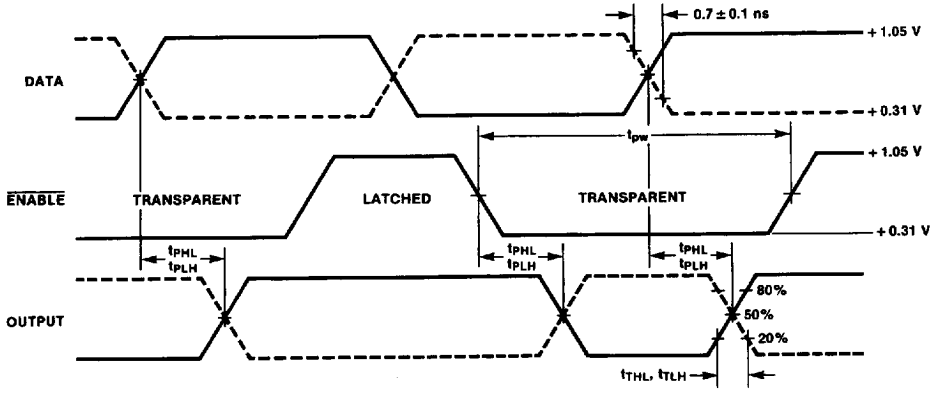
Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/9884–5

FIGURE 1. AC Test Circuit

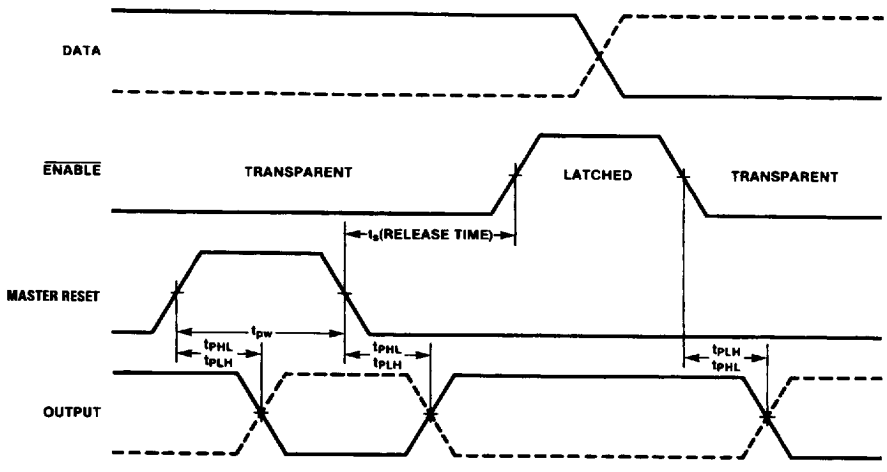
Switching Waveforms



TL/F/9884–6

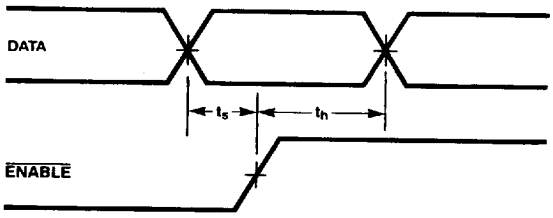
FIGURE 2. Enable Timing

Switching Waveforms (Continued)



TL/F/9884–7

FIGURE 3. Reset Timing



TL/F/9884–8

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

FIGURE 4. Data Setup and Hold Time