Quad 2-Input NOR Gate with Strobe

ELECTRICALLY TESTED PER:
MPG 10500

The 10500 is a quad 2 input **NOR** gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

- 40 mW Max/Gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	OPEN
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	OPEN
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Common Input	9	13	12	OPEN
C_{IN}	10	14	13	OPEN
C_{IN}	11	15	14	OPEN
D_{IN}	12	16	15	OPEN
D_{IN}	13	1	17	OPEN
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

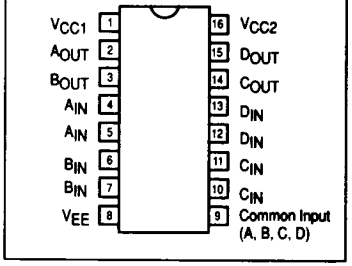
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

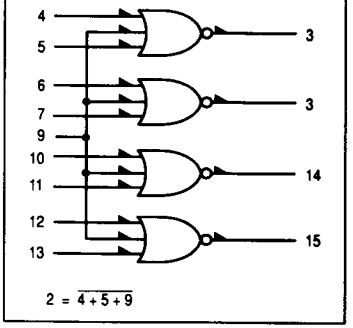
1) JAN: N/A
2) SMD: N/A
3) 883: 10500/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

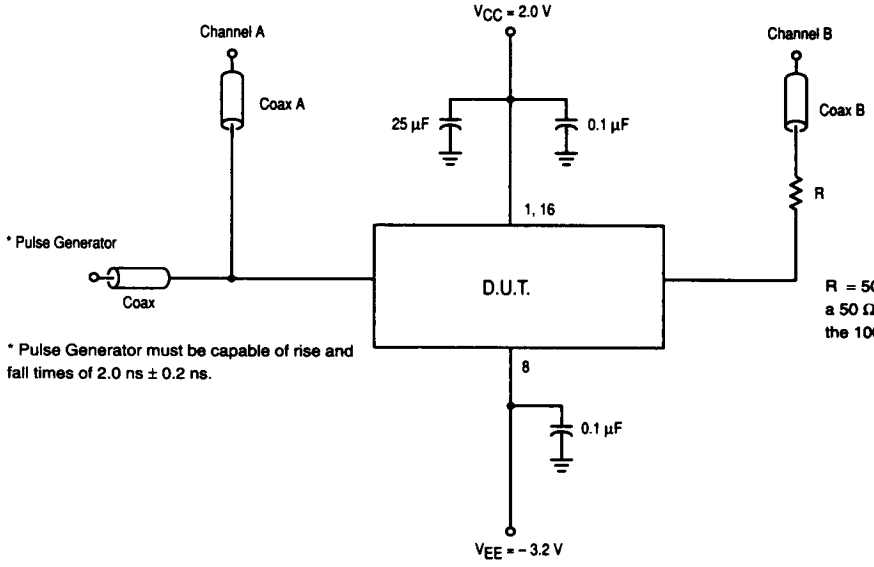
The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



$2 = \overline{4+5+9}$



NOTES
1. Length of $Coax_A$ and $Coax_B$ should be of equal length for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.

NOTES
1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

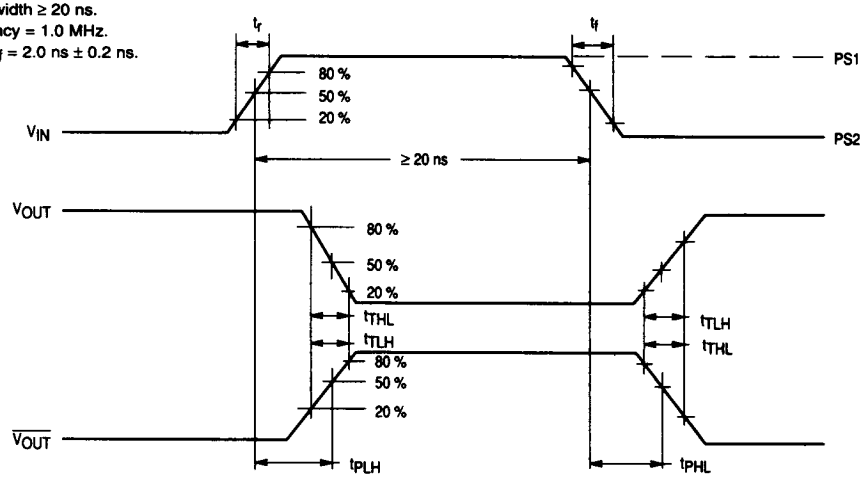


Figure 1. Switching Test Circuit and Waveforms

10500
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{EEL}	V_{EE}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	+2.0	-2.94	-5.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.345	+2.0	-2.94	-5.2
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.03	+0.285	+2.0	-2.94	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	GND	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V		4, 5, 10, 11				8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.565	– 1.92	– 1.655	V	4 - 7, 9 - 13					8	1, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V				4 - 7, 9 - 13		8	1, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.565	– 1.92	– 1.635	V			4 - 7, 9 - 13			8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Drain Current	– 26	– 3.0	– 29	– 3.0	– 29	– 3.0	mA						8	1, 16	8
I_{IH}	Input Current High		245		415		415	µA	4 - 7, 9 - 13					8	1, 16	4 - 7, 10 - 13
I_{IH1}	Input Current High		470		800		800	µA	9					8	1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13				8	1, 16	4 - 7, 10 - 13

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	4, 6	2, 3	1, 16	8	2, 3, 14, 15
t_{TLH}	Fall Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	4, 6	2, 3	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	ns	10, 13	14, 15	1, 16	8	2, 3, 14
t_{PHL}	Propagation Delay High to Low	1.0	2.9	1.0	3.7	1.0	3.7	ns	10, 13	14, 15	1, 16	8	2, 3, 14