



Error Detection-Correction Circuit

ELECTRICALLY TESTED PER:

MPG 10563

The 10563 is an error detection and correction circuit. It is a building block designed for use with memory systems. The 10563 offers economy in the design of the error detection/correction subsystems for mainframe and add-on memory systems.

For example, using eight 10563s together with eight 12-bit parity checkers (10560), single bit error detection/correction and double-bit error detection can be done on a word of 64-bit length. Only eight check bits (B₀-B₇) need be added to the word.

- 720 mW Max/Pkg (No Load)
- t_{pd} = 5.0 ns typ

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PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V _{CC1}	1	5	2	GND
P0 _B	2	6	3	51 Ω to V _{TT}
P ₃	3	7	4	51 Ω to V _{TT}
B ₅	4	8	5	OPEN
B ₆	5	9	7	OPEN
B ₂	6	10	8	GND
B ₁	7	11	9	GND
V _{EE}	8	12	10	V _{EE}
B ₀	9	13	12	OPEN
B ₃	10	14	13	GND
B ₇	11	15	14	GND
B ₄	12	16	15	OPEN
P ₂	13	1	17	51 Ω to V _{TT}
P ₁	14	2	18	51 Ω to V _{TT}
P0 _A	15	3	19	51 Ω to V _{TT}
V _{CC2}	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = - 2.0 V MAX/- 2.2 V MIN

V_{EE} = - 5.7 V MAX/- 5.2 V MIN

Military 10563

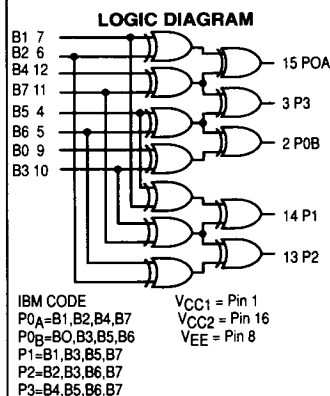
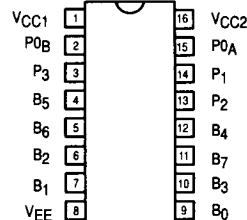


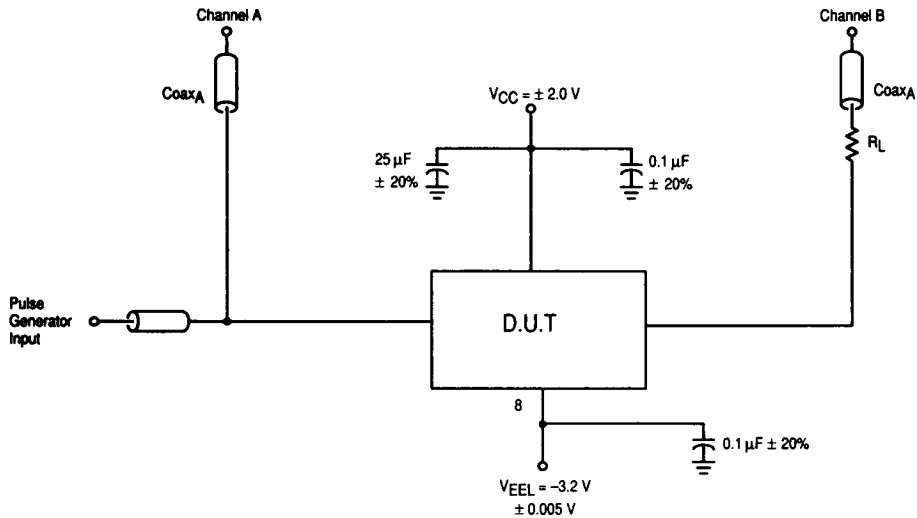
AVAILABLE AS

- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: 10563/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



**NOTES**

1. Pulse generator must be capable of rise and fall times of $2.0 \text{ ns} \pm 0.2 \text{ ns}$.
2. Length of Coax_A and Coax_B should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0 \text{ ns} \pm 0.2 \text{ ns}$ (20% to 80%)
5. $R_L = 50 \Omega$ resistor in series with 50Ω coax constituting the 100Ω load.
6. V_{IN} has the following characteristics:
 - a) pulse width $\geq 20 \text{ ns}$.
 - b) frequency = 1.0 MHz .
7. Unused outputs should be loaded 100Ω to ground.

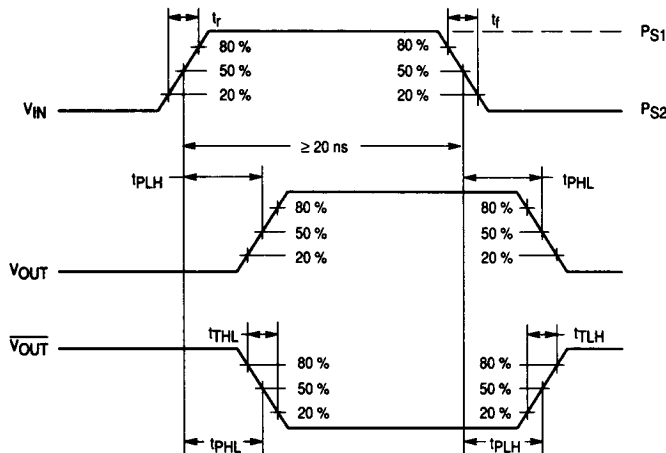


Figure 1. Switching Test Circuit and Waveforms

10563 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)						
	V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	PS ₁	PS ₂	VEEL
T _A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2
T _A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2
T _A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to – 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max											
VOH	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	V _{EE}	V _{CC}	P. U. T.			
VOL	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V					8	1, 16	2, 3, 13 - 15			
VOL1	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.525	– 1.92	– 1.635	V				4 - 7, 9 - 12	8	1, 16	2, 3, 13 - 15			
VOH1	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V			4 - 7, 9 - 12		8	1, 16	2, 3, 13 - 15			
I _{IH}	Input Current High		220		375		375	μA	4, 6, 10				8	1, 16	4, 6, 10			
I _{IH1}	Input Current High		265		450		450	μA	5, 7, 9, 11, 12				8	16	5, 7, 9, 11 12			
I _{IL}	Input Current Low	0.5		0.3		0.5		μA					8	16	2, 7, 9, 14 15			
I _{EE}	Power Supply Drain Current	– 125		– 138		– 138		mA						8	1, 16	8		

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		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		V _{IN}	V _{OUT}	V _{CC}	VEEL	PS1	P. U. T.		
t _{TLH}	Rise Time	1.1	3.9	1.1	4.5	1.1	4.4	ns	4 - 7, 9 - 12	2, 3 13 - 15	1, 16	8	7, 9, 14	2, 3, 13 - 15		
t _{THL}	Fall Time	1.1	3.9	1.1	4.5	1.1	4.4	ns	4 - 7, 9 - 12	2, 3 13 - 15	1, 16	8	7, 9, 14	2, 3, 13 - 15		
t _{PLH}	Propagation Delay	1.5	6.5	1.5	7.5	1.3	7.0	ns	4 - 7, 9 - 12	2, 3 13 - 15	1, 16	8	7, 9, 14	2, 3, 13 - 16		
t _{PHL}	Propagation Delay	1.5	6.5	1.5	7.5	1.3	7.0	ns	4 - 7, 9 - 12	2, 3 13 - 15	1, 16	8	7, 9, 14	2, 3, 13 - 15		