



4-Bit Arithmetic Logic Unit/Function Generator

**ELECTRICALLY TESTED PER:
MPG 10581**

The 10581 is a high speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two 4-bit words. Full internal carry is incorporated for ripple-through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (PG) and carry generate (GG) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the 10579, full-carry look-ahead, as a second order look ahead block, the 10581 provides high speed arithmetic operations on very long words.

- 600 mW typ/pkg (No load)
- t_{pd} (typ): A1 to F = 6.5 ns
 C_n to $C_{n+4} = 3.1$ ns
A1 to PG = 5.0 ns
A1 to GG = 4.5 ns
A1 to $C_{n+4} = 5.0$ ns

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
VCC1	1	7	2	GND
F0	2	8	3	51 Ω to VTT
F1	3	9	4	51 Ω to VTT
GG	4	10	5	51 Ω to VTT
$C_n + 4$	5	11	6	51 Ω to VTT
F3	6	12	7	51 Ω to VTT
F2	7	13	9	51 Ω to VTT
PG	8	14	10	51 Ω to VTT
B3	9	15	11	50 Ω to VEE
A3	10	16	12	GND
B2	11	17	13	50 Ω to VEE
VEE	12	18	14	VEE
S3	13	19	16	50 Ω to VEE
S0	14	20	17	GND
S2	15	21	18	50 Ω to VEE
A2	16	22	19	GND
S1	17	23	20	GND
A1	18	24	21	50 Ω to VEE
B1	19	1	23	VEE
B0	20	2	24	50 Ω to VEE
A0	21	3	25	GND
C_n	22	4	26	50 Ω to VEE
M	23	5	27	GND
VCC2	24	6	28	GND

BURN - IN CONDITIONS:

VTT = - 2.0 V MAX/ - 2.2 V MIN
VEE = - 5.7 V MAX/ - 5.2 V MIN

Military 10581

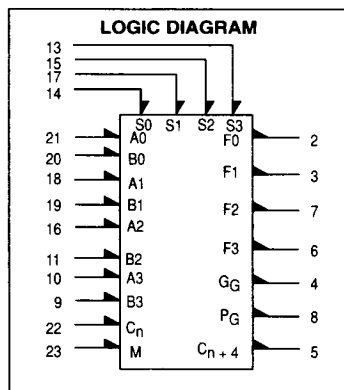
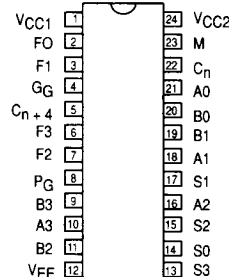


AVAILABLE AS

- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883C: 10581/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: K
CERFLAT: J
LCC: 3

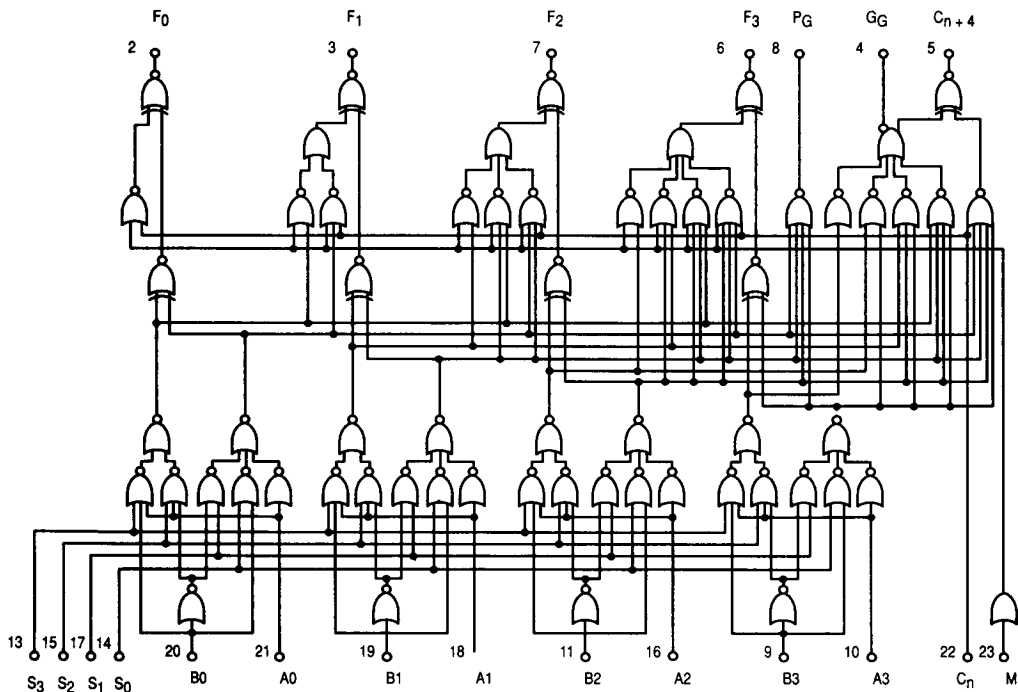
The letter "M" appears before the slash on LCC.



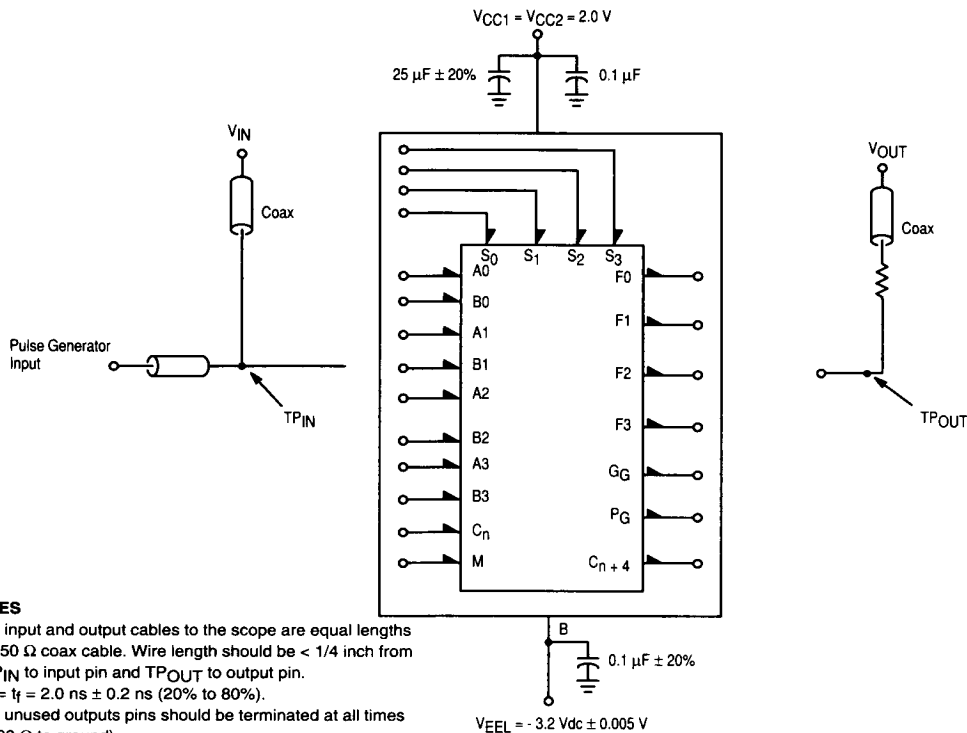
Arithmetic/Logic Functions

Function Select				Logic Function M is High C = D. C.	Arithmetic Operation M is Low C _n is low
S ₃	S ₂	S ₁	S ₀	F	F
L	L	L	L	$F = \bar{A}$	$F = A$
L	L	L	H	$F = \bar{A} + \bar{B}$	$F = A \text{ plus } (A \cdot \bar{B})$
L	L	H	L	$F = \bar{A} + B$	$F = A \text{ plus } (A \cdot B)$
L	L	H	H	$F = \text{Logical "1"}$	$F = A \text{ times } 2$
L	H	L	L	$F = \bar{A} \cdot B$	$F = (A + B) \text{ plus } 0$
L	H	L	H	$F = \bar{B}$	$F = (A + B) \text{ plus } (A \cdot \bar{B})$
L	H	H	L	$F = A \otimes B$	$F = A \text{ plus } B$
L	H	H	H	$F = A + \bar{B}$	$F = A \text{ plus } (A + B)$
H	L	L	L	$F = \bar{A} \cdot B$	$F = (A + \bar{B}) \text{ plus } 0$
H	L	L	H	$F = A \oplus B$	$F = A \text{ minus } B \text{ minus } 1$
H	L	H	L	$F = B$	$F = (A + \bar{B}) \text{ plus } (A \cdot \bar{B})$
H	L	H	H	$F = A + B$	$F = A \text{ plus } (A + \bar{B})$
H	H	L	L	$F = \text{Logical "0"}$	$F = \text{minus } 1 \text{ (two's complement)}$
H	H	L	H	$F = A \cdot \bar{B}$	$F = (A \cdot \bar{B}) \text{ minus } 1$
H	H	H	L	$F = A \cdot B$	$F = (A \cdot B) \text{ minus } 1$
H	H	H	H	$F = A$	$F = \text{minus } 1$

Logic Diagram



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NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coax cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. $t_r = t_f = 2.0 \text{ ns} \pm 0.2 \text{ ns}$ (20% to 80%).
3. All unused outputs pins should be terminated at all times (100 Ω to ground).
4. V_{IN} waveform has the following characteristics:
 - a) Pulse width $\geq 20 \text{ ns}$.
 - b) frequency = 1.0 MHz.

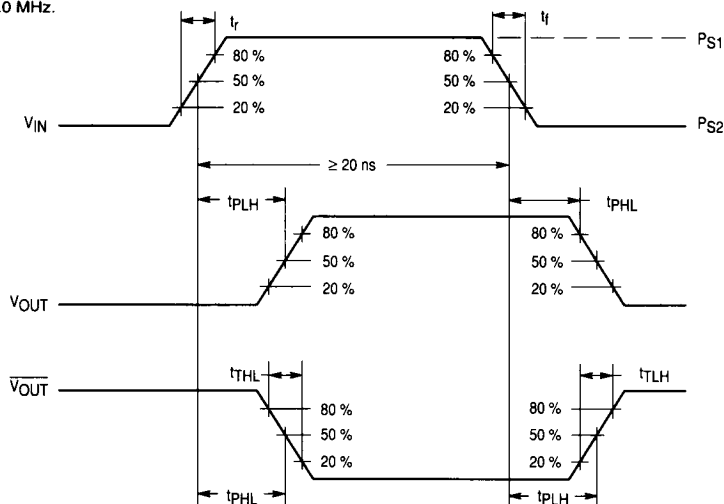


Figure 1. Switching Test Circuit and Waveforms

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QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V _{IH}	V _{IL}	V _{IHA}	V _{ILA}	PS ₁	PS ₂	V _{EE}	V _{EEL}
T _A = 25 °C	-0.78	-1.850	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T _A = 125 °C	-0.63	-1.820	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T _A = -55 °C	-0.88	-1.920	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to − 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V _{IH}	V _{IL}	V _{IHA}	V _{ILA}	V _{EE}	V _{CC}	P. U. T.	
V _{OH}	High Output Voltage	− 0.93	− 0.78	− 0.825	− 0.63	− 1.08	− 0.88	V	9 - 11 16 - 23	13 - 15			12	1, 24	2 - 8	
V _{OL1}	Low Output Voltage	− 1.85	− 1.620	− 1.82	− 1.545	− 1.92	− 1.655	V	9 - 11, 14, 16 18, 19, 21 - 23	9, 10, 13, 15 16, 17, 19, 21			12	1, 24	2, 3, 5 - 8	
V _{OLA}	Low Output Voltage	− 1.98	− 1.60	− 1.88	− 1.525	− 2.10	− 1.635	V		9 - 11, 13 - 23	14, 15	9 - 11 16 - 23	12	1, 24	2 - 8	
V _{OHA}	High Output Voltage	− 0.95	− 0.78	− 0.845	− 0.63	− 1.10	− 0.88	V	9 - 11, 13 16 - 23	13 - 23	16 - 23	13 - 15 22, 23	12	1, 24	2 - 8	
V _{OL2}	Low Output Voltage	− 1.99	− 1.620	− 1.88	− 1.545	− 2.10	− 1.655	V	11, 14, 16, 18 20, 22, 23	9, 10, 13, 15 17, 19, 21			12	1, 24	4	
I _{IH1}	Input Current High		200		340		340	μA	13, 23				12	1, 24	13, 23	
I _{IH2}	Input Current High		220		375		375	μA	10, 16, 18 21				12	1, 24	10, 16, 18 21	
I _{IH3}	Input Current High		245		415		415	μA	9, 11 19, 20				12	1, 24	9, 11, 19, 20	
I _{IH4}	Input Current High		265		450		450	μA	14, 15, 17				12	1, 24	14, 15, 17	
I _{IH5}	Input Current High		290		495		495	μA	22				12	1, 24	22	
I _{IL}	Input Current Low	0.5		0.3		0.5		μA		9 - 11 13 - 23			12	1, 24	9 - 11, 13 - 23	
I _{EE}	Power Supply Current	− 145		− 160		− 160		mA	9 - 11, 16 18 - 21				12	1, 24	12	

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		Subgroup 9		Subgroup 10		Subgroup 11													
		Min	Max	Min	Max	Min	Max	Max		V _{IN}	V _{OUT}	V _{CC}	VEEL	PS1	P. U. T.				
t _{TLH} / t _{THL}	Functional Parameters:	1.0	3.0	0.8	3.1	0.9	3.1	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7					
t _{pd}		1.1	5.0	0.9	5.1	1.0	5.1	ns	"	"	"	"	"	"					
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	5.0	1.0	5.3	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7					
t _{pd}	Propagation Delay C _N to F	2.0	7.0	2.0	7.1	1.9	7.1	ns	"	"	"	"	"	"					
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7					
t _{pd}	Propagation Delay A to F	3.0	10	2.8	10.2	2.9	10.1	ns	"	"	"	"	"	"					
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	3.5	1.0	3.6	0.9	3.5	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7					
t _{pd}	Propagation Delay A to P _G	2.0	6.5	1.8	6.5	1.8	6.6	ns	"	"	"	"	"	"					
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7					
t _{pd}	Propagation Delay A to G _G	2.0	7.0	2.0	7.1	1.9	7.1	ns	"	"	"	"	"	"					
t _{TLH} / t _{THL}	Rise & Fall Time	1.0	3.0	0.9	3.1	0.9	3.0	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7					
t _{pd}	Propagation Delay A to C _N + 4	2.0	7.0	1.9	7.5	2.0	7.1	ns	"	"	"	"	"	"					

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		Subgroup 9	Max	Subgroup 10	Max	Subgroup 11	Max		V _{IN}	V _{OUT}	VCC	VEEL	PS1	P. U. T.	
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7	
t _{pd}	Propagation Delay B to F	3.0	11	2.7	11.2	2.9	11.1	ns	"	"	"	"	"	"	
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	3.5	0.9	3.5	1.0	3.5	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7	
t _{pd}	Propagation Delay B to P _G	2.0	7.5	1.6	7.6	1.8	7.6	ns	"	"	"	"	"	"	
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	5.0	1.0	5.0	1.0	5.0	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7	
t _{pd}	Propagation Delay B to G _G	2.0	8.0	2.0	8.1	1.9	8.1	ns	"	"	"	"	"	"	
t _{TLH} / t _{THL}	Rise & Fall Time	1.0	3.0	0.9	3.0	0.9	3.0	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7	
t _{pd}	Propagation Delay B to C _n + 4	2.0	8.0	1.9	8.5	1.9	8.1	ns	"	"	"	"	"	"	
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7	
t _{pd}	Propagation Delay M to F	3.0	10	2.8	10.2	2.3	10.3	ns	"	"	"	"	"	"	
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7	
t _{pd}	Propagation Delay S to F	3.0	10	2.6	10.2	2.7	10.2	ns	"	"	"	"	"	"	

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				Min	Max	Min	Max		Min	Max		V _{IN}	V _{OUT}	V _{CC}	VEEL	PS ₁
t _{TLH} / t _{THL}	Functional Parameters:															
	Rise & Fall Time	1.1	5.0	1.0	5.1	1.0	5.1	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22		2 - 7	
t _{pd}	Propagation Delay S to P _G	2.0	8.0	1.8	8.1	1.9	8.1	ns	"	"	"	"	"	"	"	
t _{TLH} / t _{THL}	Rise & Fall Time	1.1	5.0	1.0	5.1	1.0	5.1	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22		2 - 7	
t _{pd}	Propagation Delay S to C _n + 4	2.0	9.0	1.8	9.1	1.9	9.1	ns	"	"	"	"	"	"	"	
t _{TLH} / t _{THL}	Rise & Fall Time	0.8	6.0	0.8	6.2	0.8	6.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22		2 - 7	
t _{pd}	Propagation Delay S to G _G	2.0	9.0	1.7	9.1	1.7	9.2	ns	"	"	"	"	"	"	"	