GigaBit Logic

10G044

T-68-21-51

3 to 8-Line or Dual 2 to 4-Line Decoder/Demux Boolean Function Generator • 650 ps Delay

10G PicoLogic™ Family

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DISTINCTIVE CAPABILITIES

- Dual independent 2- to 4-line decoders
- Single 3- to 8-line decoder operation
- Dual 1:4 or single 1:8 demultiplexing capability
- Expandable to 1 of 24 with no external comps.
- Boolean function generation capability
- Active low mutually exclusive outputs
- Up to 1.6 GHz input freq. supported
- ECL and PicoLogic family compatible I/O
- Wired-OR output capability
- Temperature and voltage compensated design
- Available in leadless or C-leaded chip carriers or in die form
- Packages contain internal decoupling capacitors for optimum high frequency performance
- 0°C to 85°C operating temperature range

APPLICATIONS

- High speed memory decoding
- Data transmission systems
- Demultiplexers
- Function generation

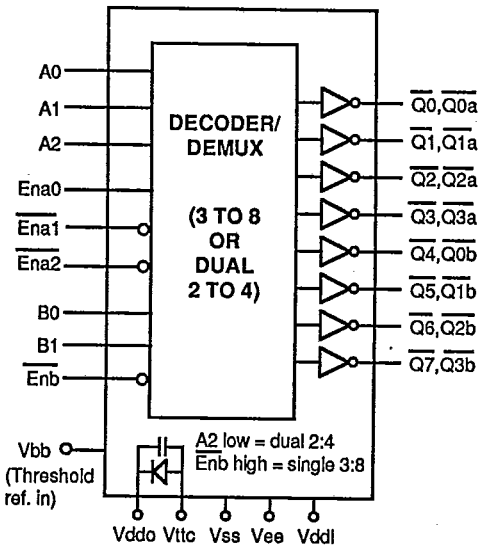
FUNCTIONAL DESCRIPTION

The 10G044 is an ECL and PicoLogic family compatible ultra-fast GaAs digital integrated circuit that is designed to perform the work of five separate devices. The 10G044 can be operated as a : 1) dual 2-to-4 line decoder; 2) single 3-to-8 line decoder; 3) dual 1:4 addressable demultiplexer; 4) single1:8 addressable demultiplexer; 5) Boolean function generator. When A2 is low, the 10G044 functions as a dual 2- to 4-line decoder or dual 1:4 Demux; when $\overline{Enb}$ is held high, the device operates as a single 3- to 8-line decoder or single 1:8 Demux. For compatibility with any ECL or GaAs logic family, the 10G044 incorporates the PicoLogic standard input threshold compensation circuit driven by the VBB input.

Typical address to output propagation delay is 500 ps. Typical output delays from the Enable inputs are 750 ps (Ena0) and 650 ps ($\overline{Enx}$). The 10G044 can support an input frequency of 1.6 GHz while dissipating less than 1.4W at room temperature. Output rise and fall times are typically 150 ps.

The 10G044 is a member of GigaBit Logic's 10G PicoLogic family of gallium arsenide integrated circuits and is fabricated using GigaBit's high volume, GaAs MESFET process technology.

BLOCK DIAGRAM



10G044 ORDERING INFORMATION

PACKAGE TYPE	DELAY (25°C max, An - Qn)
	650 ps
40 pin Leadless CC	10G044-2L
40 pin C-Leaded CC	10G044-2C
Die	10G044-2X

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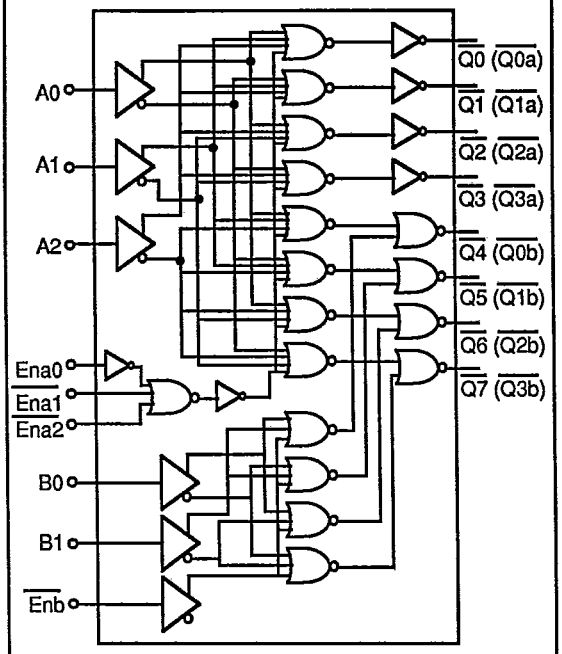
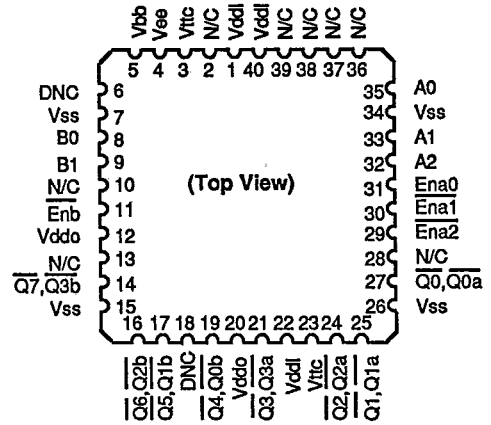
10G044 LOGIC DIAGRAM



PACKAGE PIN FUNCTION DIAGRAM

PACKAGE TYPES "L" AND "C"



NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = Do Not Connect.

DUAL 2-TO-4 LINE DECODING & DUAL 1:4 DEMULTIPLEXING*

A Side

Ena0	$\overline{Ena1}$	$\overline{Ena2}$	A1	A0	$\overline{Q0a}$	$\overline{Q1a}$	$\overline{Q2a}$	$\overline{Q3a}$
L	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	H	X	X	H	H	H	H
H	L	L	L	L	L	H	H	H
H	L	L	L	H	H	L	H	H
H	L	L	H	L	H	H	L	H
H	L	L	H	H	H	H	H	L

A2 = L

*Ena0, $\overline{Ena1}$ or $\overline{Ena2}$ used as DEMUX data input.

B Side

$\overline{Enb}$	B1	B0	$\overline{Q0b}$	$\overline{Q1b}$	$\overline{Q2b}$	$\overline{Q3b}$
H	X	X	H	H	H	H
L	L	L	Q	H	H	H
L	L	H	H	Q	H	H
L	H	L	H	H	Q	H
L	H	H	H	H	H	Q

A2 = L

*Q = L for 2- to 4-line decoding.
Q = $\overline{Enb}$ for 1:4 demultiplexing

The 10G044 functions as either two independent 2-to-4 line decoders or as a single 3-to-8 line decoder. In the dual 2-to-4 mode, the address inputs are A0, A1 and B0, B1 with A2 unused and held low. Each of the two independent decoders accepts their respective A and B address inputs and provides four mutually exclusive active low outputs: Q0a-Q3a and Q0b-Q3b respectively. The A side has one active high and two active low enables; Ena0, $\overline{Ena1}$ and $\overline{Ena2}$. The B side has one active low enable, $\overline{Enb}$.

When disabled, all outputs are forced high. The B enable input and any one of the two active low A side enables (or Ena0 if data inversion is desired) can be used as the data inputs when the 10G044 is operated as a dual 1:4 demultiplexer. In this case, the A2 input must also be held low to enable the B outputs. The remaining two A side enables can be used as data input strobes for the A side demultiplexer. A0, A1 and B0, B1 provide the A side and B side demultiplexer address inputs respectively.

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3-TO-8 LINE DECODING & 1:8 DEMULTIPLEXING

Ena0	$\overline{Ena1}$	$\overline{Ena2}$	A2	A1	A0	$\overline{Q0}$	$\overline{Q1}$	$\overline{Q2}$	$\overline{Q3}$	$\overline{Q4}$	$\overline{Q5}$	$\overline{Q6}$	$\overline{Q7}$	FUNCTION
L	X	X	X	X	X	H	H	H	H	H	H	H	H	Output disable
X	H	X	X	X	X	H	H	H	H	H	H	H	H	
X	X	H	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	Q	H	H	H	H	H	H	H	3-to-8 decoding or 1:8 demultiplexing
H	L	L	L	L	H	H	Q	H	H	H	H	H	H	
H	L	L	L	H	L	H	H	Q	H	H	H	H	H	
H	L	L	L	H	H	H	H	H	Q	H	H	H	H	
H	L	L	H	L	L	H	H	H	H	Q	H	H	H	
H	L	L	H	L	H	H	H	H	H	H	Q	H	H	
H	L	L	H	H	L	H	H	H	H	H	H	Q	H	
H	L	L	H	H	H	H	H	H	H	H	H	H	Q	

Enb = H Q = L for 3-to-8 decoding; Q = Ena0 inverse, $\overline{Ena1}$ or $\overline{Ena2}$ for 1:8 demultiplexing.

In the 3-to-8 line decoder mode, the 10G044 accepts three binary weighted inputs - A0, A1 and A2 - and when enabled, provides eight mutually exclusive active low outputs, $\overline{Q0}$ through $\overline{Q7}$. The $\overline{Enb}$ pin must be tied high in this mode. To configure an eight output addressable demultiplexer, the address inputs are provided on A0, A1 and A2 and either $\overline{Ena1}$ or $\overline{Ena2}$ is used as the data input pin (or Ena0 if data inversion is desired). The remaining two unused A side enables can be used as data input strobes. $\overline{Enb}$ must be held high in this case as well.

BOOLEAN FUNCTION GENERATION

When A2 is held low, the 10G044 can simultaneously generate the four minterms of the input variables A0 and A1 and the four minterms of inputs B0 and B1. Additionally, when A2 is held high, the 10G044 will generate the minterms of the A inputs (A0, A1) NORed with the minterms of the B inputs in corresponding pairs. In both cases, the generation of A and B input minterms can be controlled by the respective A and B input enables. These operations are shown in the following three truth tables.

Minterm generation of the variables A0 and A1 and associated enables

Ena0	$\overline{Ena1}$	$\overline{Ena2}$	A1	A0	$\overline{Q0a}$	$\overline{Q1a}$	$\overline{Q2a}$	$\overline{Q3a}$	FUNCTION
L	X	X	X	X	H	H	H	H	Output disable
X	H	X	X	X	H	H	H	H	
X	X	H	X	X	H	H	H	H	
H	L	L	L	L	L	H	H	H	A minterms
H	L	L	L	H	H	L	H	H	
H	L	L	H	L	H	H	L	H	
H	L	L	H	H	H	H	H	L	

$\overline{Q0a} = \overline{(\overline{A0} \cdot \overline{A1})}$

$\overline{Q1a} = \overline{(A0 \cdot \overline{A1})}$

$\overline{Q2a} = \overline{(\overline{A0} \cdot A1)}$

$\overline{Q3a} = \overline{(A0 \cdot A1)}$

A2 = L

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Minterm generation of the variables B0 and B1 & associated enables

$\overline{Enb}$	B1	B0	$\overline{Q0b}$	$\overline{Q1b}$	$\overline{Q2b}$	$\overline{Q3b}$	FUNCTION
H	X	X	H	H	H	H	Output disable
L	L	L	L	H	H	H	B Minterms $\overline{Q0b} = \overline{(\overline{B0} \cdot \overline{B1})}$
L	L	H	H	L	H	H	$\overline{Q1b} = \overline{(B0 \cdot \overline{B1})}$
L	H	L	H	H	L	H	$\overline{Q2b} = \overline{(\overline{B0} \cdot B1)}$
L	H	H	H	H	H	L	$\overline{Q3b} = \overline{(B0 \cdot B1)}$

A2 = L

Again, the operations expressed in these previous two tables can occur simultaneously. When A2 is held high, the eight individual minterms described above are functionally NORed together in corresponding pairs and are made available on the four $\overline{Qb}$ output pins. In addition, by controlling the Ena2 and Enb pins, the minterms of the A0, A1 inputs or the B0, B1 inputs can be generated and directed to the same $\overline{Qb}$ output pins. These operations are shown in the following table.

Selecting B output minterms and sum of products minterm generation

Ena0	$\overline{Ena1}$	$\overline{Ena2}$	$\overline{Enb}$	A1	A0	B1	B0	$\overline{Q0b}$	$\overline{Q1b}$	$\overline{Q2b}$	$\overline{Q3b}$	FUNCTION
L	X	X	H	X	X	X	X	H	H	H	H	
X	H	X	H	X	X	X	X	H	H	H	H	Output disable
X	X	H	H	X	X	X	X	H	H	H	H	
H	L	L	H	0	0	X	X	L	H	H	H	$\overline{Q0b} = \overline{(\overline{A0} \cdot \overline{A1})}$
H	L	L	H	0	1	X	X	H	L	H	H	$\overline{Q1b} = \overline{(A0 \cdot \overline{A1})}$
H	L	L	H	1	0	X	X	H	H	L	H	$\overline{Q2b} = \overline{(\overline{A0} \cdot A1)}$
H	L	L	H	1	1	X	X	H	H	H	L	$\overline{Q3b} = \overline{(A0 \cdot A1)}$
X	X	H	L	X	X	0	0	L	H	H	H	$\overline{Q0b} = \overline{(\overline{B0} \cdot \overline{B1})}$
X	X	H	L	X	X	0	1	H	L	H	H	$\overline{Q1b} = \overline{(B0 \cdot \overline{B1})}$
X	X	H	L	X	X	1	0	H	H	L	H	$\overline{Q2b} = \overline{(\overline{B0} \cdot B1)}$
X	X	H	L	X	X	1	1	H	H	H	L	$\overline{Q3b} = \overline{(B0 \cdot B1)}$
H	L	L	L	0	0	0	0	L	H	H	H	
H	L	L	L	0	0	0	1	L	L	H	H	
H	L	L	L	0	0	1	0	L	H	L	H	
H	L	L	L	0	0	1	1	L	H	H	L	
H	L	L	L	0	1	0	0	L	L	H	H	$\overline{Q0b} = \overline{(\overline{A0} \cdot \overline{A1})} + \overline{(\overline{B0} \cdot \overline{B1})}$
H	L	L	L	0	1	0	1	H	L	H	H	
H	L	L	L	0	1	1	0	H	L	L	H	$\overline{Q1b} = \overline{(A0 \cdot \overline{A1})} + \overline{(B0 \cdot \overline{B1})}$
H	L	L	L	0	1	1	1	H	L	H	L	
H	L	L	L	1	0	0	0	L	H	L	H	
H	L	L	L	1	0	0	1	H	L	L	H	$\overline{Q2b} = \overline{(\overline{A0} \cdot A1)} + \overline{(\overline{B0} \cdot B1)}$
H	L	L	L	1	0	1	0	H	H	L	H	
H	L	L	L	1	0	1	1	H	H	L	L	$\overline{Q3b} = \overline{(A0 \cdot A1)} + \overline{(B0 \cdot B1)}$
H	L	L	L	1	1	0	0	L	H	H	L	
H	L	L	L	1	1	0	1	H	L	H	L	
H	L	L	L	1	1	1	0	H	H	L	L	
H	L	L	L	1	1	1	1	H	H	H	L	

A2 = H

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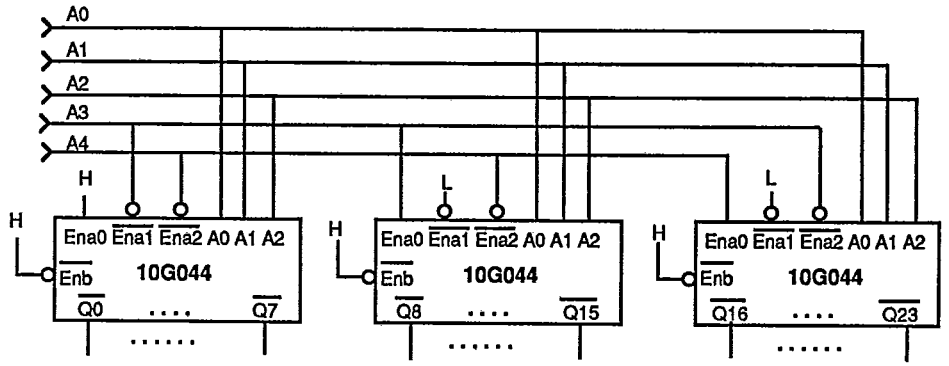
EXPANSION TO 24 DECODED OUTPUTS



A4	A3	
0	0	Only Q0 to Q7 enabled
0	1	Only Q8 to Q15 enabled
1	0	Only Q16 to Q23 enabled
1	1	All outputs disabled (high)

H = Vddo or Vddl
L = Vtt or Vss

PIN DESCRIPTIONS

A0, A1,A2	3:8 decoder address inputs
A0, A1	2:4 decoder A address inputs
Ena0, Ena1, Ena2	3:8 and 2:4 decoder A side enable inputs
B0, B1	2:4 decoder B address inputs
Enb	2:4 decoder B enable input
Q0 - Q7	3:8 decoder outputs
Q0a - Q3a	2:4 decoder A outputs
Q0b - Q3b	2:4 decoder B outputs
VDDO	Ground connection for the output drivers
VDDL	Ground connection for internal switching logic
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	Internal VDDO decoupling capacitor return pin. VTTC is brought into the 10G044 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the 10G044 die. VTTC is typically tied to VTT (nom. -2.0V).
VBB	Input to the 10G044's input threshold compensation circuit. Connect to Vbb supplied from ECL when driving from ECL; connect to the PicoLogic threshold reference voltage (VBBS) when driving from PicoLogic. (NOTE: the 10G044 does not provide a VBBS output).
DNC	Do Not Connect to this pin.
N/C	No connection.

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DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd., unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VIH	Input Voltage High					1
VIL	Input Voltage Low					1
ISS	Power Supply Current		280	370	mA	
IEE	Power Supply Current		75	100	mA	
PD	Power Dissipation		1.35	1.8	W	

NOTES:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

1. Ena1 and Ena2 are unbuffered inputs. Either one, but not both simultaneously, may be driven with ECL levels. The other must be driven with GaAs levels of VIH min = -0.8 V and VIL max = -1.8 V.

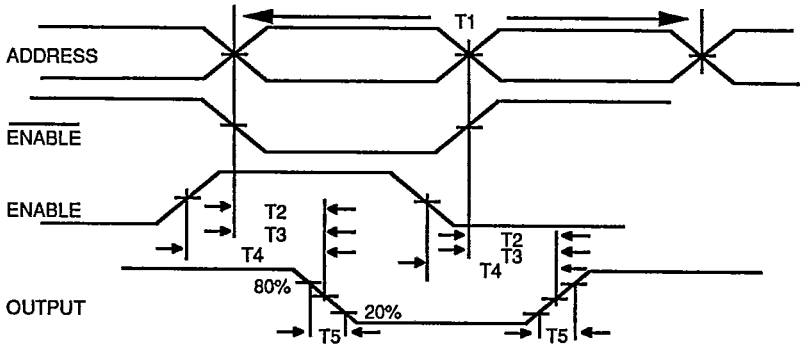
AC CHARACTERISTICS (Note 1)

10G044-2 VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Input frequency	1.2		1.2	1.6		1.2		GHz	
T2	Address to output delay	400	700	325	500	650	425	750	ps	
T3	$\overline{\text{Enable}}$ to output delay	475	850	450	650	800	500	900	ps	
T4	Enable to output delay	525	950	500	750	900	550	1000	ps	
T5	Output rise and fall times		175		125	175		215	ps	2

Notes: 1. Test conditions (unless otherwise noted): Vbb = -1.2V; Vtt = -2.0V; Vttc = Vtt; Rload = 50Ω to Vtt; Vih = -0.7V; Vil = -1.7V; Voh≥ -0.7V; Vol ≤ -1.7V. Input signal rise and fall times ≤ 150 ps.
2. Rise & fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



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24 PIN HYBRID 18 PIN PACKAGE

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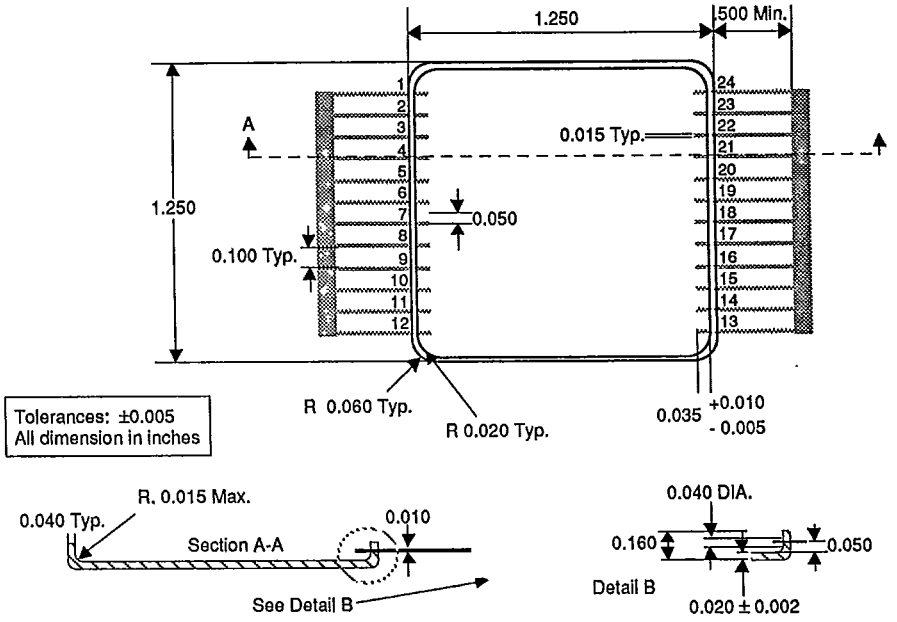
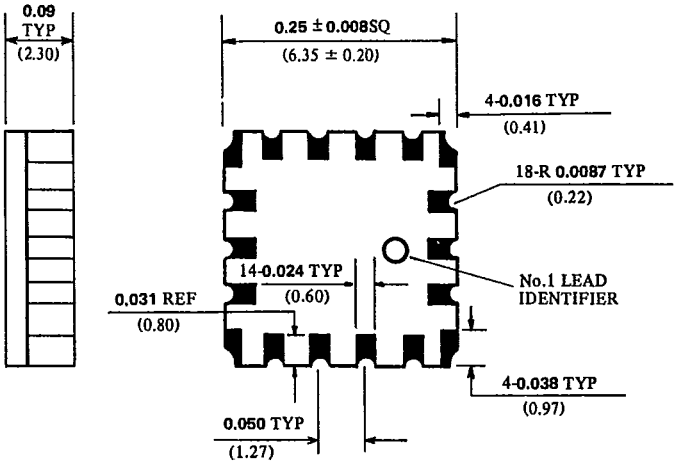
24 PIN HYBRID PACKAGE

Type H



18 PIN LEADLESS CHIP CARRIER

TYPE L1



All dimensions shown in **inches** and (millimeters)

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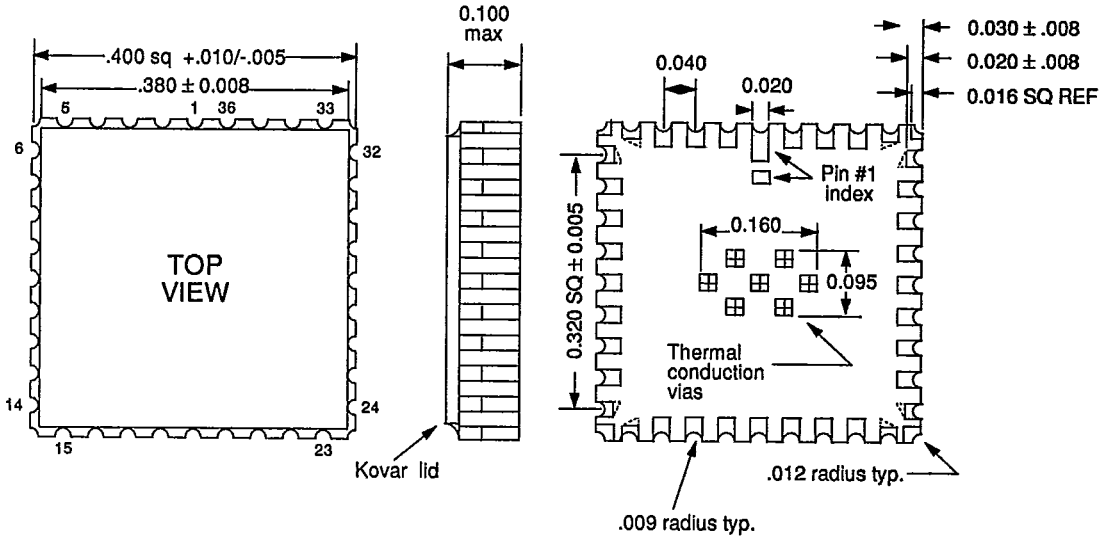
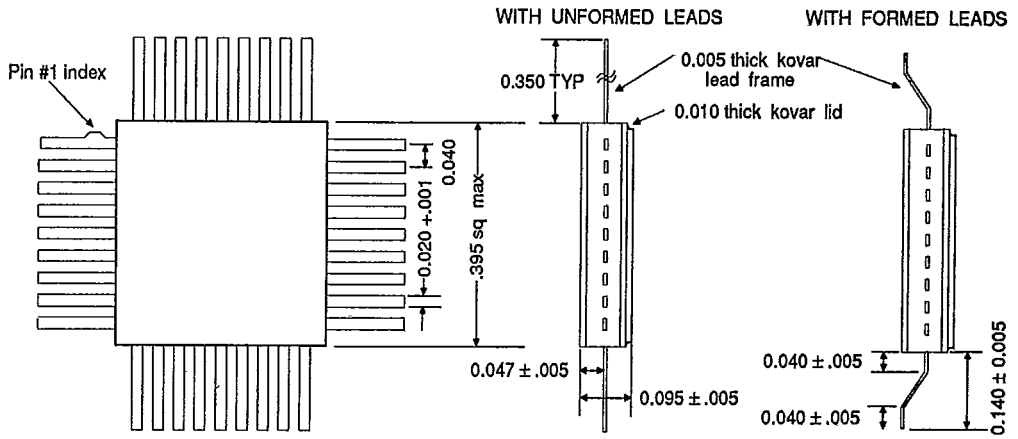
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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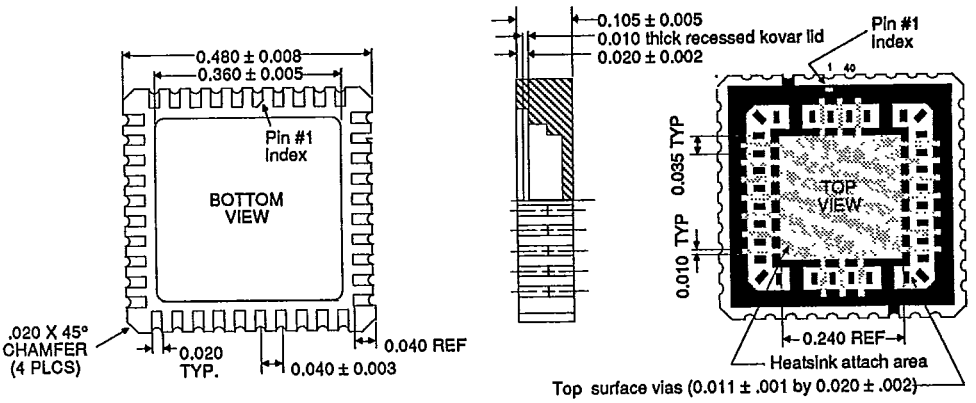
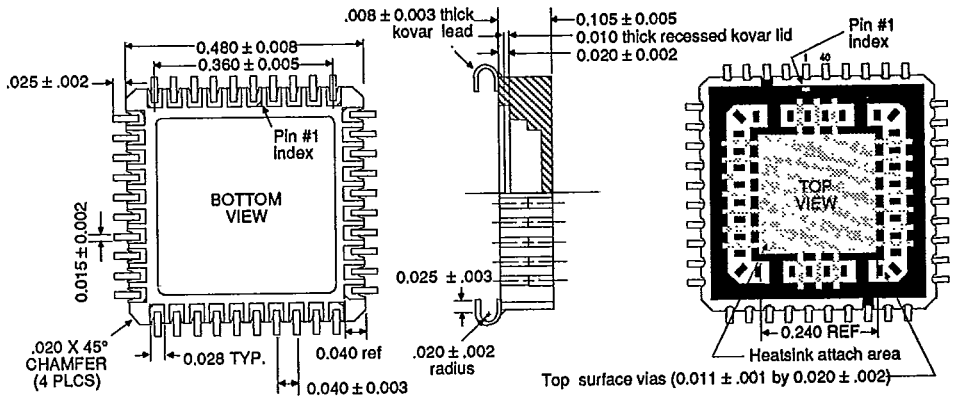
GigaBit Logic

40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

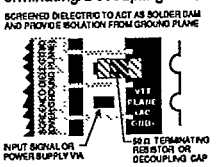


NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:
Metalized Ceramic.....
Screened Dielectric.....
Bare Ceramic.....

Top Surface Terminating/Decoupling Detail

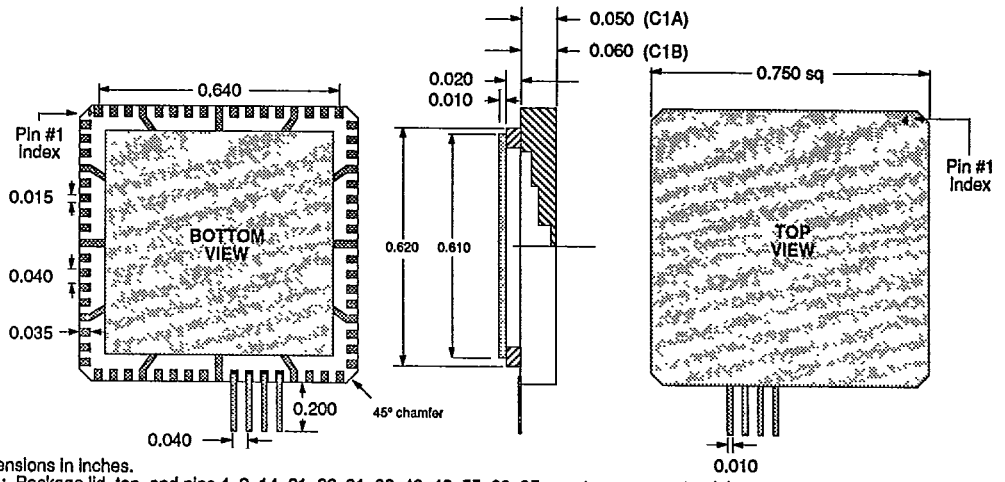


GigaBit Logic

68 & 132 PIN PACKAGES

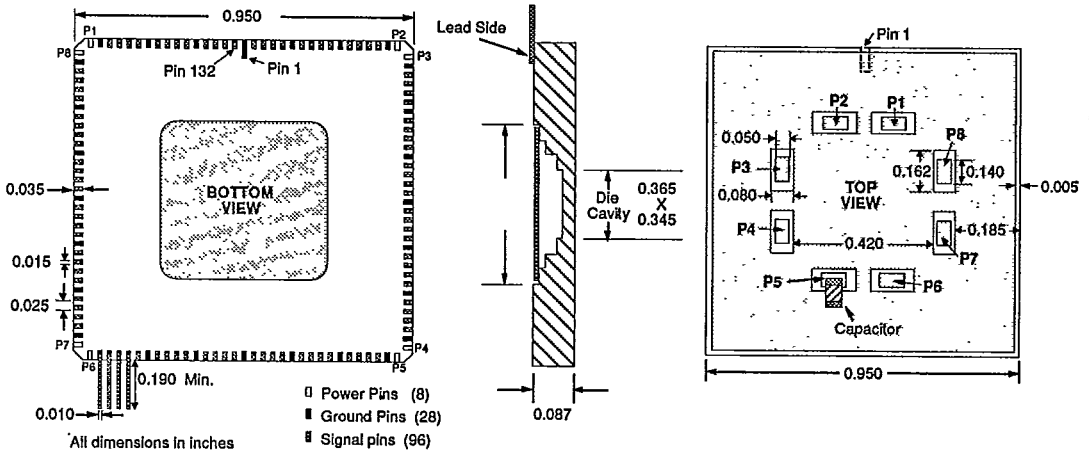
T-90-20

68 PIN LEADED CHIP CARRIER
TYPE C1



(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3



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