



Triple 4-3-3 Input NOR Gate

ELECTRICALLY TESTED PER:
5962-8756401

The 10H506 is a Triple 4-3-3 input **NOR** gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply.

- Propagation Delay, 1.0 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
VCC1	1	5	2	GND
BOUT	2	6	3	51 Ω to VTT
AOUT	3	7	4	51 Ω to VTT
AIN	4	8	5	51 Ω to VTT
AIN	5	9	7	OPEN
AIN	6	10	8	OPEN
AIN	7	11	9	OPEN
VEE	8	12	10	VEE
BIN	9	13	12	OPEN
BIN	10	14	13	51 Ω to VTT
BIN	11	15	14	OPEN
CIN	12	16	15	OPEN
CIN	13	1	17	OPEN
CIN	14	2	18	51 Ω to VTT
COUT	15	3	19	51 Ω to VTT
VCC2	16	4	20	GND

BURN - IN CONDITIONS:

VTT = - 2.0 V MAX/ - 2.2 V MIN

VEE = - 5.7 V MAX/ - 5.2 V MIN

Military 10H506

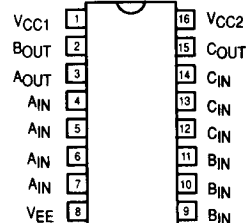


AVAILABLE AS

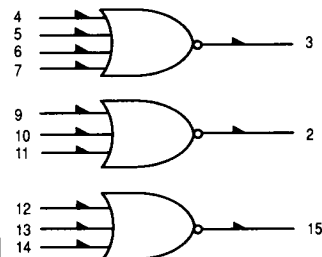
- 1) JAN: N/A
 - 2) SMD: 5962-8756401
 - 3) 883: 10H506/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

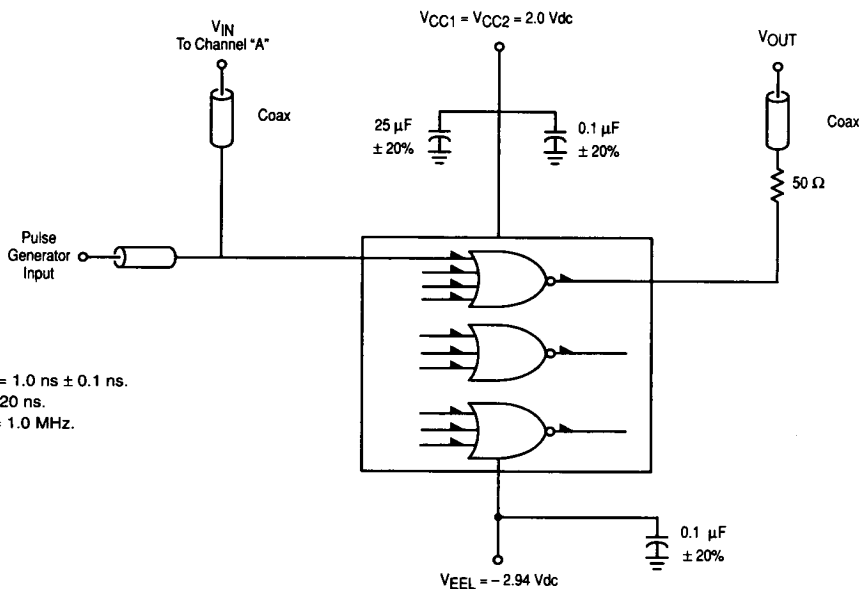
The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



10H506



NOTES

1. $t_r = t_f = 1.0 \text{ ns} \pm 0.1 \text{ ns}$.
2. $P_W \geq 20 \text{ ns}$.
3. $PRF = 1.0 \text{ MHz}$.

NOTES

1. All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100Ω resistor to ground.

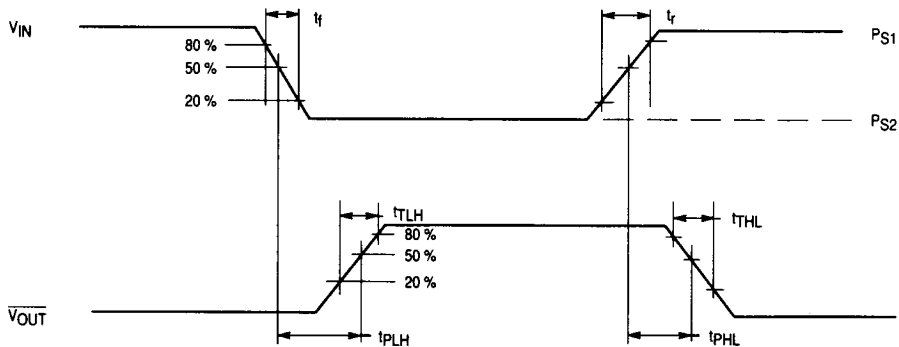


Figure 1. Switching Test Circuit and Waveforms

10H506 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	VEE1	VEE2	VEEL	VEEL
T _A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-2.94
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-2.94
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 0 V, Output Load = 100 Ω to -2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{EE1}	V _{EE2}	V _{CC}	P.U.T.		
V _{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V		4-7 9-14			8		1, 16	2, 3, 15		
V _{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V	4-7 9-14				8		1, 16	2, 3, 15		
V _{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V				4-7 9-14	8	8	1, 16	2, 3, 15		
V _{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V			4-7 9-14		8	8	1, 16	2, 3, 15		
I _{EE}	Power Supply Current	-21		-23		-23		mA					8		1, 16	8		
I _{IH1}	Input Current High		310		500		500	μA	4-7 9-14				8		1, 16	4-7, 9-14		
I _{IL}	Input Current Low	0.5		0.3		0.5		μA		4-7 9-14				8	1, 16	4-7, 9-14		

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max							
t _{TLH}	Rise Time	0.6	1.8	0.55	1.9	0.5	1.7	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	P.U.T.	
t _{THL}	Fall time	0.6	1.8	0.55	1.9	0.5	1.7	ns	10	2	1, 16	8	3, 15	
t _{PHL}	Propagation Delay High to Low	0.5	1.75	0.55	1.8	0.5	1.7	ns	13	15	1, 16	8	2, 3	
t _{PLH}	Propagation Delay Low to High	0.5	1.75	0.55	1.8	0.5	1.7	ns	13	15	1, 16	8	2, 3	