MOTOROLA

Dual D Type Master-Slave Flip-Flop

Military 10H531

ELECTRICALLY TESTED PER:
5962-8756101

The 10H531 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

2

- Propagation Delay, 1.0 ns Typical
- 340 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8756101
3) 883: 10H531/BXAJC
X = CASE OUTLINE AS FOLLOWS:

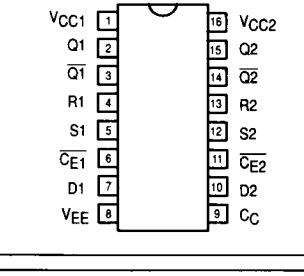
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

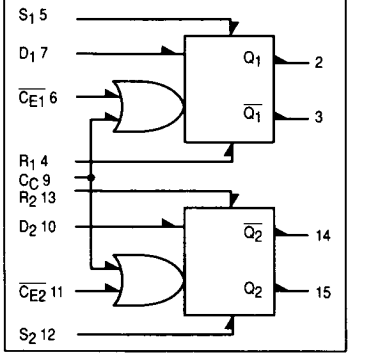
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
$\overline{Q_1}$	3	7	4	51 Ω to V_{TT}
R_1	4	8	5	51 Ω to V_{TT}
S_1	5	9	7	GND
$\overline{C_{E1}}$	6	10	8	OPEN
D_1	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
C_C	9	13	12	OPEN
D_2	10	14	13	OPEN
$\overline{C_{E2}}$	11	15	14	OPEN
S_2	12	16	15	GND
R_2	13	1	17	51 Ω to V_{TT}
$\overline{Q_2}$	14	2	18	51 Ω to V_{TT}
Q_2	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM

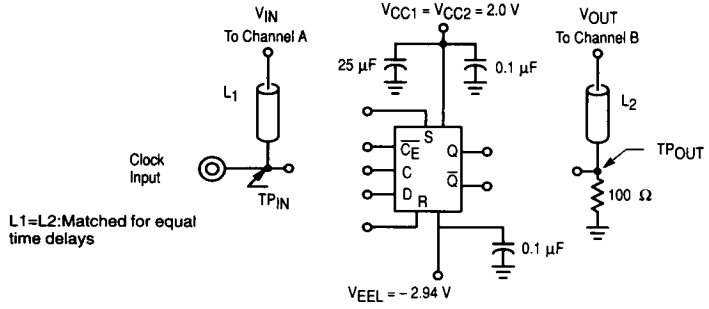


R-S Truth Table		
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined
A clock H is a clock transition from a Low to High state

Clock Truth Table		
C	D	Q_{n+1}
L	Ø	Q_n
H	L	L
H	H	H

Ø = Don't Care
$C = \overline{CE} + C_C$



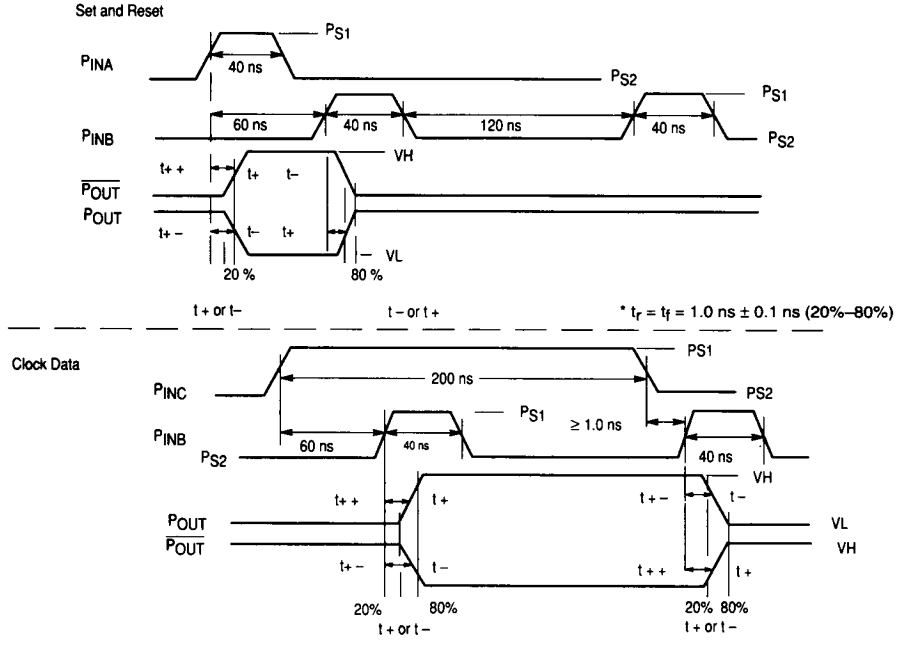


Figure 1. Switching Test Circuit and Waveforms

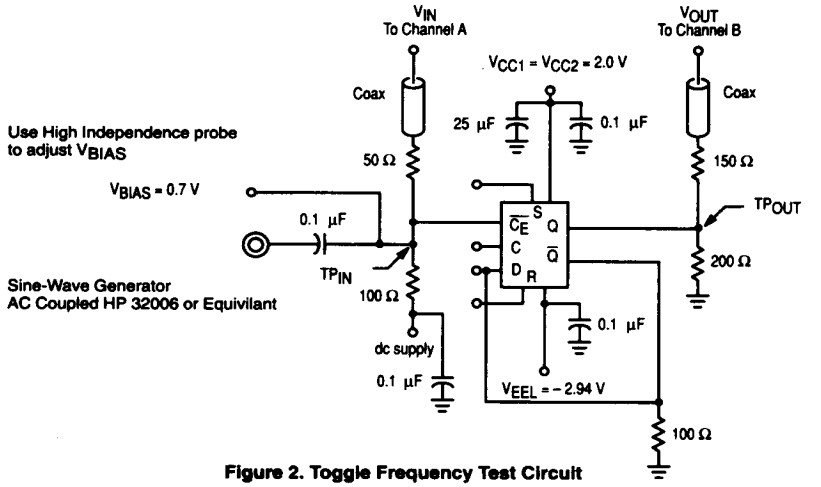
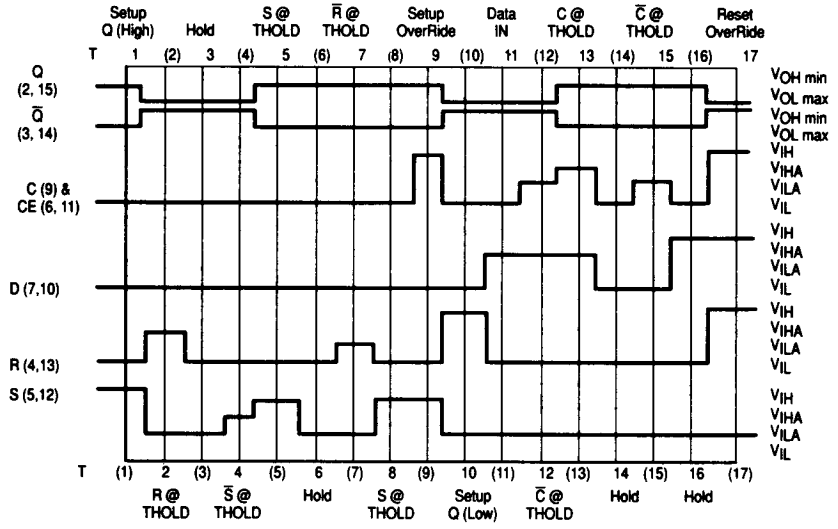
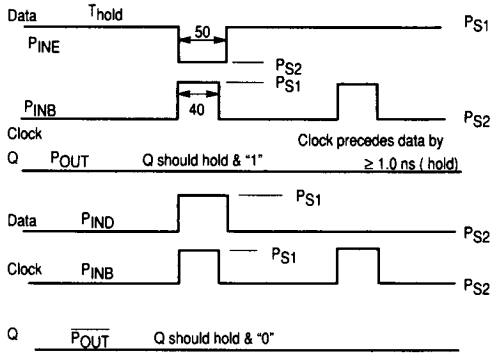


Figure 2. Toggle Frequency Test Circuit

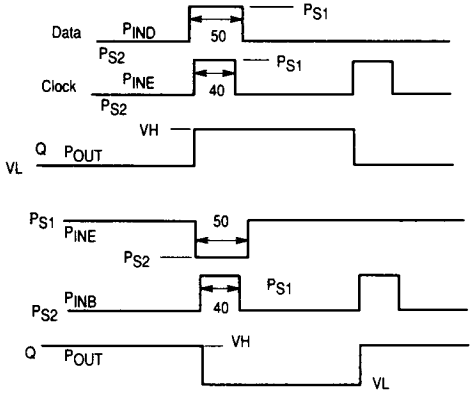


Note: Do not remove power during sequence of tests.

Figure 3. Timing Diagram



NOTES
1. t_{hold} is min. time after positive transition of the clock pulse that information must remain unchanged at the data input.
2. For all t_{hold} tests, pulse width should not be less than 20 ns.



NOTES
1. t_{setup} is the min. time before the positive transition of the clock information must be present at the data input.
2. For all setup tests, pulse widths should not be less than 20 ns.

Data precedes clock by ≤ 1.5 ns (setup)

Figure 4. T_{HOLD} Waveforms

10H531
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.780	-1.950	-1.110	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.650	-1.950	-0.960	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.840	-1.950	-1.160	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4, 5 12, 13	4 – 7 9 – 13	8		1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	5, 12	4 – 7 9 – 13	8		1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V			8	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V			8	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	–56		–62		–62		mA		6, 11	8		1, 16	8
I_{IH}	Input Current High		390		660		660	µA	9		8		1, 16	9
I_{IH1}	Input Current High		310		530		530	µA	6, 11		8		1, 16	6, 11
I_{IH2}	Input Current High		465		790		790	µA	4, 5 12, 13		8		1, 16	4, 5, 12, 13
I_{IH3}	Input Current High		285		485		486	µA	7, 10		8		1, 16	7, 10
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 – 7 9 – 13		8	1, 16	4 – 7, 9 – 13

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
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		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T
t_r	Rise Time	0.5	2.0	0.6	2.2	0.45	1.8	ns	4, 5	3	1, 16	8	2, 14, 15
t_f	Fall Time	0.5	2.0	0.6	2.2	0.45	1.8	ns	4, 5	3	1, 16	8	2, 14, 15
t_{pd}	Propagation Delay CLK, CE, Set, Reset	0.7	2.15	0.7	2.2	0.6	2.1	ns	10, 11	15	1. 16	8	2, 3, 14
t_{SET}	Set Up Time	0.7		0.7		0.7		ns	6, 7, 10, 11	2, 15	1. 16	8	2, 3, 14, 15
t_{HOLD}	Hold Time	0.8		0.8		0.8		ns	6, 7, 10, 11	2, 15	1, 16	8	2, 3, 14, 15
f_{tog}	Toggle Frequency	250		250		250		MHz					(See Fig. 2)