MOTOROLA

Military 10H561

Binary to 1-8 Decoder (Low)

ELECTRICALLY TESTED PER:
5962-8756701

The 10H561 provides parallel decoding of a three bit binary word to one of eight lines. The 10H561 is useful in high-speed multiplexer/demultiplexer applications.

The 10H561 is designed to decode a three bit input word to one of eight output lines. The 10H561 output will be low when selected while all other outputs are high. The enable inputs, when either or both are high, force all outputs high.

The 10H561 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

- Propagation Delay, 1.5 ns Typical
- 470 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8756701
3) 883: 10H561/BXAJC
X = CASE OUTLINE AS FOLLOWS:

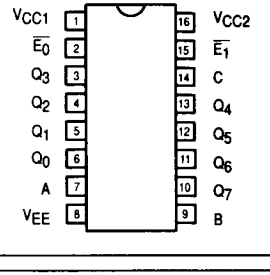
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

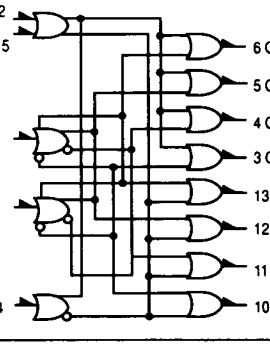
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{E_0}$	2	6	3	GND
Q_3	3	7	4	V_{TT}
Q_2	4	8	5	V_{TT}
Q_1	5	9	7	V_{TT}
Q_0	6	10	8	V_{TT}
A	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B	9	13	12	OPEN
Q_7	10	14	13	V_{TT}
Q_6	11	15	14	V_{TT}
Q_5	12	16	15	V_{TT}
Q_4	13	1	17	V_{TT}
C	14	2	18	GND
$\overline{E_1}$	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



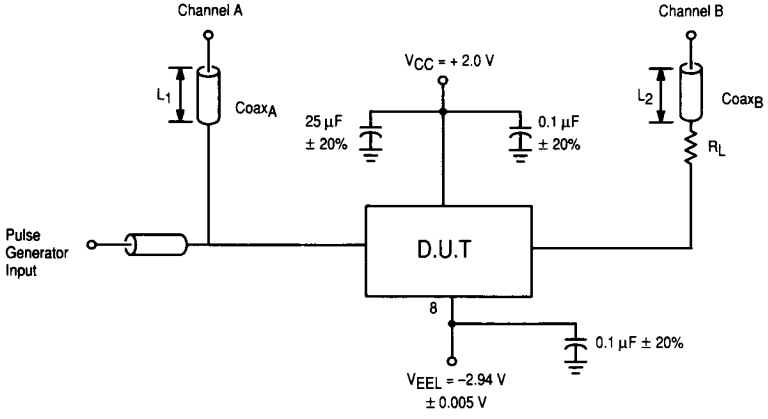
POSITIVE LOGIC DIAGRAM



TRUTH TABLE

Enable Inputs		Inputs			Outputs							
$\overline{E_1}$	$\overline{E_0}$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	Ø	Ø	Ø	Ø	H	H	H	H	H	H	H	H
Ø	H	Ø	Ø	Ø	H	H	H	H	H	H	H	H

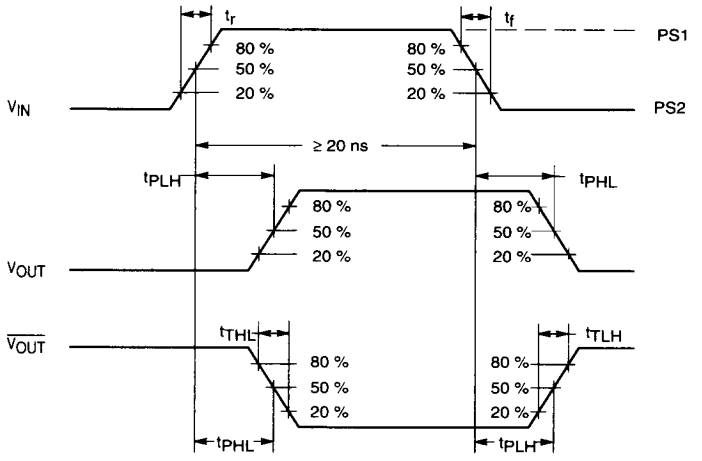
Ø = Don't Care



NOTES

1. All other outputs loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. $L_1 = L_2$: Matched for equal time delay.
4. R_L = 50 Ω.

Figure 1. Switching Test Circuit



NOTES
1. V_{IN} = 20 ns.
2. f_{IN} = 1.0 MHz.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10H561
QUIESCENT LIMIT TABLE*

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	2, 7, 9				8		1, 16	3 - 6, 10 - 13
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.535	-1.95	-1.61	V	7, 9, 14				8		1, 16	3 - 6, 10 - 13
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	7, 9, 14		2, 7, 9 14, 15	7, 9, 14	8	8	1, 16	3 - 6, 10 - 13
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.535	-1.95	-1.61	V	7, 9, 14		7, 9, 14		8	8	1, 16	3 - 6, 10 - 13
I_{EE}	Power Supply Current	-76		-84		-84		mA	2, 7, 9, 14, 15				8		1, 16	8
I_{IH}	Input Current High		275		465		465	µA	2, 7, 9, 14, 15				8		1, 16	2, 7, 9, 14, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2, 7, 9, 14, 15				8	1, 16	2, 7, 9, 14, 15

10H561
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		P_{S2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.55	1.5	0.6	1.6	0.55	1.5	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{THL}	Fall Time	0.55	1.5	0.6	1.6	0.55	1.5	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PLH1}	Propagation Delay Data	0.85	2.1	1.05	2.3	0.8	1.9	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PHL1}	Propagation Delay Data	0.65	2.2	0.7	2.3	0.6	2.2	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PLH}	Rise Time for Pins Enable	1.25	2.3	1.4	2.6	1.15	2.2	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PHL}	Rise Time for Pins Enable	0.8	2.3	0.9	2.4	0.8	2.3	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PLH2}	Propagation Delay Data	0.75	2.1	0.85	2.3	0.7	2.0	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PHL2}	Propagation Delay Data	0.8	2.2	1.0	2.4	0.75	2.2	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13