

Hex "D" Master-Slave Flip-Flop

**ELECTRICALLY TESTED PER:
5962-8751201**

The 10H576 contains six master slave type "D" flip-flops with a common clock. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.7 ns Typical
- 675 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

FUNCTION	PIN ASSIGNMENTS			BURN-IN (CONDITION C)
	DIL	FLATS	LCC	
V _{CC1}	1	5	2	GND
Q ₀	2	6	3	51 Ω to V _{TT}
Q ₁	3	7	4	51 Ω to V _{TT}
Q ₂	4	8	5	51 Ω to V _{TT}
D ₀	5	9	7	GND
D ₁	6	10	8	GND
D ₂	7	11	9	GND
V _{EE}	8	12	10	V _{EE}
Clock	9	13	12	CP1
D ₃	10	14	13	GND
D ₄	11	15	14	GND
D ₅	12	16	15	GND
Q ₃	13	1	17	51 Ω to V _{TT}
Q ₄	14	2	18	51 Ω to V _{TT}
Q ₅	15	3	19	51 Ω to V _{TT}
V _{CC2}	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = -2.0 V MAX/ -2.2 V MIN

V_{EE} = -5.7 V MAX/ -5.2 V MIN

Military 10H576

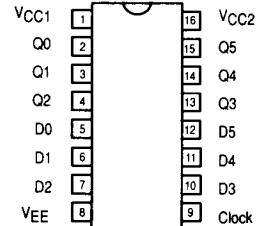


AVAILABLE AS

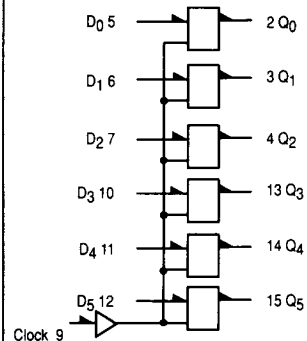
- 1) JAN: N/A
 2) SMD: 5962-8751201
 3) 883: 10H576/BXAJC
 X = CASE OUTLINE AS FOLLOWS:

**PACKAGE: CERDIP: E
 CERFLAT: F
 LCC: 2**

**The letter "M" appears before
 the slash on LCC.**



LOGIC DIAGRAM



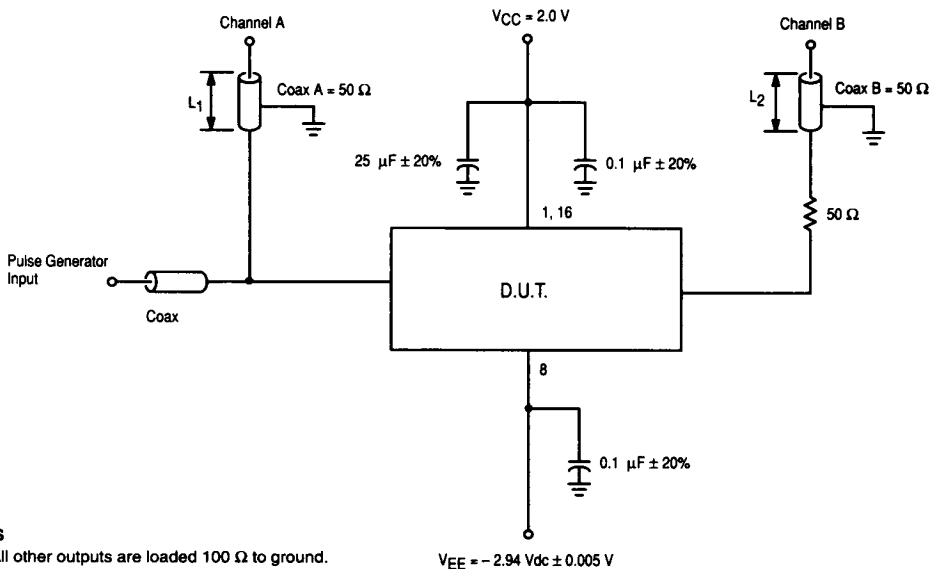
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CLOCK TRUTH TABLE		
C	D	Q_{n+1}
L	$\emptyset$	Q_n
H*	L	L
H*	H	H

$\emptyset$ = Don't Care

* A clock H is a clock transition from a low to a high state

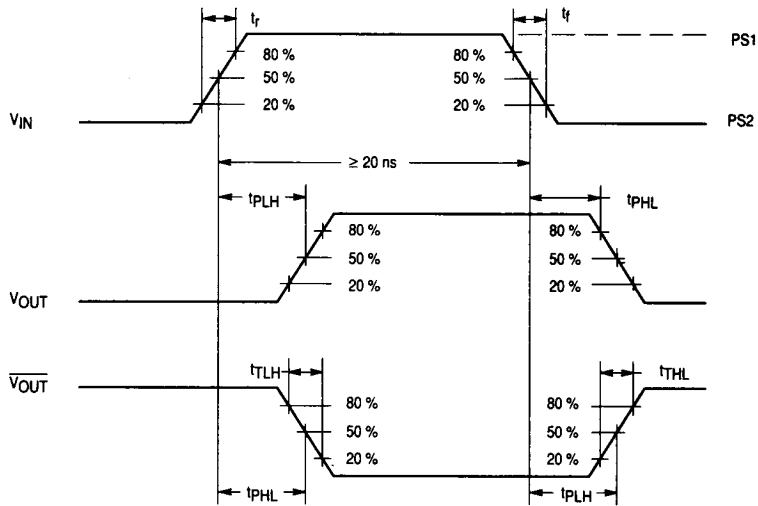
2



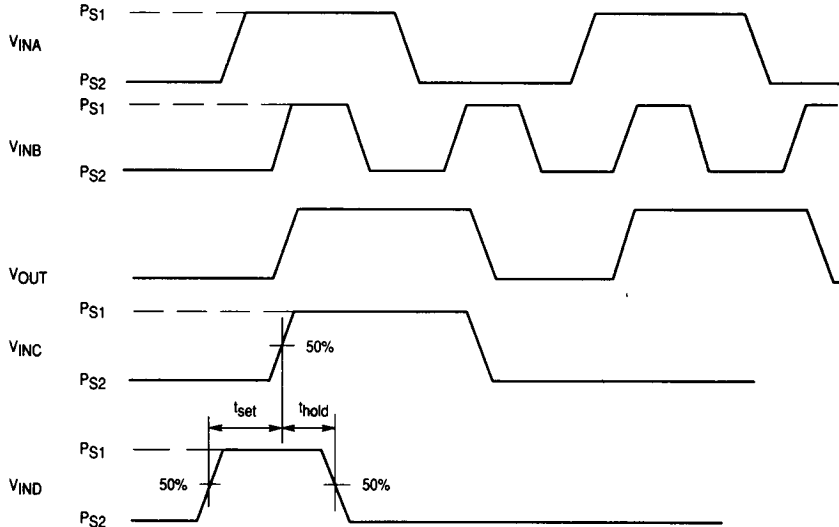
NOTES

1. All other outputs are loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. L_1 : L_2 : Matched for equal time delay.
4. $V_{IN} = 20$ ns.
5. $f_{IN} = 1.0$ MHz.
6. $t_r = t_f = 1.0$ ns (20% - 80%) ± 0.1 ns.

Figure 1. Test Circuit

**NOTES**

1. All other outputs are loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. L₁: L₂: Matched for equal time delay.
4. V_{IN} = 20 ns.
5. f_{IN} = 1.0 MHz.
6. t_r = t_f = 1.0 ns (20% - 80%) $\pm$ 0.1 ns.

Figure 2. Test Circuit Waveform**Figure 3. tSET and tHOLD Waveform**

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QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100.Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	V _{EE1}	V _{EE2}	VEEL	VEEL
T _A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-2.94
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-2.94
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max											
V _{OH}	High Output Voltage	- 1.01	- 0.78	- 0.86	- 0.65	- 1.06	- 0.84	V	5 - 7 10 - 12	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{EE2}	V _{EE1}	V _{CC}	Cp1	P. U. T.
V _{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	- 1.565	- 1.95	- 1.61	V			5 - 7 10 - 12				8	1, 16	9, P ₁	2 - 4 13 - 15
V _{OH1}	High Output Voltage	- 1.01	- 0.78	- 0.86	- 0.65	- 1.06	- 0.84	V	5 - 7 10 - 12	5 - 7 10 - 12	5 - 7 10 - 12	5 - 7 10 - 12	8	8	1, 16	⁹ P ₁ - 3	2 - 4 13 - 15	
V _{OL1}	Low Output Voltage	- 1.96	- 1.58	- 1.95	- 1.565	- 1.95	- 1.61	V	5 - 7 10 - 12	5 - 7 10 - 12		5 - 7 10 - 12	8	8	1, 16	⁹ P ₁ - 3	2 - 4 13 - 15	
I _{EE}	Power Supply Current	- 112		- 123		- 123		mA						8	1, 16		8	
I _{IH}	Input Current High		265		425		425	μA	5 - 7 10 - 12					8	1, 16		5 - 7 10 - 12	
I _{IH1}	Input Current High		420		670		670	μA	9					8	1, 16		9	
I _{IL}	Input Current Low	0.5		0.3		0.5		μA		5 - 7 9 - 12		8			1, 16		5 - 7 10 - 12	

NOTES

1. Hold power during all V_{OH} and V_{OL} tests.

2. P1)  V_{IH}
 P2)  V_{IH}
 V_{IL2}

10H576 QUIESCENT LIMIT TABLE *

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Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS1	PS2	VEE1	VEE2	VEEL	
T _A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	
T _A = 125 °C	-0.65	-1.95	-0.96	-1.485	+1.24	+0.36	-5.46	-4.94	-2.94	
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
Functional Parameters:		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max							
t _{TLH}	Rise Time	0.7	1.8	0.8	1.9	0.8	1.8	ns	5 - 7, 9 - 15	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15	
t _{FHL}	Fall Time	0.7	1.8	0.8	1.9	0.8	1.8	ns	5 - 7, 9 - 15	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15	
t _{PLH}	Propagation Delay	1.0	2.7	1.0	3.0	1.0	2.9	ns	5 - 7, 9 - 15	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15	
t _{PHL}	Propagation Delay	1.0	2.7	1.0	3.0	1.0	2.9	ns	5 - 7, 9 - 15	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15	
t _{Setup}	Setup Time	1.5		1.5		1.5		ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15	
t _{Hold}	Hold Time	0.8		0.8		0.8		ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15	
t _{Toggle}	Toggle Frequency	250		250		250		MHz	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15	