series 185A400





FEATURES

- Full 3 VA Output
- Transformer Isolated Output
- Short Circuit Protection
- Thermal Cutoff Protection
- Integral Heatsinking
- No +5V Supply Required
- Synchro/Resolver Inputs/Outputs

APPLICATIONS

Differential measurement — Control — Digital offset of Synchro Angles

GENERAL DATA

The 185A400 is a family of miniature modularized Solid State Control Differential Transmitters. The analog inputs and outputs can be specified as either synchro or resolver formats. The analog output accurately represents the difference in angle between the analog input and the digital input angles. This output is capable of delivering a full 3VA. The output stage is current limited and features a thermal cutoff to prevent overheating. An integral aluminum top surface on the module provides all the necessary heat-sinking.

INPUT/OUTPUT

The 185A400 has two inputs, an analog angle input ♣ and a 13 bit digital input ♠. The analog output represents the angular difference between the two inputs, (♠-♣). The digital input is parallel natural binary angle format. To accommodate fewer input bits than provided, unused inputs must be grounded. The digital inputs are CMOS with standard CMOS logic levels. The analog output is designed to deliver a continuous full 3VA to CT or CDX type loads; it is not intended for driving TR loads.

OVERTEMPERATURE PROTECTION

The top of the 185A400 consists of a metal top plate which provides all required heat sinking. Thermal resistance from top plate to free air is 15 degrees centigrade per VA. A thermal cutout is included in the design which disables the output power amplifiers when the temperature of the top plate reaches 115 degrees centigrade. Once the top plate temperature drops approximately 10 degrees, the output amplifiers are automatically enabled and normal operation is resumed. Sufficient air circulation should be provided for the metal top.

CAUTION

The digital angle inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic field. Unused devices must be stored in conductive foam.

ELECTRICAL SPECIF Parameter	FICATIONS Value
Accuracy ⁽¹⁾	± 6 minutes
Resolution	13 bits (0.044°)
Digital Input (\$\psi\$)(2)	Parallel binary angle, positive logic, CMOS levels
Analog Input (0)(3)	11.8 Vrms L-L 400 Hz into 100K 90 Vrms L-L 400 Hz into 600K 90 Vrms L-L 60 Hz into 600K
Analog Output (φ-θ) ^{(4) (5)}	11.8 Vrms L-L 400 Hz @ 3VA max. 90 Vrms L-L 400 Hz @ 3VA max. 90 Vrms L-L 60 Hz @ 3VA max.
Overtemperature Output (OT)	Logic '1' = overtemperature 2 TTL loads max.
Power Supplies Voltage Current	± 15V ± 5% 60 ma + load
Temperature Ranges Operating	0 to +70°C -55 to +85°C (ET)

Storage NOTES

- 1. Accuracy applies for:
 - (a) ± 10% variation in power supplies
 - (b) ± 10% signal amplitude variation
 - (c) 10% harmonic distortion
 - (d) any balanced load from no load to full load (e) over operating temperature range
- Signals shall not be applied to digital inputs while the device power supply is off. Digital input levels should not go below ground or exceed +5Vdc.

-55 to +125°C

- Synchro input is a solid state Scott "T"; any one stator may be grounded. Common mode voltages up to specified L-L voltage have no effect on operation.
- Transformer isolated output; any one stator may be grounded.
- 5. For 60 Hz output, external transformers are required.

NOTES

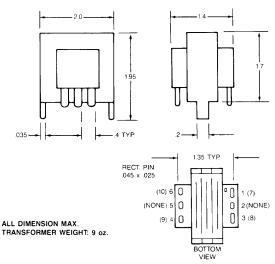
- 1. Non-cumulative
- 2. S4 appears on resolver output models only.
- 3. Designators in parenthesis are for resolver input units.
- 4. Rigid 0.040 diameter pins suitable for solder-in or plug-in applications.

ORDERING INFORMATION

185A Suffix	Analog Input		Analog Output		Frequency
	Туре	Voltage	Туре	Voltage	(Hz)
400	Syn	11.8	Syn	11.8	400
401	Syn	11.8	Syn	90	400
402	Syn	90	Syn	90	400
403	Syn	90	Syn	11.8	400
404	Syn	90	Syn	90	60
405	Res	11.8	Res	11.8	400

Standard temperature range 0 to 70°C, add suffix ET to part number for extended range (– 55 to + 85°C). Consult factory for part numbers describing additional features.

EXTERNAL TRANSFORMERS (60 HZ ONLY)



INTERCONNECTING DIAGRAM

