APR 26 1993

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Military 188100

Advance Information

RISC Multichip Module

MPO

MULTICHIP MODULE

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
4) CMP: 188100-XX/ *

* See Commercial Plus and Avionics Options: (BR914/D)

XX = Speed in MHz (20, 33)

The 188100 Multichip Module consists of one 88100 and two 88200's configured in a HYPERmodule™ Harvard Architecture conveniently packaged in a single 241 pin PGA package. This compact solution offers a 2x footprint savings over the three packaged PGA devices. This product is ideally suited for RISC computing platform solutions in multiprocessing and file server applications. The product is Ada compiler supported and a custom PCB is available for software development.

The 88100 is a reduced instruction set computer (RISC) microprocessor implemented with Motorola's HCMOS technology incorporating 32-bit registers, data paths, and addresses. In designing the 88100, Motorola has incorporated a high degree of fine-grain parallelism; four independent execution units, maintain separate fully concurrent execution pipelines. Most instructions operate in one machine cycle, or effective concurrent execution can be accomplished through internal pipelines in one machine cycle. A common register file provides data sharing and synchronization control among the execution units through register scoreboarding.

The 88200 is a high performance 16-Kbyte Cache Memory Management Unit (CMMU) implemented with Motorola's HCMOS technology providing zero-wait-state memory management and data caching. The memory management unit (MMU) efficiently supports a demand-page virtual memory environment with two logical address ranges (user/supervisor) of 4-Gbytes each. Translated addresses are provided by one of two logical address translation caches (ATCs), providing address translation in one clock cycle for most memory accesses. The page address translation cache (PATC) is a 56-entry, fully associative cache containing recently used translations for 4-Kbyte memory pages and is maintained by 88200 hardware.

The block address translation cache (BATC) is a 10-entry cache, loaded by software containing translations for 512-Kbyte memory blocks. The BATC translations are used for operating system software or other memory-resident instructions and data. In addition, the MMU provides access control for the two logical address spaces. The CMMU data cache is a 16-Kbyte, four-way, set-associative cache for instruction or data storage. The cache incorporates memory-update policies and cache-coherency mechanisms that support multiprocessor applications. The 88200 CMMU also includes an 88100-compatible processor bus (P-bus) interface and a memory bus (M-bus) interface.

Features of the 188100 include:

- One 88100 RISC processor and two 88200 CMMU's in a single multichip module package
- A 241 pin PGA hermetic package with a heatsink/standoff
- Twenty two pull-up resistors (10K Ω) and two pull-down resistors (10K Ω) included in the package
- 20 MHz available, 33 MHz version planned
- Ada supported
- High-Speed Interrupt Processing with Minimal Interrupt Latency
- One design supports a wide range of Microprocessor/Cache Configurations
- Increased Quality, Reliability, and Heat Dissipation
- Small Size (less than 3.25 square inches, or 8.23 square centimeters)
- Applicable with Motorola's Low Skew CMOS Clock Drivers
- Wide Range of software support, including Bus Functional Behavioral Models for the 88100 and 88200
- Printed Circuit Board implementation available for Logic Analysis and Real Time Program Analysis

HYPERmodule is a trademark of Motorola, Inc.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Features of the 88100 are as follows:

- Single-Clock Integer, Logical, Bit Field, Branch, and Store Operations
- 51 Instructions and 7 Data Types
- Fine-Grain Parallelism:
  - — 4 Fully Independent Execution Units with Five Concurrent Pipelines
  - — Execution Synchronized in Hardware by Scoreboard Register
- Nondestructive Register and Condition Code Model Allowing Fast Operand Access and Operand Reuse
- 32 General Purpose Registers
- Single and Double Precision IEEE 754 Floating-Point Compatibility (Up to One Operation per Clock Cycle)
- Full 32-Bit Combinational Multiplier
- Separate Data and Instruction Memory Ports (Harvard Bus Structure) Allowing Simultaneous Accesses:
  - — 30-Bit Data Address Bus
  - — 32-Bit Data Bus (32-Bit Word)
  - — 30-Bit Instruction Address Bus (32-Bit Boundary Addressing)
  - — 32-Bit Instruction Bus (Fixed Instruction Length of 32 Bits)
- Pipelined Load and Store Operations (Up to 80 Mbytes/sec at 20 MHz)
- Functional Redundancy Fault Detection
- Selectable Big-Endian or Little-Endian Byte Ordering
- Complex Instruction Sequences Easily Built from Simple Instructions by High Level Language Compiler
- Extensible Architecture Facility through Special Function Units

Features of the 88200 CMMU are as follows:

- Two Logical Address Spaces of 4-Gbytes each (User Supervisor)
- Automatically Maintained PATC and Software-Maintained BATC
- Write Protection for User and Supervisor Accesses
- Used and Modified Flags Maintained in Page Translation Tables
- 16-Kbytes, Four-way, Set-Associative Physical Cache
- Zero-Wait-State Physical Cache Accesses — Address Translation in Parallel with Cache Access
- LRU (Least Recently Used) Replacement Algorithm for each Cache Set
- Cache Entries Allocated with Copyback or Write-through Policies
- Bus Snoop Protocol Keeps the Cache Consistent with other Caches and with Main Memory
- Cache Flush and Invalidate Initial Selectively by Software and Executed Automatically by Hardware
- Cache Inhibit Flags on Area, Segment, Page, and Block Basis
- Semaphores for Efficient Multiprocessor Synchronization (In Memory and Cached)
- Data Cache and ATC's can be Flushed by any Processor or I/O Device
- Checker Mode Fault Detection (Functional Redundancy)
- Parity-Protected Memory Bus
- Cache Line Disable Flags

For detailed information on Motorola's 88100 and 88200 chip set please refer to the following documentation:

• MC88100UM/AD Rev 1	MC88100 RISC Microprocessor User's Manual, Second Edition
• MC88200UM/AD Rev 1	MC88200 Cache Memory Management Unit User's Manual, Second Edition
• MC88100/D	MC88100 Technical Summary 32-Bit RISC Microprocessor
• MC88200/D	MC88200 Technical Summary 16-Kbyte Cache/Memory Management Unit (CMMU)
• 88KSUPPAK/D	88000 Software and Support "The Source"
• M88KPAK/D	88000 Family Information
• HM88KUM/D2	HM88K HYPERmodule 32-Bit RISC Processor Mezzanine Module User's Manual

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	- 0.3 to + 7.0	V
Input Voltage	V_{IN}	- 0.3 to + 7.0	V
Operating Temperature	T_A	- 55 to + 125	°C
Storage Temperature Range	T_{STG}	- 55 to + 150	°C

THERMAL CHARACTERISTICS — PGA PACKAGE

Parameter	Symbol	Value	Unit
Thermal Resistance — Ceramic		Preliminary	°C/W
Junction to Ambient	θ_{JA}	3.3	
Junction to Case	θ_{JC}	2.2	

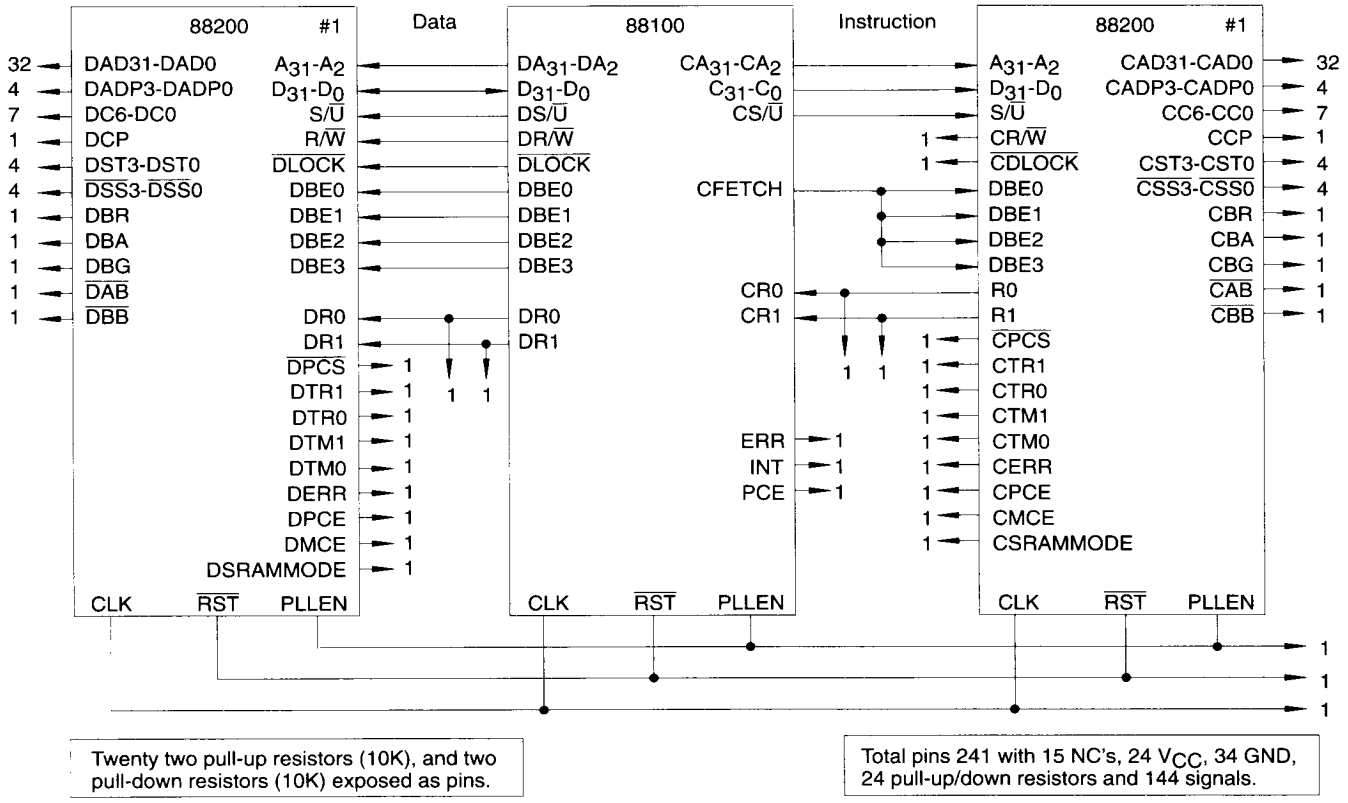
DC CHARACTERISTICS

(V_{CC} = 5 V_{dc} ± 5%, GND = 0 V_{dc}, T_A = - 55°C to + 125°C)

Characteristic	Symbol	Min	Max	Unit
Clock Low Voltage	V_{CL}	- 0.3	0.2 V_{CC}	V
Clock High Voltage	V_{CH}	- 0.8 V_{CC}	V_{CC} + 0.3	V
Input Low Voltage (All Inputs Except CLK)	V_{IL}	- 0.3	0.8	V
Input High Voltage (All Inputs Except CLK)	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage @ 8 mA I_{OL}	V_{OL}	—	0.5	V
Output High Voltage @ - 4 mA I_{OH}	V_{OH}	2.4	—	V
Input Leakage Current	I_{IN}	—	10	µA
High-Impedance Leakage Current	I_{TSI}	—	20	µA
Typical Power Dissipation (T_A = 0 °C) 20 MHz 33 MHz	P_D	—	1.5 1.8	W
Input Capacitance (V_{IN} = 0 V, T_A = 25°C, f = 1 MHz)	C_i	—	15	pF
Output Capacitance (V_{IN} = 0 V, T_A = 25°C, f = 1 MHz)	C_o	—	15	pF
Output Load Capacitance All P-bus Outputs All M-bus Outputs	C_L	—	70 130	pF
AC Output Delay Derating (See Note)	C_{LD}	—	1	ns/25 pF

Note: Only applies when exceeding the specified output load capacitance (C_L). Absolute output load capacitance, per output for correct device operation, must be less than or equal to 120 pF for P-bus and 180 pF for M-bus.

188100 Block Diagram



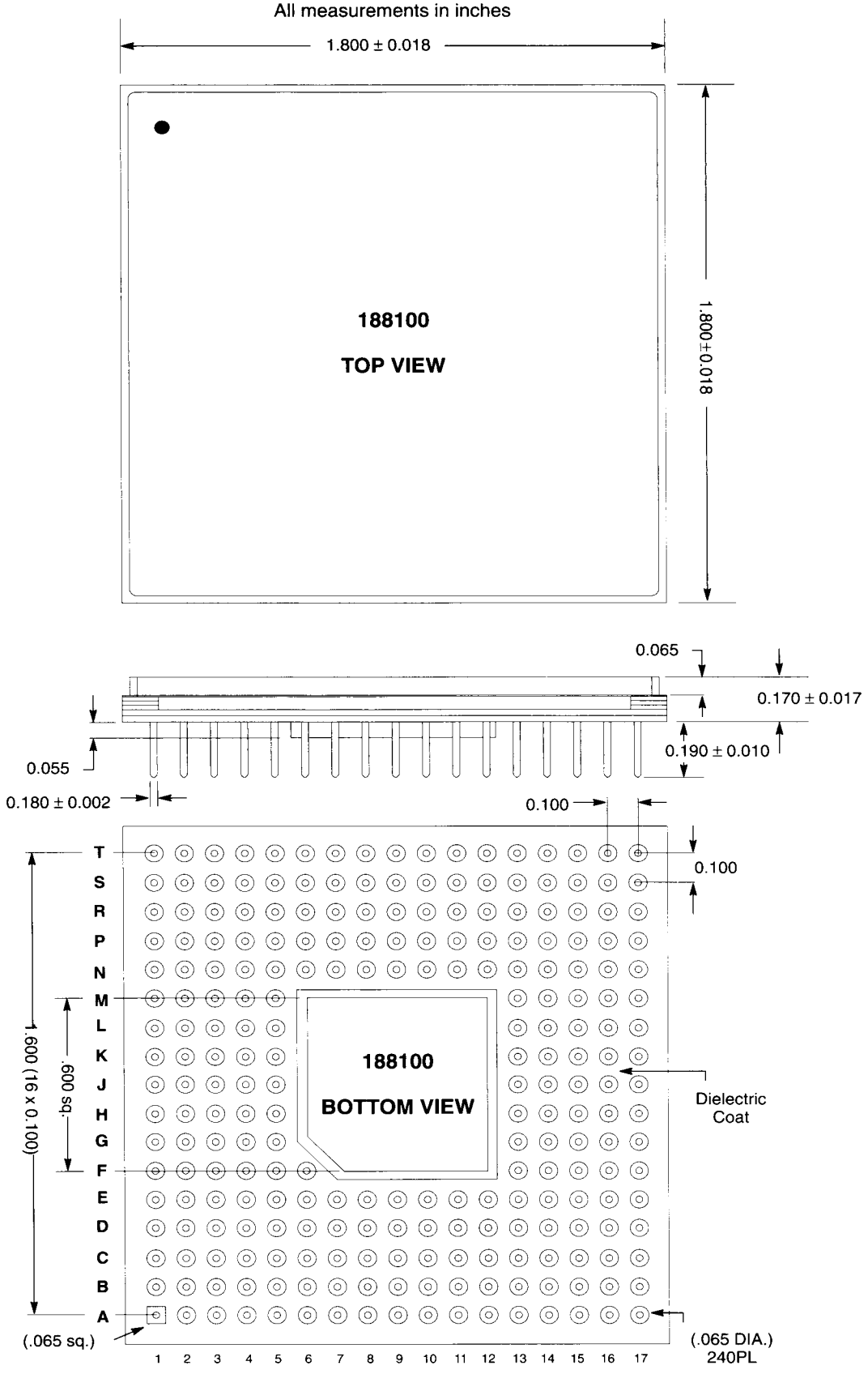
Twenty two pull-up resistors (10K), and two pull-down resistors (10K) exposed as pins.

Total pins 241 with 15 NC's, 24 V_{CC}, 34 GND, 24 pull-up/down resistors and 144 signals.

PIN GRID ARRAY (PGA)

Package Information

All measurements in inches



Pin Grid Array Package
Pin Assignment Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	V_{SS}	B15	CC3	D12	CST2	F15	CAD29
A2	V_{DD}	B16	V_{SS}	D13	CBR	F16	V_{SS}
A3	$\overline{DSS1}$	B17	V_{DD}	D14	CC2	F17	V_{DD}
A4	$\overline{DPCS}$	C1	DBA	D15	CADP0	G1	DAD25
A5	$\overline{DBB}$	C2	$\overline{DAB}$	D16	CADP1	G2	V_{SS}
A6	V_{DD}	C3	DST1	D17	CADP2	G3	DAD26
A7	DADP0	C4	DST3	E1	DC5	G4	DAD27
A8	DADP3	C5	DSMODE	E2	V_{SS}	G5	DAD28
A9	V_{SS}	C6	DC3	E3	DC6	G13	CAD28
A10	CBG	C7	DCP	E4	DC0	G14	CAD27
A11	$\overline{CSS0}$	C8	DTR1	E5	DC1	G15	CAD26
A12	V_{DD}	C9	$\overline{CPCS}$	E6	$\overline{DSS2}$	G16	V_{SS}
A13	CST3	C10	$\overline{CBB}$	E7	DC2	G17	CAD25
A14	C2ERR	C11	$\overline{CSS1}$	E8	DADP2	H1	DAD22
A15	CC4	C12	CST1	E9	DTR0	H2	DAD23
A16	V_{DD}	C13	CTM1	E10	CMCE	H3	DAD24
A17	V_{SS}	C14	CC1	E11	$\overline{CSS3}$	H4	DAD21
B1	V_{DD}	C15	CCP	E12	CST0	H5	DAD20
B2	V_{SS}	C16	CC6	E13	CBA	H13	CAD24
B3	$\overline{DSS3}$	C17	CC5	E14	CADP3	H14	CAD23
B4	DBR	D1	DERR	E15	CTM0	H15	CAD20
B5	DBG	D2	DTM1	E16	CTR1	H16	CAD21
B6	V_{SS}	D3	DST2	E17	CTR0	H17	CAD22
B7	V_{SS}	D4	$\overline{DSS0}$	F1	V_{DD}	J1	V_{SS}
B8	DTM0	D5	DMCE	F2	V_{SS}	J2	DAD18
B9	$\overline{CDLOCK}$	D6	DST0	F3	DAD30	J3	DAD19
B10	$\overline{CAB}$	D7	DC4	F4	DAD31	J4	DAD17
B11	V_{SS}	D8	DADP1	F5	DAD29	J5	DAD16
B12	V_{SS}	D9	CR/$\overline{W}$	F6	GND	J13	CAD19
B13	V_{SS}	D10	CSMODE	F13	CAD31	J14	CAD18
B14	CC0	D11	$\overline{CSS2}$	F14	CAD30	J15	CAD16
J16	CAD17	M17	V_{DD}	P14	PU	S11	V_{SS}
J17	V_{SS}	N1	DAD3	P15	PU	S12	V_{SS}
K1	DAD13	N2	DAD2	P16	N.C.	S13	PU
K2	DAD14	N3	DAD1	P17	N.C.	S14	PU
K3	DAD15	N4	DAD0	R1	N.C.	S15	PU
K4	DAD12	N5	N.C.	R2	$\overline{RESET}$	S16	V_{SS}
K5	DAD11	N6	N.C.	R3	N.C.	S17	V_{DD}
K13	CAD15	N7	N.C.	R4	N.C.	T1	V_{SS}
K14	CAD14	N8	N.C.	R5	N.C.	T2	V_{DD}
K15	CAD11	N9	CPCE	R6	N.C.	T3	CCR0
K16	CAD12	N10	PU	R7	N.C.	T4	N.C.
K17	CAD13	N11	PU	R8	CLK	T5	N.C.
L1	DAD10	N12	PU	R9	N.C.	T6	V_{DD}
L2	V_{SS}	N13	CAD0	R10	PD	T7	N.C.
L3	DAD9	N14	CAD1	R11	PU	T8	ERR
L4	DAD8	N15	CAD2	R12	PU	T9	V_{SS}
L5	DAD7	N16	V_{SS}	R13	PU	T10	PU
L13	CAD7	N17	CAD3	R14	PU	T11	PU
L14	CAD8	P1	DPCE	R15	PU	T12	V_{DD}
L15	CAD9	P2	DR1	R16	V_{DD}	T13	PU
L16	V_{SS}	P3	DR0	R17	V_{DD}	T14	PU
L17	CAD10	P4	N.C.	S1	V_{DD}	T15	PU
M1	V_{DD}	P5	N.C.	S2	V_{SS}	T16	V_{DD}
M2	V_{SS}	P6	N.C.	S3	CCR1	T17	V_{SS}
M3	DAD6	P7	N.C.	S4	N.C.		
M4	DAD5	P8	INT	S5	V_{SS}		
M5	DAD4	P9	PCE	S6	V_{SS}		
M13	CAD6	P10	PU	S7	V_{SS}		
M14	CAD4	P11	PU	S8	PLLEN		
M15	CAD5	P12	PU	S9	N.C.		
M16	V_{SS}	P13	PU	S10	PD		