9
Electrical Specifications

This chapter specifies the following electrical behavior of the 21285:

- Absolute maximum ratings
- dc specifications
- ac timing specifications

9.1 PCI Electrical Specification Conformance

The 21285 PCI pins conform to the basic set of PCI electrical specifications in the *PCI Local Bus Specification, Revision 2.1.* See that document for a complete description of the PCI I/O protocol and pin ac specifications.

9.2 Absolute Maximum Ratings

The 21285 is specified to operate at a maximum PCI frequency of 33 MHz and a **fclk_in** frequency of 66 MHz at a junction temperature (T_j) not to exceed 125°C. Table 9–1 lists the absolute maximum ratings for the 21285. These are stress ratings only; extended exposure to the maximum ratings may affect the reliability of the device.

Table 9–1 Absolute Maximum Ratings

Parameter	Minimum	Maximum
T_j	—	125°C
T_a	0°C	70°C
P_{WC}	—	2.1 W
Voltage applied to any pin	V_{ss} - 0.5 V	5.5 V
Storage temperature range	–55°C	125°C

9.3 DC Specifications

Table 9–2 defines the dc parameters met by all 21285 PCI signals under normal operating conditions.

Note: In Table 9–2, currents into the chip (chip sinking) are denoted as positive (+) current. Currents from the chip (chip sourcing) are denoted as negative (–) current.

Table 9–2 DC Parameters *(Sheet 1 of 2)*

Symbol	Parameter	Condition	Minimum	Maximum	Unit
Power Signal					
V_{dd}	Supply voltage	—	3.0	3.6	V
PCI Signals					
V_{il}	Low-level input voltage[1]	—	–0.5	0.3 V_{dd}	V
V_{ih}	High-level input voltage[1]	—	0.5 V_{dd}	V_{dd} + 0.5 V	V
V_{ol}	Low-level output voltage[2]	I_{out} = 1500 µA	—	0.1 V_{dd}	V
V_{ol5V}	Low-level output voltage[3]	I_{out} = 6 mA	—	0.55	V
V_{oh}	High-level output voltage[2]	I_{out} = –500 µA	0.9 V_{dd}	—	V
V_{oh5V}	High-level output voltage[4]	I_{out} = –2 mA	2.4	—	V
I_{il}	Low-level input leakage current[1,5]	0 < V_{in} < V_{dd}	—	±10	µA
C_{in}	Input pin capacitance	—	—	10.0	pF
C_{IDSEL}	**idsel** pin capacitance	—	—	8.0	pF
C_{clk}	**pci_clk** pin capacitance	—	5.0	12.0	pF
Non-PCI Signals					
V_{ihc}	IC input high voltage[4,5]	—	0.8 × V_{dd}	V_{dd} + 0.5	V
V_{ilc}	IC input low voltage[4,5]	—	–0.5	0.2 × V_{dd}	V
I_{ilc}[6]	Input leakage current	0 < V_{in} < V_{dd}	–10	10	µA
V_{ohc}[7]	High-level output voltage[4,5]	I_{oh} = –4 mA	2.4	—	V
V_{olc}[7]	Low-level output voltage[4,5]	I_{ol} = 4 mA	—	0.4	V
V_{ohc}[8]	High-level output voltage[4]	I_{oh} = –12 mA	2.4	—	V

DC Specifications

Table 9–2 DC Parameters *(Sheet 2 of 2)*

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{olc}[8]	Low-level output voltage	I_{ol} = 12 mA	—	0.4	V
I_{ts}	Tristate leakage current	—	—	100	µA
C_{in}	Input pin capacitance	—	—	5	pF
C_{io}	Input/output pin capacitance	—	—	12	pF
I_{dd}	Power supply current	—	—	500	mA

[1]Guarantees meeting the specification for the 5-V signaling environment.

[2]For 3.3-V signaling environment.

[3]For 5-V signaling environment.

[4]Voltage measured with respect to V_{ss}.

[5]IC-CMOS-level inputs (include IC and ICOCZ pin types).

[6]Leakage currents for **ma[12:0]** and **ba[1:0]** are -200 µA minimum and 200 µA maximum.

[7]Not including clocks.

[8]Including clocks (**MCLK**, **fclk**, and **sdclk[3:0]**).

9.4 AC Timing Specifications

The next sections describe the following specifications:

- PCI clock timing
- PCI signal timing
- PCI reset timing
- JTAG timing

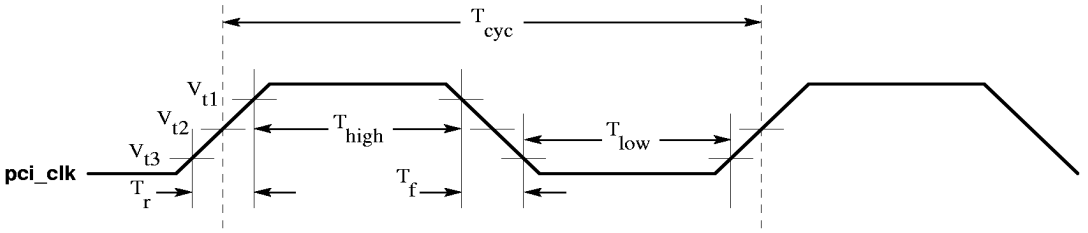
9.4.1 PCI Clock Timing Specifications

The ac specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. The output responses are delays from clock to signal. The ac specifications are defined separately for each clock domain (**pci_clk** and **fclk_in**) within the 21285.

Figure 9–1 shows the ac parameter measurements for the **pci_clk** signal, and Table 9–3 specifies **pci_clk** parameter values for clock signal ac timing. See also Figure 9–2 for a further illustration of signal timing.

AC Timing Specifications

Figure 9–1 PCI Clock Signal AC Parameter Measurement Conditions



Note:

V_{t1} – 2.0 V for 5-V clocks; 0.5 V_{cc} for 3.3-V clocks

V_{t2} – 1.5 V for 5-V clocks; 0.4 V_{cc} for 3.3-V clocks

V_{t3} – 0.8 V for 5-V clocks; 0.3 V_{cc} for 3.3-V clocks

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Table 9–3 PCI Clock Signal AC Parameters

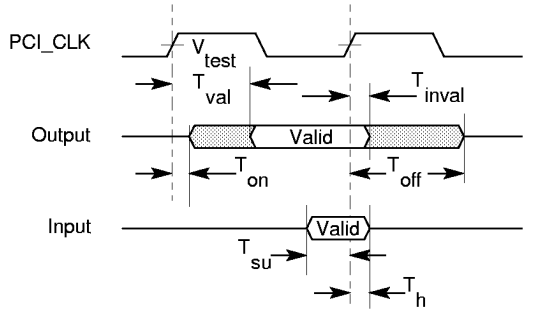
Symbol	Parameter	Minimum	Maximum	Unit
T_{cyc}	**pci_clk** cycle time	30	∞	ns
T_{high}	**pci_clk** high time	11	—	ns
T_{low}	**pci_clk** low time	11	—	ns
	pci_clk slew rate[1]	1	4	V/ns

[1] 0.2 V_{cc} to 0.6 V_{cc}.

9.4.2 PCI Signal Timing Specifications

Figure 9–2 and Table 9–4 show the PCI signal timing specifications. Table 9–5 correlates the ac parameters with the 21285 signal pins.

Figure 9–2 PCI Signal Timing Measurement Conditions



AC Timing Specifications

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Table 9–4 PCI Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{val}	**pci_clk** to signal valid delay — bused signals[1,2,3]	2	11	ns
$T_{val(ptp)}$	**pci_clk** to signal valid delay — point-to-point[1,2,3]	2	12	ns
T_{on}	Float to active delay[1,2]	2	—	ns
T_{off}	Active to float delay[1,2]	—	28	ns
T_{su}	Input setup time to **pci_clk**—bused signals[1,2,3]	7	—	ns
$T_{su(ptp)}$	Input setup time to **pci_clk**—point-to-point[1,2,3]	10, 12	—	ns
T_{h}	Input signal hold time from **pci_clk**[1,2]	0	—	ns

[1] See Figure 9–2.

[2] All PCI interface signals are referenced to **pci_clk**.

[3] Point-to-point signals are **req_l** and **gnt_l**. Bused signals are **ad, cbe_l, par, perr_l, serr_l, frame_l, irdy_l, trdy_l, devsel_l, stop,** and **idsel.**

AC Timing Specifications

Table 9–5 lists the ac parameters that are applied in Table 9–4.

Table 9–5 PCI Signal Timing AC Parameters

Name	T_{val}	$T_{val\ (ptp)}$	T_{on}, T_{off}	T_{su}, T_h	$T_{su\ (ptp)}$, T_h
ad[31:0]	y	—	y	y	—
cbe_l[3:0]	y	—	y	y	—
par	y	—	y	y	—
frame_l	y	—	y	y	—
irdy_l	y	—	y	y	—
trdy_l	y	—	y	y	—
stop	y	—	y	y	—
devsel_l	y	—	y	y	—
idsel	—	—	—	y	—
perr_l	y	—	y	y	—
serr_l	y	—	—	—	—
req_l	—	y	—	—	—
gnt_l	—	—	—	—	y
pci_irq_l	y	—	—	—	—

9.4.3 PCI Reset Timing Specifications

Table 9–6 shows the reset timing specifications for **pci_rst_l**.

Table 9–6 PCI Reset Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{rst}	**pci_rst_l** active time after power stable[1]	1	—	ms
$T_{rst—clk}$	**pci_rst_l** active time after **pci_clk** stable[1]	100	—	µs
$T_{rst—off}$	**pci_rst_l** active-to-output float delay[2]	—	40	ns
	pci_rst_l slew rate[1]	50	—	mV/ns

[1]Applies to rising (deasserting) edge only.

[2]All PCI output drivers are asynchronously floated when **pci_rst_l** is asserted (except **ad**, **cbe_l**, and **par**, which are driven to 0 if **pci_cfn** is asserted).

9.4.4 JTAG Timing Specifications

Table 9–7 shows the JTAG timing specifications.

Table 9–7 JTAG Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{jf}	**tck** frequency	0	10	MHz
T_{jht}	**tck** high time	45	—	ns
T_{jlt}	**tck** low time	45	—	ns
T_{jrt}	**tck** rise time[1]	—	10	ns
T_{jft}	**tck** fall time[2]	—	10	ns
T_{js}	**tdi**, **tms** setup time to **tck** rising edge	10	—	ns
T_{jh}	**tdi**, **tms** hold time from **tck** rising edge	25	—	ns
T_{jd}	**tdo** valid delay from **tck** falling edge[3]	—	30	ns
T_{jfd}	**tdo** float delay from **tck** falling edge	—	30	ns

[1]Measured between 0.8 V and 2.0 V.

[2]Measured between 2.0 V and 0.8 V.

[3]C_1 = 50 pF.

9.5 Memory and SA-110 Interface Timing

The timing parameters specified in this section are valid for the full range of voltage and temperature variations as stated in Sections 9.2 and 9.3. The ac specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. The output responses are delays from clock to signal. All signal timings are referenced to the rising edge of **fclk_in** unless otherwise stated.

9.5.1 SA-110, 21285, and SDRAM Clock Signal Timing Specifications

Figure 9–3 and Table 9–8 show the SA-110, 21285, and SDRAM clock signal timing specifications.

Note: The specifications listed in Table 9–8 are subject to change for pass 2.

Figure 9–3 Clock Signal AC Parameter Measurement Conditions

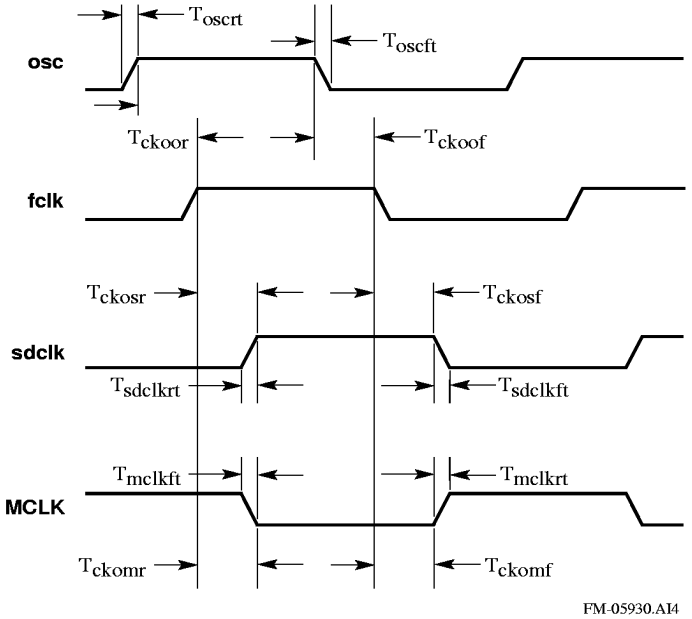


Table 9–8 SA-110, 21285, and SDRAM Clock Signal AC Parameters

Name	Parameter	Minimum	Maximum	Unit
T_{ckoor}	**osc** rising **fclk** rising	1.9	4.4	ns
T_{ckoof}	**osc** falling **fclk** falling	1.9	4.0	ns
T_{oscrt}	**osc** rise time	.5	2.0	ns
T_{oscft}	**osc** fall time	.5	2.0	ns
T_{ckoi}	**fclk** to **fclk_in** delay[1]	—	—	ns
T_{ckomf}	**fclk** to **MCLK** delay - **fclk** rising	1.9	3.8	ns
T_{ckomr}	**fclk** to **MCLK** delay - **fclk** falling	2.1	4.9	ns
T_{mclkrt}	**MCLK** rise time	.5	2.0	ns
T_{mclkft}	**MCLK** fall time	.5	2.0	ns
T_{ckosr}	**fclk** to **sdclk** delay - **fclk** rising[2]	1.9	3.9	ns
T_{ckosf}	**fclk** to **sdclk** delay - **fclk** falling[2]	1.9	4.3	ns
$T_{sdclkrt}$	**sdclk** rise time	.5	1.0	ns
$T_{sdclkft}$	**sdclk** fall time	.5	1.0	ns
T_{skew1}	Skew between rising edges on any two of **sdclk[3:0]**	—	—	ns
T_{skew2}	Skew between **MCLK** falling and any of **sdclk[3:0]** rising	—	—	ns

[1]This delay is not specified. It is imposed by etch delays in the module design. In the module design, the capacitive load and etch length on the following nets should be matched: 21285 **fclk** output to 21285 **fclk_in**; 21285 **MCLK** output to SA-110 MCLK pin; 21285 **sdclk[3:0]** outputs to SDRAM CLK pin.

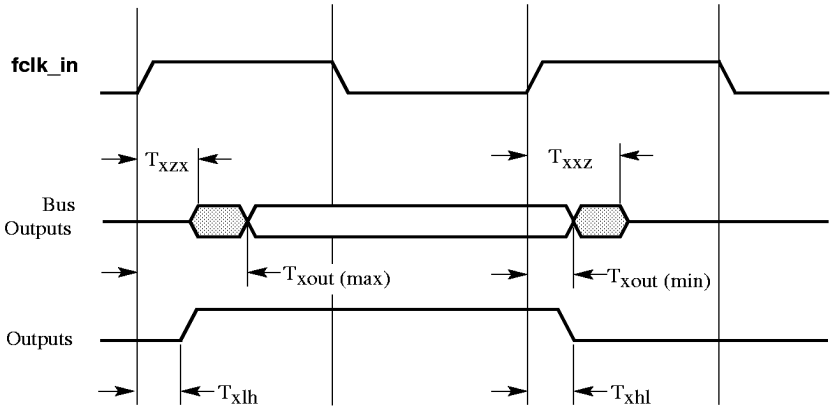
[2]Any of **sdclk[3:0]**.

9.5.2 SA-110, 21285, and SDRAM Interface Timing Specifications

Figures 9–4 and 9–5 with Table 9–9 show the memory and SA-110 interface timing specifications.

Note: The specifications listed in Table 9–9 are subject to change for pass 2.

Figure 9–4 Interface Timing Measurement Conditions



Timing Symbol(s)	Corresponding Parameter Value
T_{xzx}	T_{dzx}, T_{pzx}, T_{azx}, T_{dqmzx}, T_{mazx}, T_{cmdzx}, T_{cszx}
T_{xxz}	T_{dxz}, T_{pxz}, T_{axz}, T_{dqmxz}, T_{maxz}, T_{cmdxz}, T_{cszx}
T_{xout} (max), T_{xout} (min)	T_{dout}, T_{pout}, T_{aout}, T_{dqmout}, T_{maout}, T_{cmdout}, T_{csout}
T_{xlh}	T_{xwlh}, T_{dwlh}, T_{rcslh}, T_{rdlh}, T_{wrlh}, T_{xcslh}, T_{abelh}, T_{dbelh}
T_{xhl}	T_{xwhl}, T_{dwhl}, T_{rcshl}, T_{rdhl}, T_{wrhl}, T_{abehl}, T_{abehl}, T_{dbehl}

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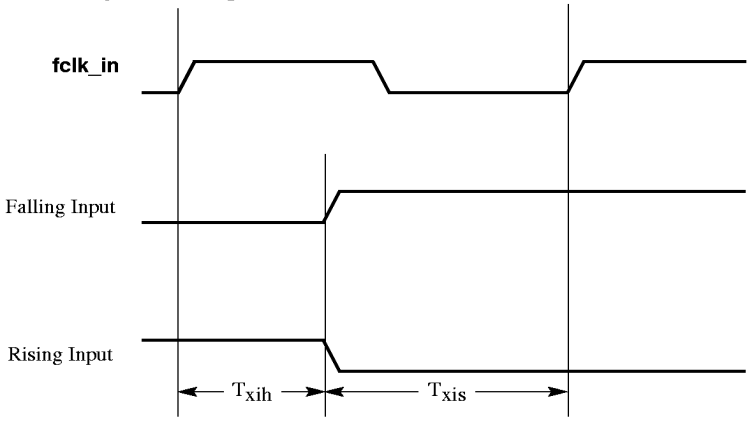
Figure 9–5 Input Timing Measurement Conditions



Timing Symbol(s)	Corresponding Parameter Value
T_{xih}	T_{dih}, T_{mrih}, T_{loih}, T_{rwih}, T_{clih}
T_{xis}	T_{dis}, T_{mris}, T_{lois}, T_{rwis}, T_{clis}

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Table 9–9 Memory and SA-110 AC Parameters *(Sheet 1 of 3)*

Name	Parameter	Minimum	Maximum	Unit
T_{dis}	T_{dis} data-in setup[1]	0	—	ns
T_{dih}	T_{dih} data-in hold[1]	1.6	—	ns
T_{pis}	T_{pis} parity-in setup	4.7	—	ns
T_{pih}	T_{pih} parity-in hold	1.6	—	ns
T_{dout}	Data-out delay	4.9	11.4	ns
T_{pouta}	Asynchronous parity-out delay (SA-110 write)	3.3	10.5	ns
T_{pouts}	Synchronous parity-out delay (21285 write)	5.7	17.0	ns
T_{dzx}	Data turn-on time	4.1	11.2	ns
T_{dxz}	Data turn-off time	4.1	11.2	ns
T_{pzx}	Parity turn-on time	4.0	11.1	ns
T_{pxz}	Parity turn-off time	4.0	11.1	ns

Memory and SA-110 Interface Timing

Table 9–9 Memory and SA-110 AC Parameters *(Sheet 2 of 3)*

Name	Parameter	Minimum	Maximum	Unit
T_{ais}	Address input setup	1.4	—	ns
T_{aih}	Address input hold	1.0	—	ns
T_{aout}	Address output delay (includes **rom_oe_l**, **rom_we_l**)	4.4	11.5	ns
T_{azx}	Address turn-on time	4.5	13.0	ns
T_{axz}	Address turn-off time	4.5	13.0	ns
T_{dqma}	**dqm[3:0]** maximum output delay during SA-110 write, timed from SA-110 address in	—	9.1	ns
T_{dqmh}	**dqm[3:0]** minimum output hold during SA-110 write, timed from rising **fclk_in**	4.7	—	ns
T_{dqms}	**dqm[3:0]** output delay during 21285 write	4.6	10.6	ns
T_{maout}	**ma**, **ba** output delay	5.0	10.8	ns
T_{cmdout}	**cmd[2:0]** output delay	5.2	11.4	ns
T_{csout}	**cs_l[3:0]** output delay	5.1	11.4	ns
T_{xwhl}	**xd_wren_l** assertion delay	5.3	10.5	ns
T_{xwlh}	**xd_wren_l** negation delay	5.1	10.9	ns
T_{dwhl}	**d_wren_l** assertion delay	4.5	9.3	ns
T_{dwlh}	**d_wren_l** negation delay	4.7	10.0	ns
T_{rcshl}	**rom_ce_l** assertion delay	4.7	9.6	ns
T_{rcslh}	**rom_ce_l** negation delay	4.9	10.2	ns
T_{rdhl}	**xrd_l** assertion delay	5.4	10.5	ns
T_{rdlh}	**xrd_l** negation delay	5.1	10.9	ns
T_{wrhl}	**xwr_l** assertion delay	5.4	10.6	ns
T_{wrlh}	**xwr_l** negation delay	5.1	11.0	ns
T_{xcshl}	**xcs_l** assertion delay[2]	4.3	8.9	ns
T_{xcslh}	**xcs_l** negation delay[2]	4.3	9.6	ns
T_{abehl}	**ABE** negation delay	5.2	10.3	ns
T_{abelh}	**ABE** assertion delay	5.0	10.4	ns

Table 9–9 Memory and SA-110 AC Parameters *(Sheet 3 of 3)*

Name	Parameter	Minimum	Maximum	Unit
T_{dbehl}	**DBE** negation delay	4.4	9.1	ns
T_{dbelh}	**DBE** assertion delay	4.5	9.6	ns
T_{mris}	**nMREQ** input setup	1.4	—	ns
T_{mrih}	**nMREQ** input hold	0.7	—	ns
T_{lois}	**LOCK** input setup	0.9	—	ns
T_{loih}	**LOCK** input hold	0.6	—	ns
T_{rwis}	**nRW** input setup	0.3	—	ns
T_{rwih}	**nRW** input hold	1.6	—	ns
T_{clis}	**CLF** input setup	1.0	—	ns
T_{clih}	**CLF** input hold	0.6	—	ns

[1]For SA-110 writes to 21285, 21285 reads of SDRAM, and 21285 reads of ROM.

[2]For **xcs** signals that are configured as outputs.