FBGA User's Guide

Version 4.2

July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **22247** Revision **J** Amendment **0** Issue Date **November I, 2002**

FBGA User's Guide

November 1, 2002 Version 4.2

AMD

Chapter 1: Introduction

There is a trend in the electron industry to miniaturize. From tower PCs to lap-tops to PocketPCs, from giant cell phones to pager size handsets, the demand for smaller feature rich electronic devices will continue for years to come.

The trend for Chip Scale Packages (CSP) have grown tremendously since their introduction. Applications such as cell phones, home entertainments, automotive engine controllers and networking equipments all have adopted CSP packages into their systems. To address the needs of different applications such as small package size, reliability or migration compatibility, AMD offers three families of CSP: *Fine-Pitch Ball Grid Array (FBGA), Fortified-BGA and Stacked-MCM*

Table 1.1: Package Highlights

Package Highlights	Benefits	Target Applications
FBGA Package		
Small Package	Ideal for space constraint PCB designs	Ideal for application with space constraints. Portable application such as mobile phones, camcorders and PDAs would benefit most
1.2mm Max package height	Ideal for low-provide application	
BT-Resin	Superior board level reliability	
Fortified-BGA		
Uniform 11x13mm Package size	Simple and smooth migration and compatibility across densities up to 256Mb	Removes concerns for Automotive, Networking, Telecom and other applications that demand the highest board level reliabilities
1.0mm Ball Pitch	Allows for more relax PCB design rules	
0.6mm Ball Diameter	Improves board level reliabilities	
Stacked-MCM		
Small Package size	Idea for space constrain PCB designs	Enabling applications with increase memory for higher performance without increase in board space. Ideally suited for Camcorders, mobile phones, PDAs and other wireless applications
1.4mm Max Height	Idea for low-profile applications	
Combines Flash and SRAM	Increase memory capacity with no increase in board spaces	

Table 1.1: Package Highlights

Available Combinations: 128Mb Flash + Flash 16Mb Flash + 2Mb SRAM 16Mb Flash + 4Mb SRAM 32Mb Flash + 4Mb SRAM 32Mb Flash + 8Mb SRAM 64Mb Flash + 8Mb SRAM 64Mb Flash + 16Mb SRAM	Flexible memory combinations for number design possibilities and opportunities	

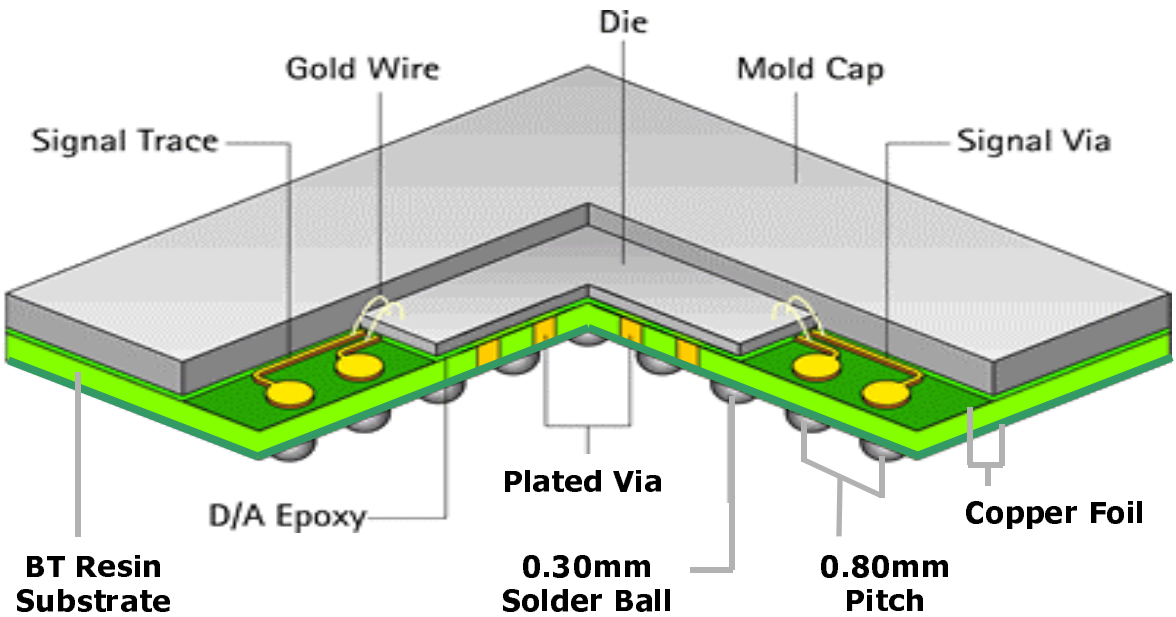
Chapter 2: AMD Fine-Pitch Ball Grid Array (FBGA)

The AMD FBGA package family offers Flash memory designers significant reduction in board real estate over Thin Small Outline Packages (TSOPs). In addition AMD FBGA packages provide many advantages over other Flash memory supplies' chip scale packages, sush as alternatives robust board level reliability and smooth pinout migrations. The packages are available for several popular 1.8-volt and 3.0-volt Flash memory densities. The FBGA packages are constructed similar to conventional IC packages and are an extension of the proven BGA technologies. For PCB assembly, existing equipment and proven manufacturing processes may be used.

Package Construction

AMD FBGA is constructed on rigid BT-Resin substrates. The die is mounted on the substrate and the leads are bonded using gold wires. The device is encapsulated in plastic and solder balls are attached to the bottom of the substrate.

Figure 2-1. FBGA Construction



Note: Package Height = 1.2 mm max.

The Impact of Die Size Changes on FBGA Package Size

There are many costs associated with the manufacturing of semiconductor devices: die cost, assembly cost and testing costs just to name a few. The die cost typically has the most impact on the total manufacturing cost. In order to drive down the cost of the final product, semiconductor manufacturers

will stride to reduce die sizes. AMD's FBGA packages allow smaller, lower cost die to be placed in the same package without affecting package dimensions or requiring PC board redesigns.

The Impact of Die Size Changes on FBGA Package Size

The minimum distance between balls on the FBGA, the ball pitch, great affects an OEM's PC board technology and system routing complexity. Device with ball pitches of 0.8mm can be easily be routed with today's widely used and cost effect PC board technology (FR4 with 0.005 inch lines and spaces).

FBGA Package Pinouts

All pinouts are shown top view, with balls facing down.

Figure 2-2. 48-Ball Ball (4 Mb to 32Mb, x8/x16, Low Voltage)

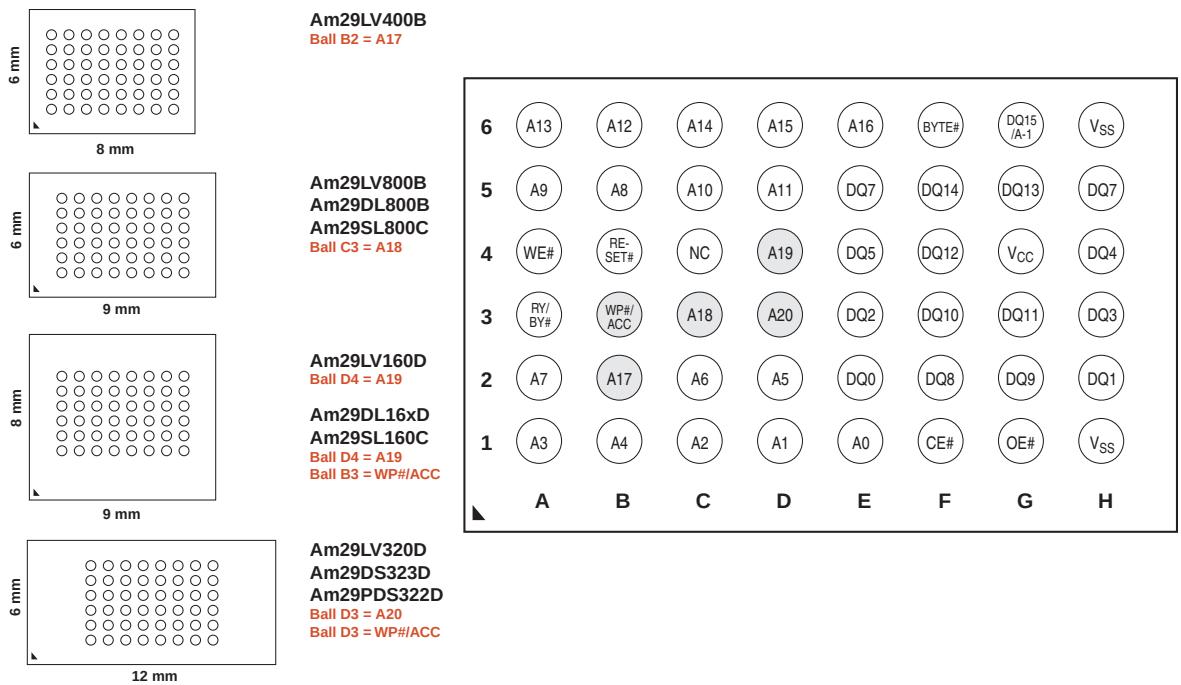
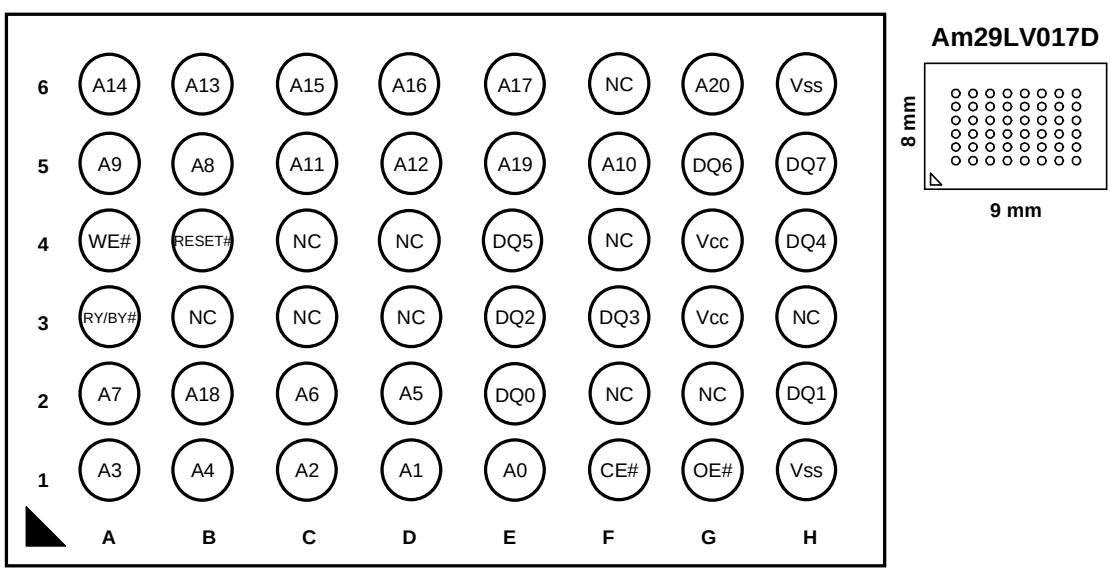


Figure 2-3. 48-Ball (16 Mb, x8, Low Voltage)



All pinouts in this chapter are shown top view, balls facing down.

Figure 2-4. 63-Ball (32 Mb to 64 Mb, x8/x16, Low Voltage)

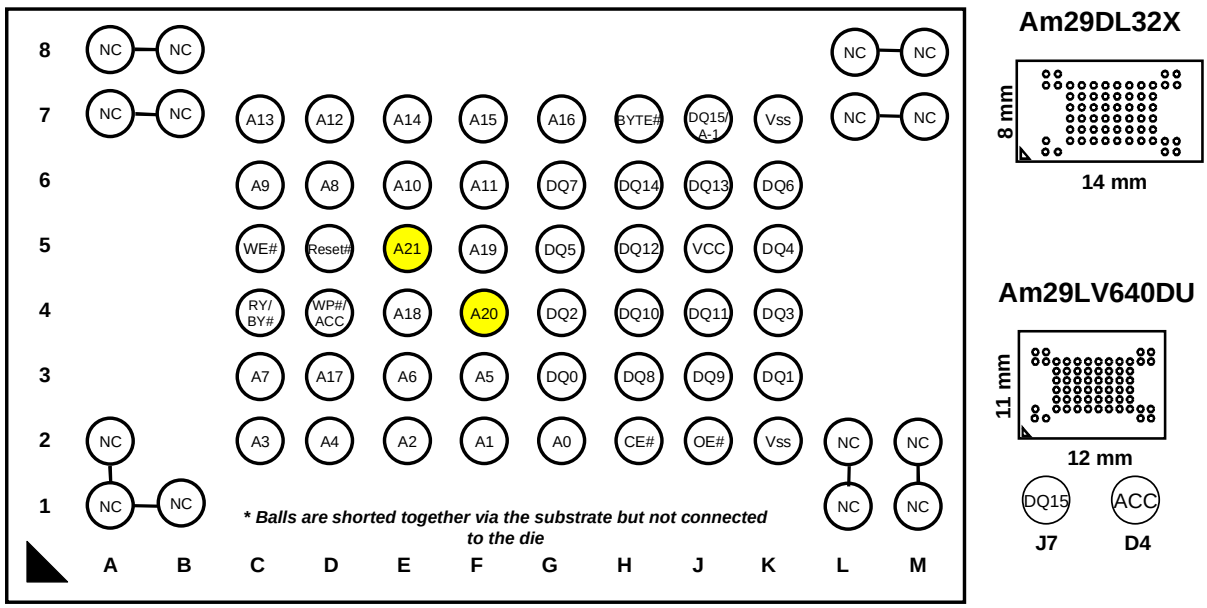
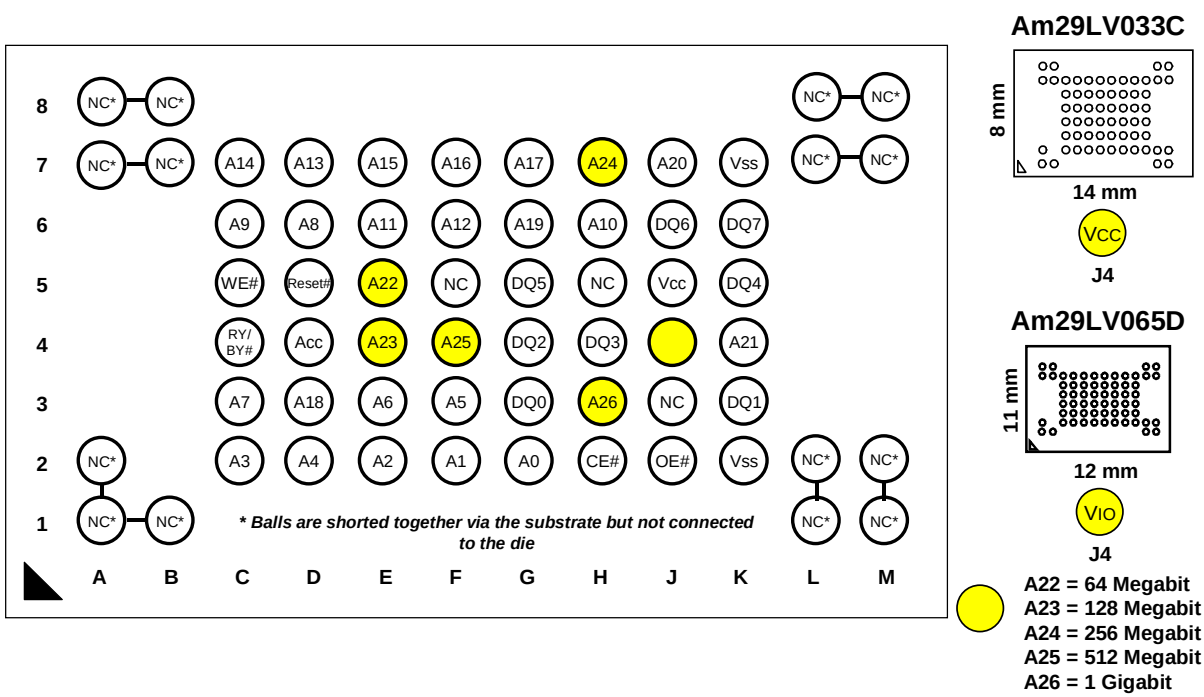


Figure 2-5. 63-Ball (32 Mb to 1 Gb, x8, Low Voltage)



All pinouts in this chapter are shown top view, balls facing down.

Figure 2-6. 84-Ball (32 Mb to 4 Gb, x16/x32 Low Voltage)

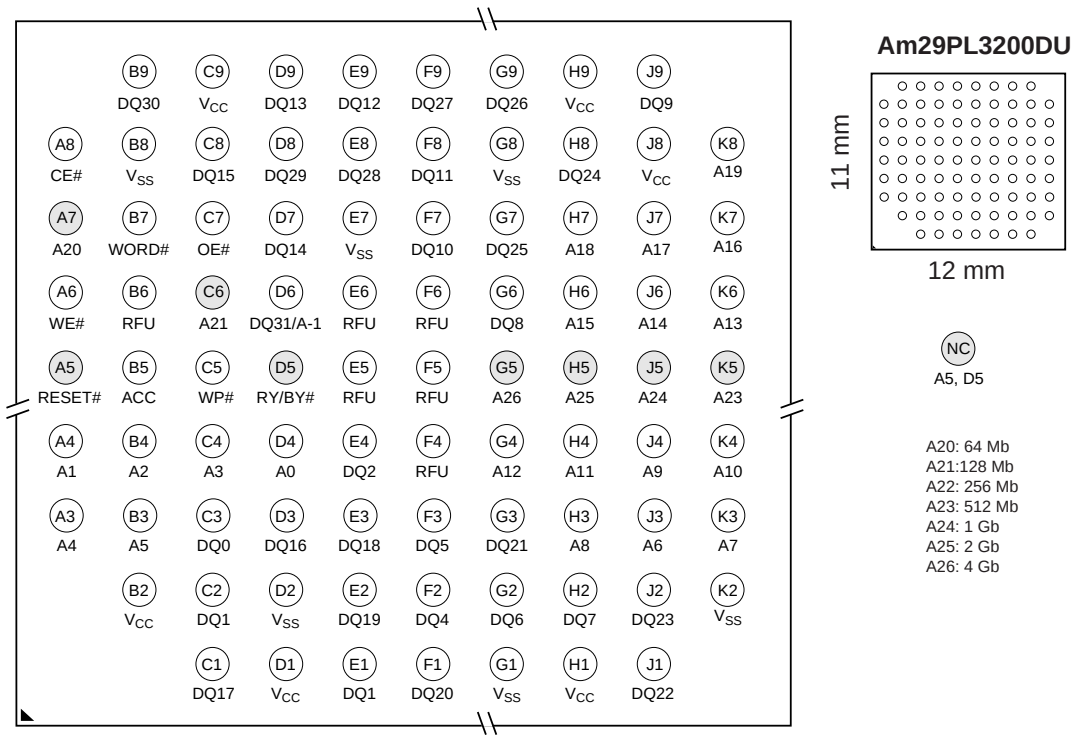
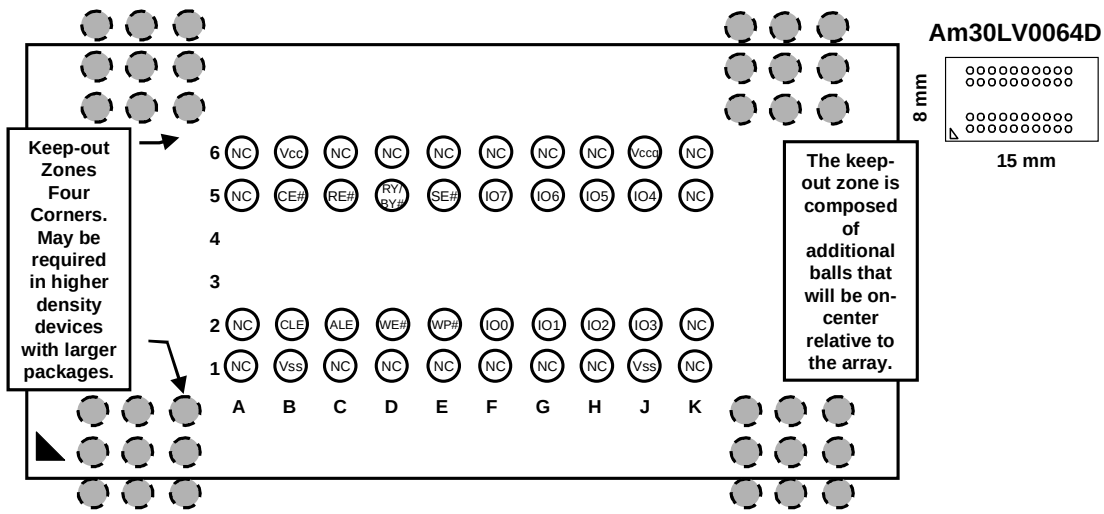


Figure 2-7. 84-Ball (32 Mb to 128 Mb, x16/x3240-Ball (64 Mb, x8, UltraNAND Only)



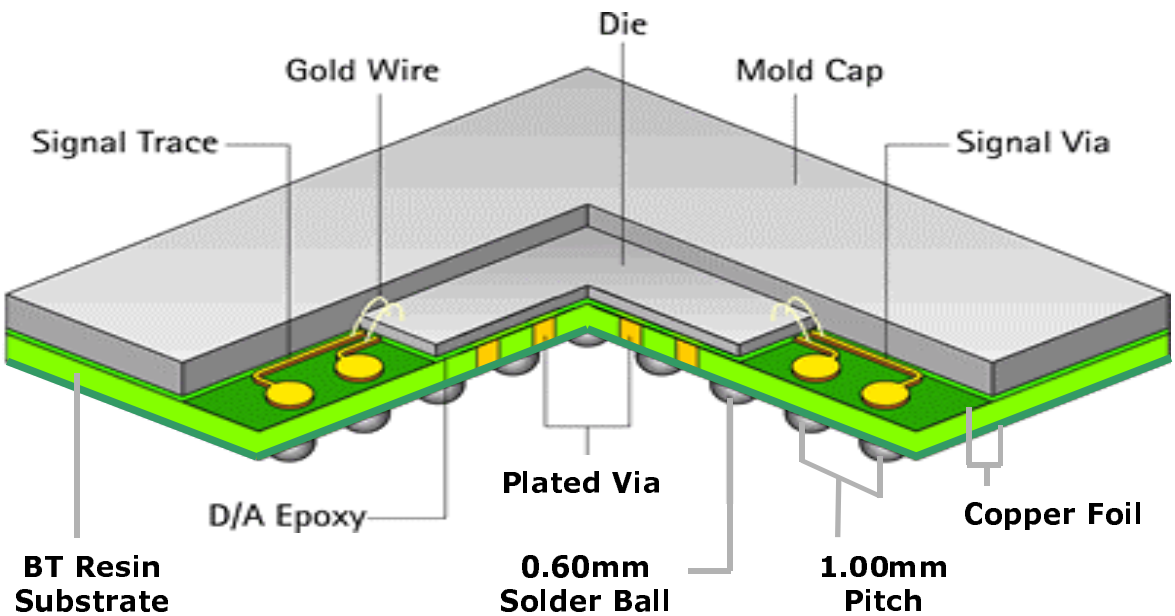
Chapter 3: AMD Fortified-BGA

New performance driven applications continues to demand high board level reliability packages from Flash memories. In addition, as PCB designs become increasingly complex, assembly-friendly package becomes more desirable. AMD's Fortified-BGA for the Flash memory combines both superior reliability beyond the standard requirements and ease-of-use in one single package. It is ideal for telecom, networking, automotive and avionics applications.

Package Construction

AMD's Fortified-BGA is offer in a single easy to use 13x11mm x 1.4mm Ht. Package size, with 0.6mm solder ball diameter at 1.0mm ball pitch. Designed around AMD's already robust FBGA (0.8mm ball pitch), the Fortified-BGA uses industry proven BT-Substrate to lower the CTE mismatch between the substrate and the PCB.

Figure 3-1. Fortified-BGA Construction



Note: Package Height = 1.4mm Max.

Effects of Solder Ball Diameter

It is well known in the industry that solder ball diameter has a direct affect on solder joint reliability during temperature cycling. Lager solder balls typically yield higher standoff heights after board assembly. The importance of higher standoff is easiest explained through CTE mismatch. As describe in many papers, higher standoff typically yields higher solder joint reliability during temperature cycling. AMD's Fortified-BGA currently has the largest solder ball size (0.6mm Diameters) of any

BGA package for Flash memory. As a result, AMD's Fortified-BGA offers superior board level reliability, during Temperature Cycling, compared to other competitor's BGA packages. When compared to a competitor's 10x13mm BGA, the 64-Ball (8x8 matrix) Fortified-BGA is expected to have a higher relative life by a factor of 4.3X, and the 80-Ball (8x10 matrix) Fortified-BGA is expected be 4.6X higher relative life.

Fortified-BGA Migration and Transition

AMD's Fortified-BGA has taken AMD's tradition of simple pinout migration to higher density one step further. It virtually allows migration between densities without new board designs.

Fortified-BGA's 11x13mm package size is designed to host any Flash density up to 256Mb. This concept greatly lowers cost for customers. By anticipating future density needs, customers can virtually have one board design. Furthermore, this "one-package-fits-all" concept can also help trim equipment cost. The same socket, test boards, handlers, traces etc. are now interchangeable between densities. Thereby increases the useful life of equipments.

AMD's Fortified-BGA takes full advantage of the real estate underneath the package. With 1.0mm ball pitch, PCB design rules can be more relaxed. At any drill or pad size, 1.0mm pitch provides more clearance for traces and spaces. For example, either 5mil or 7mil trace and space design rules can by used. More clearance also allows for larger via capabilities, ideal for multi-layer PCB designs.

Board assembly also benefits from 1.0mm ball pitch. AMD's Fortified-BGA is aligned with many FPGAs and Micro-Controller in terms of ball pitch. This allows for less expensive PCB technology to be used.

AMD's Fortified-BGA, in essence, simplifies customers' transition to BGA packages. It is a Low-Cost, highly reliable CSP solution to TSOP and other traditional leaded packages.

Fortified-BGA (FBGA) Pinouts

All pinouts are shown top view, with balls facing down.

Figure 3-2. 64-Ball Fortified-BGA

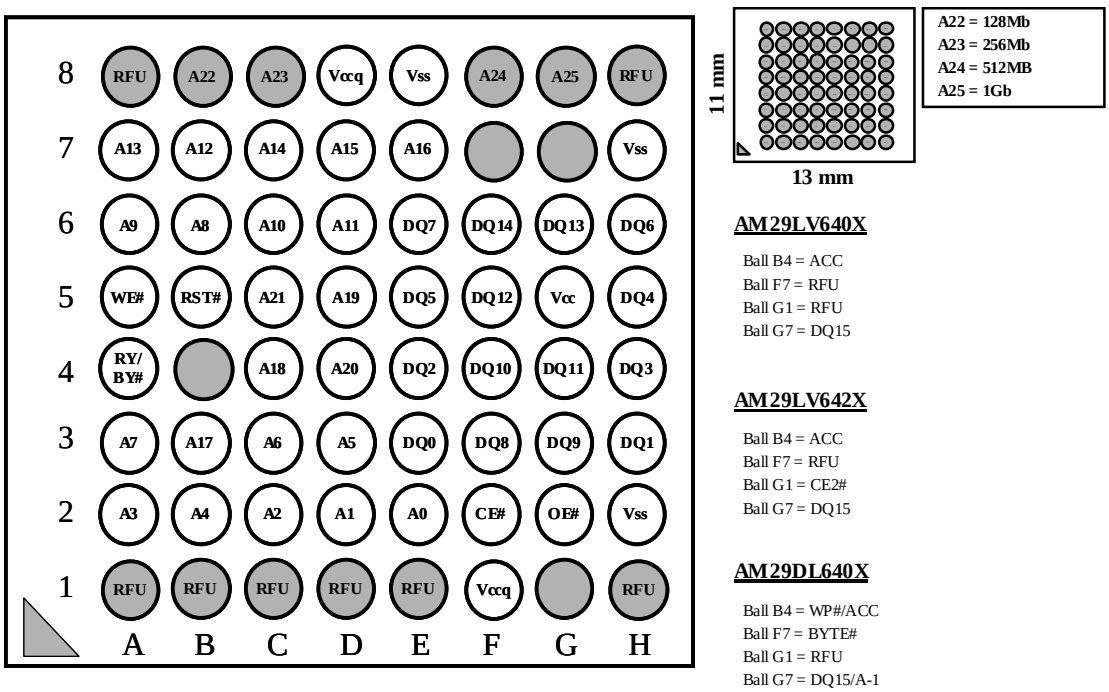
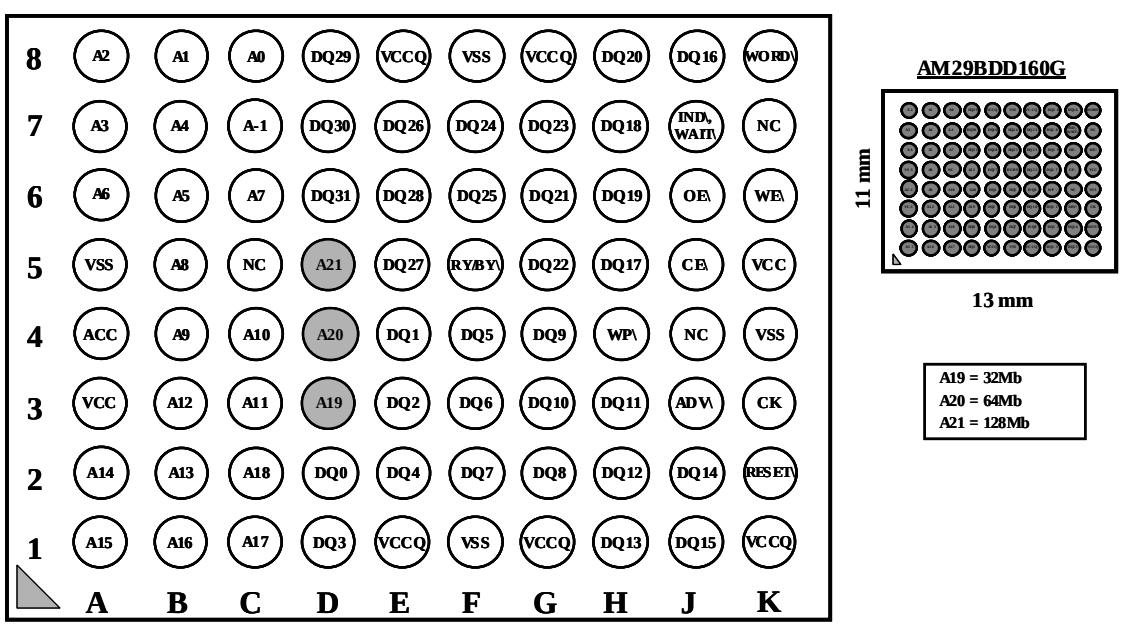


Figure 3-3. 80-Ball Fortified-BGA



Chapter 4: AMD Multi-Chip Packaging

In portable consumer product segment such as Cell phones, PDAs, digital cameras and audio players there are demands to increase features and functionalities as well as for smaller, thinner product size. In order to meet these demands, AMD launched a line of MCP (Multi-Chip Package) products.

Through system integration and PCB optimization, MCP enhances system design in numerous ways such as reduce PCB size, lower PCB cost, reduce components, lighter weight, smaller system, increase features and customer flexibility.

Package Construction

Figure 4-1. 2-Die MCP Construction

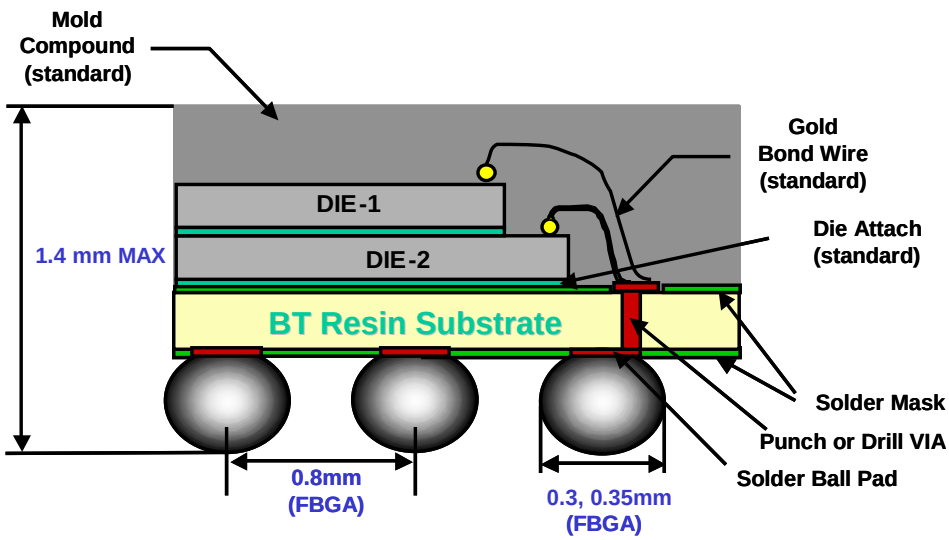
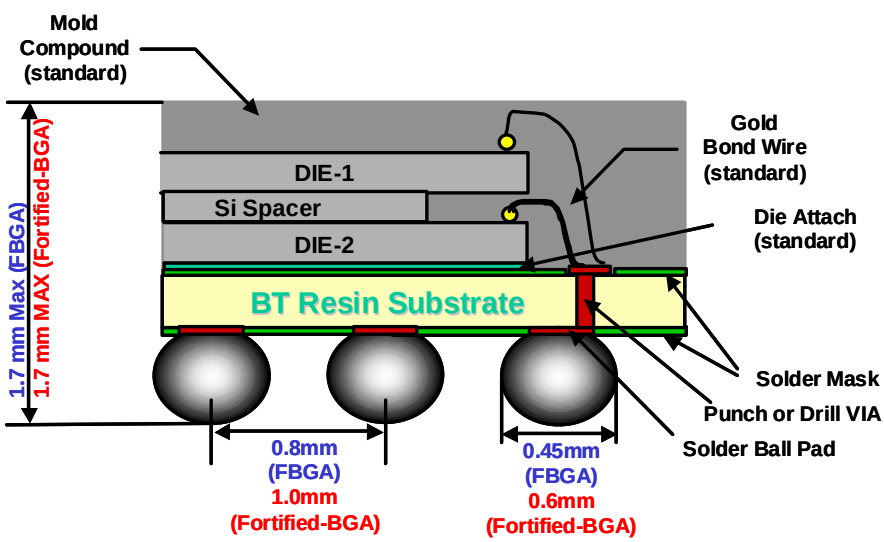


Figure 4-2. Same-Die Stack (SDS) MCP Construction



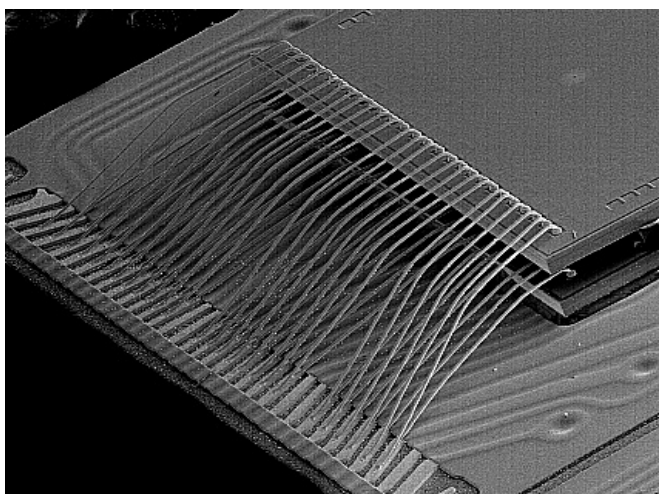
System integration and space savings

MCPs are gaining momentum in the industry as a system integration solution. In the cellular phone market, Flash and SRAM MCP combinations have become very popular. It stacks one die on top of the other on a rigid BT-substrate. Both chips are wire- bonded to the top of the substrate and overmolded with encapsulant, solder balls on the bottom of the package. This technology allows companies to immediately take advantage space savings, with either smaller or more feature rich products.

Two die stacking is typically use if the top die size is small enough not to cover the bond pad of the bottom die. However, if both dies are similar in size Same-Die-Stacking (SDS) must be use. SDS uses a spacer-die, between the top die and the bottom, to allow for addiquiet wire bonding space of the bottom die. SDS provides powerful flexibility to system integration. With SDS, not only can components of two different application be integrate in single package, same components can also be integrated to added feature or higher densities, such as Flash+Flash.

Figure 4-3. 2-Die Stack (Flash+SRAM) MCP

Figure 4-4. Same-Die-Stack (SDS) MCP



MCP Package Pinouts

All pinouts are shown top view, with balls facing down.

Figure 4-5. Am29DL16XD and 4Mb (x8/x16) SRAM MCP Pinout

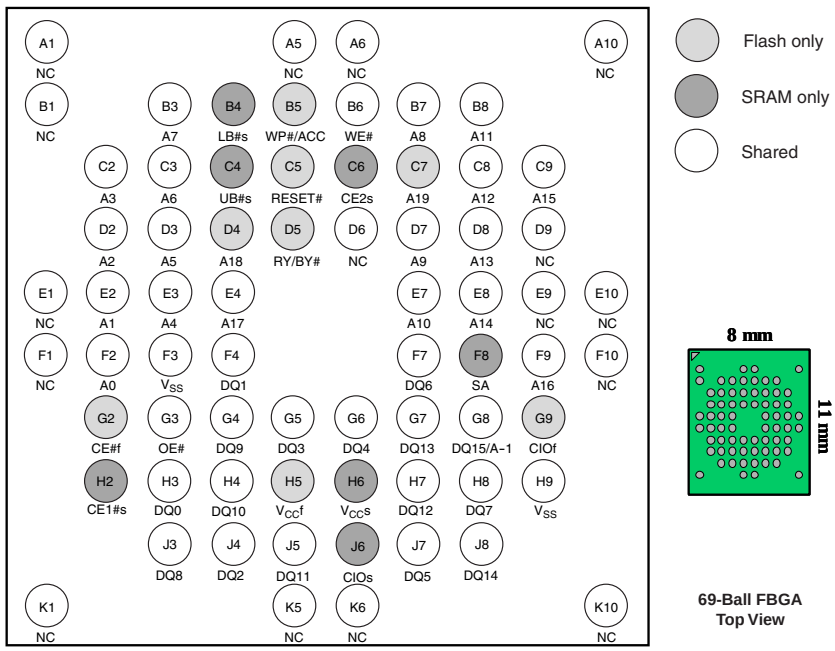


Figure 4-6. Am29DL32XD and 4Mb (x8/x16) SRAM MCP Pinout

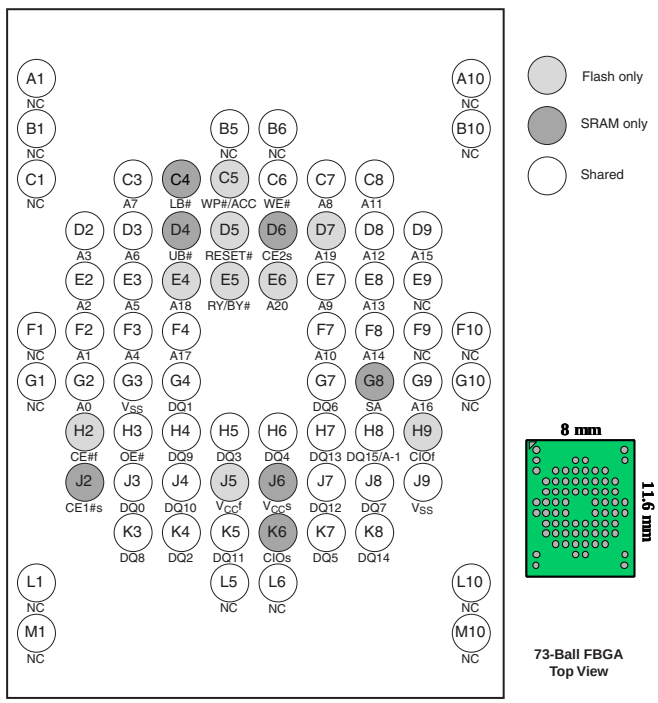


Figure 4-7. Am29DL32XD and 8Mb (x8/x16) SRAM MCP Pinout

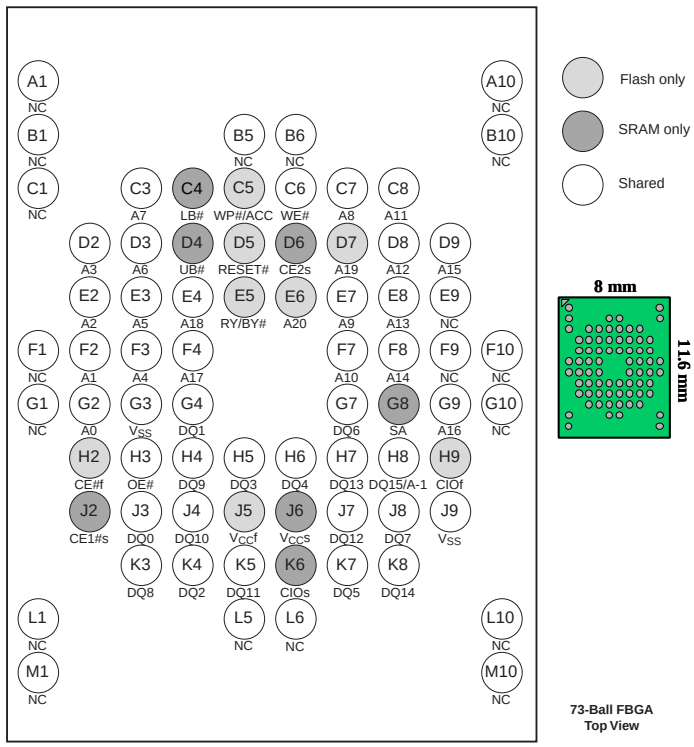
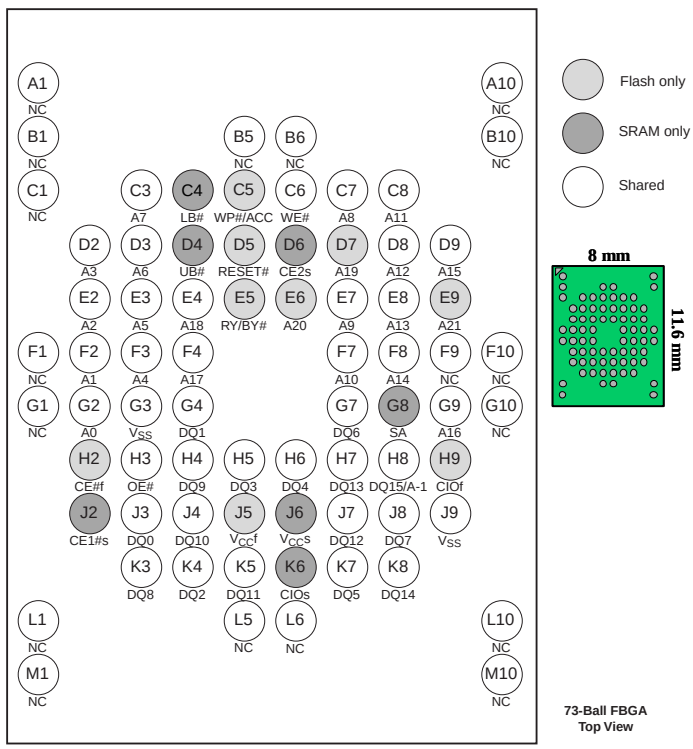


Figure 4-8. Am29DL64XD and 8Mb (x8/x16) SRAM MCP Pinout



Chapter 5: Daisy Chains

Daisy Chains are primarily requested by OEMs to perform assembly evaluations. Prior to production, an OEM will generally solder daisy chain samples on to a daisy chain PCB and perform Open/Short testing to check for misalignments. This test will help OEMs characterize its assembly process and equipment prior to full production. Daisy Chains are also used in Second Level Solder-Joint Board Reliability studies. The daisy chain samples are assembled onto the matching PCB and subjected to temperature cycling in an oven. Board Level Reliability tests are tools to help predict and measure the expected life of a packages. For more in depth information on Second Level Solder-Joint Board Reliability, please refer to "Reliability Evaluation Of Chip Scale Packages" by Ranjit Gannamani, Viswanath Valluri, Sidharth, and MeiLu Zhang (see "Article Reprints"). For more in-depth information on Daisy Chains please refer to the "Daisy Chain Samples Application Note". Both are listed in the Appendices.

Figure 5-1. FBGA 16 Mbit Daisy Chain Schematic (Top View)

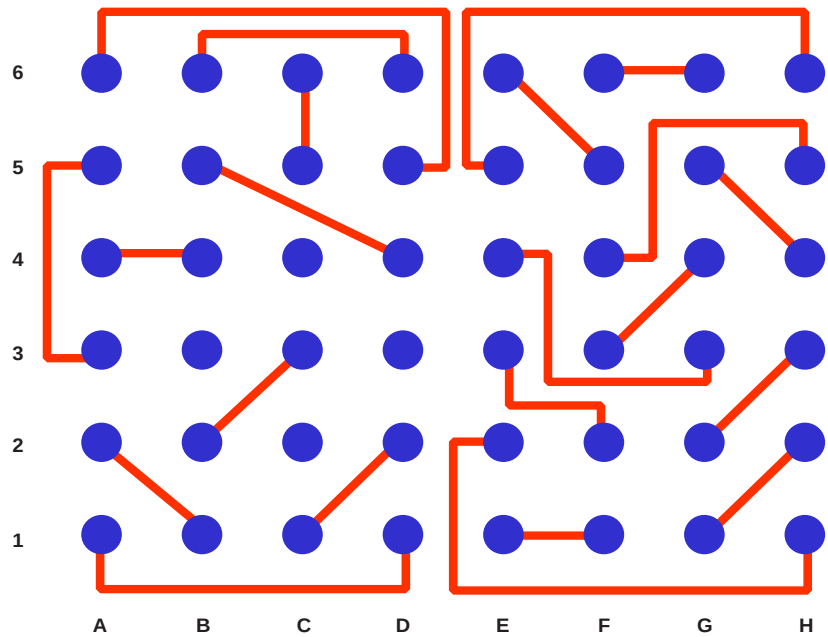
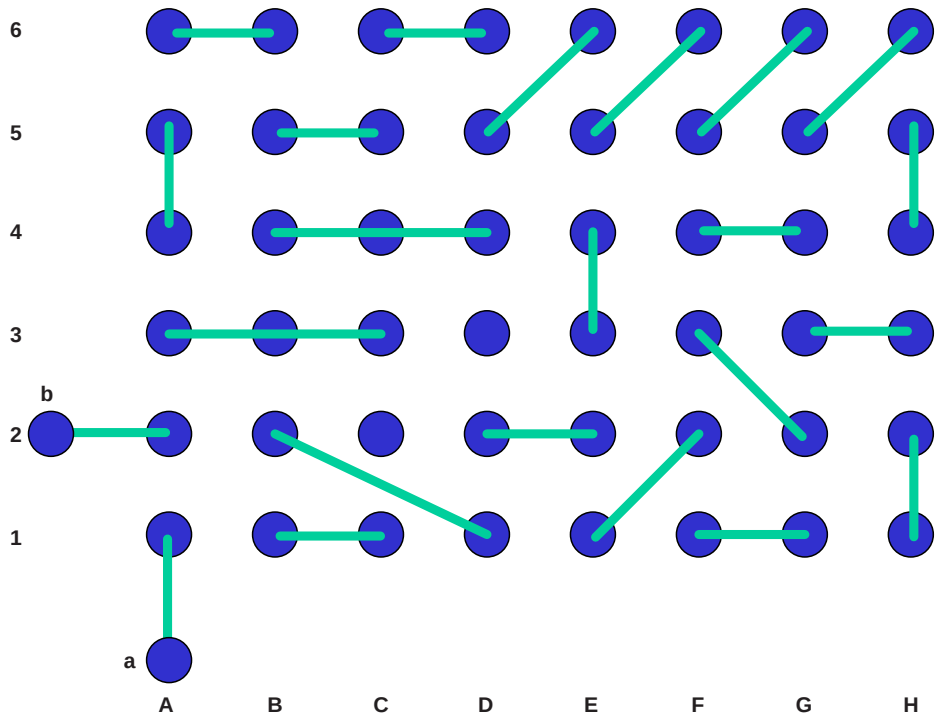


Figure 5-2. FBGA 16 Mbit Board Layout (Top View)



a and b are the input and output of the network for this device.

Figure 5-3. FBGA 32 Mbit Daisy Chain Schematic (Top View)

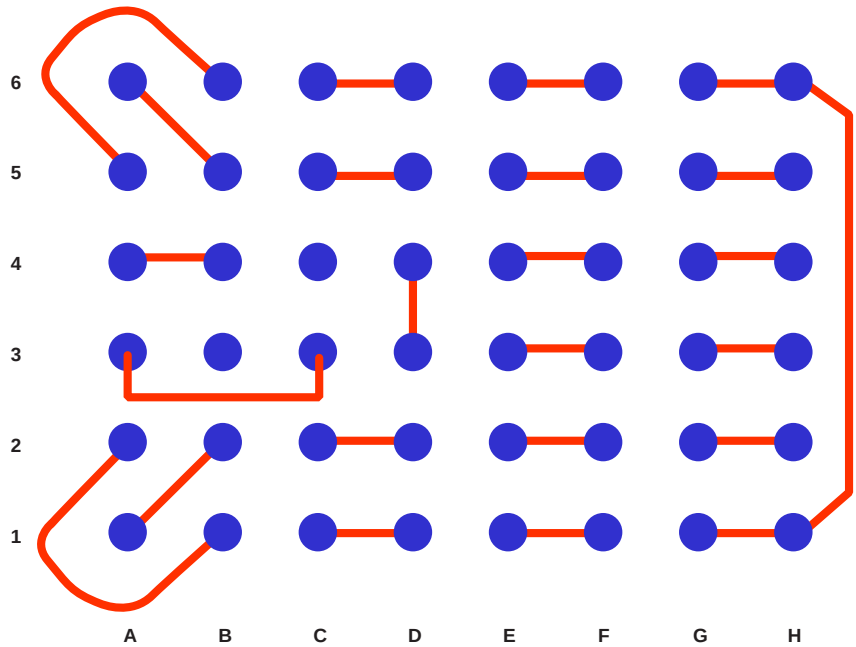
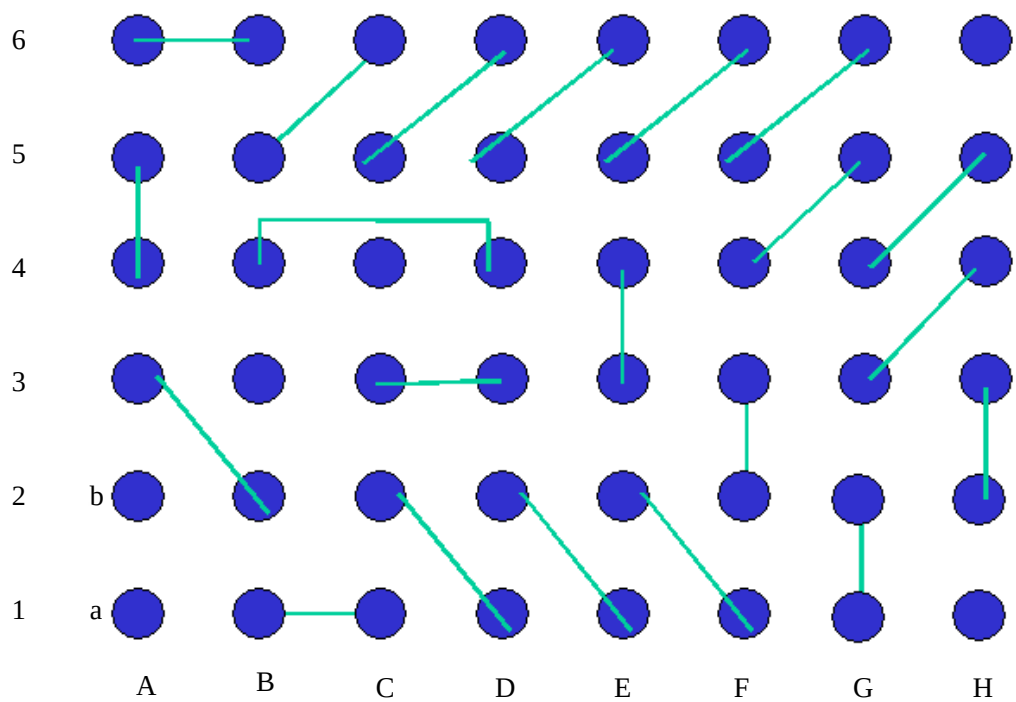


Figure 5-4. FBGA 32 Megabit Board Layout (Top View)



Notes:

1. a, b are the input and output of the network for the device.
2. c, d are the input and output of a separate network for the support balls.

Figure 5-5. FBGA 64 Mbit Daisy Chain Schematic (Top View)

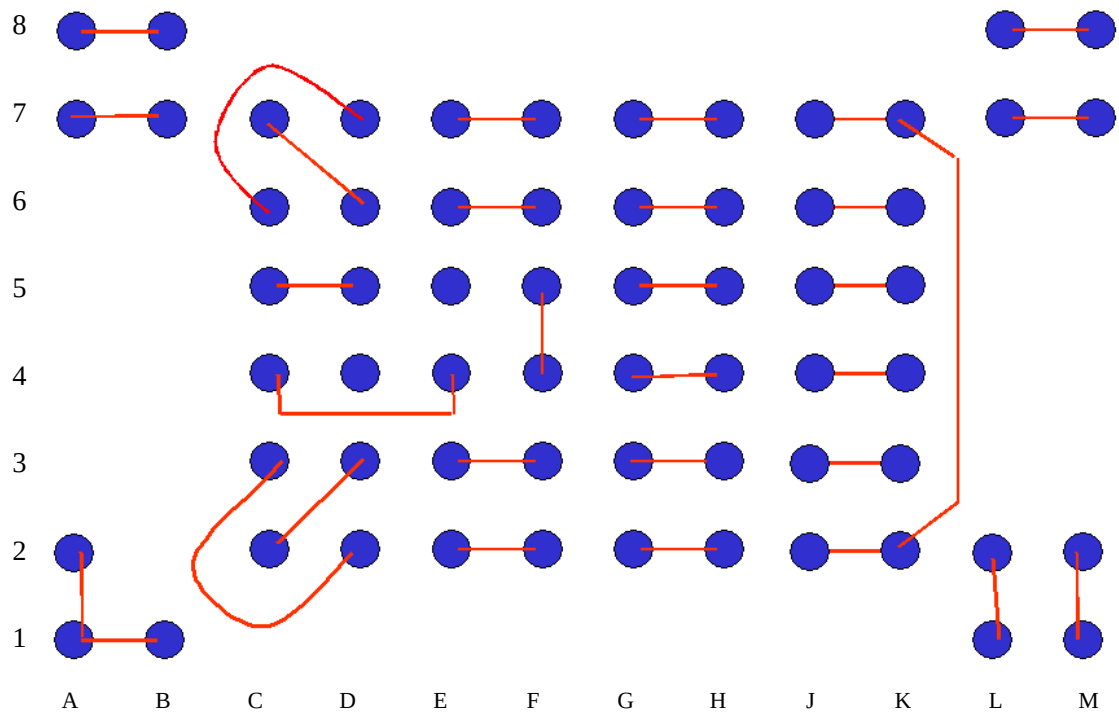


Figure 5-6. FBGA 64 Mbit Board Layout (Top View)

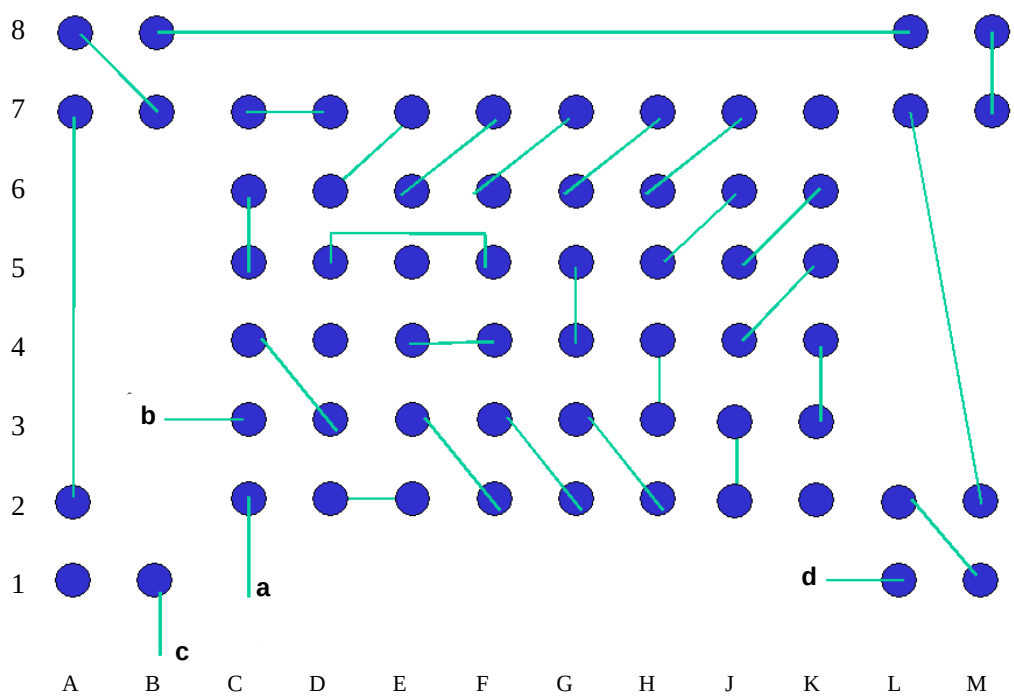


Figure 5-7. FBGA 84-Ball Daisy Chain Schematic (Top View)

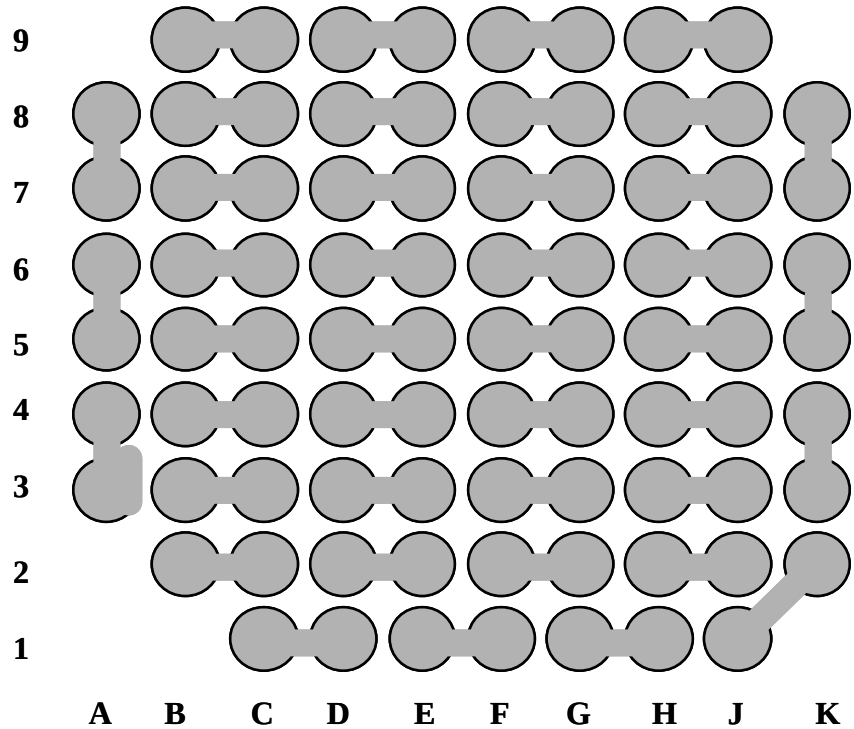


Figure 5-8. Fortified BGA 84-Ball Board Layout (Top View)

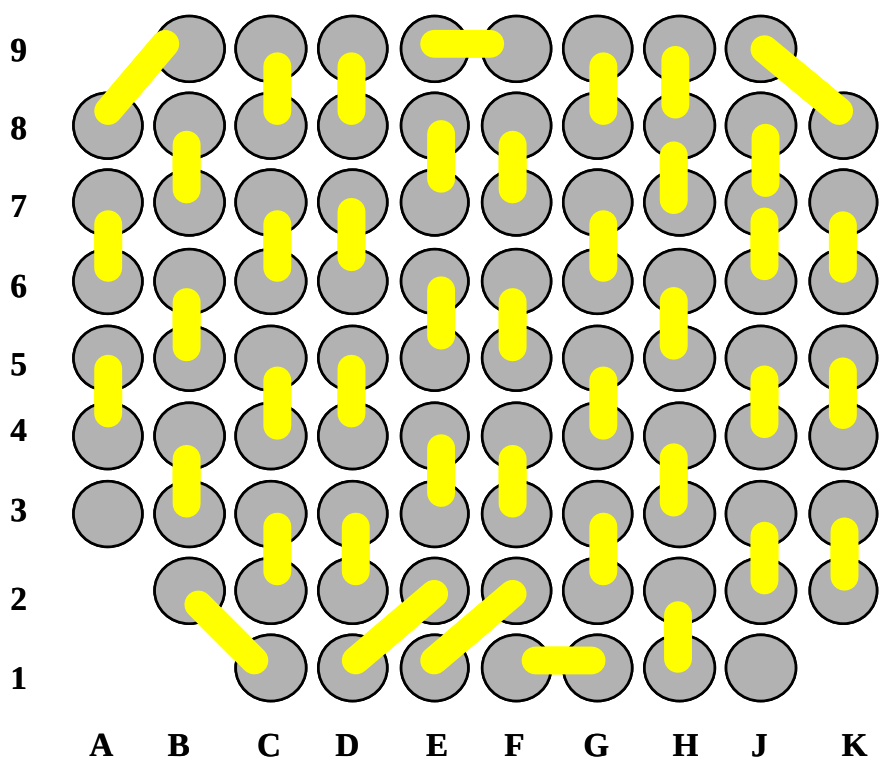


Figure 5-9. Fortified BGA 64-Ball Board Layout (Top View)

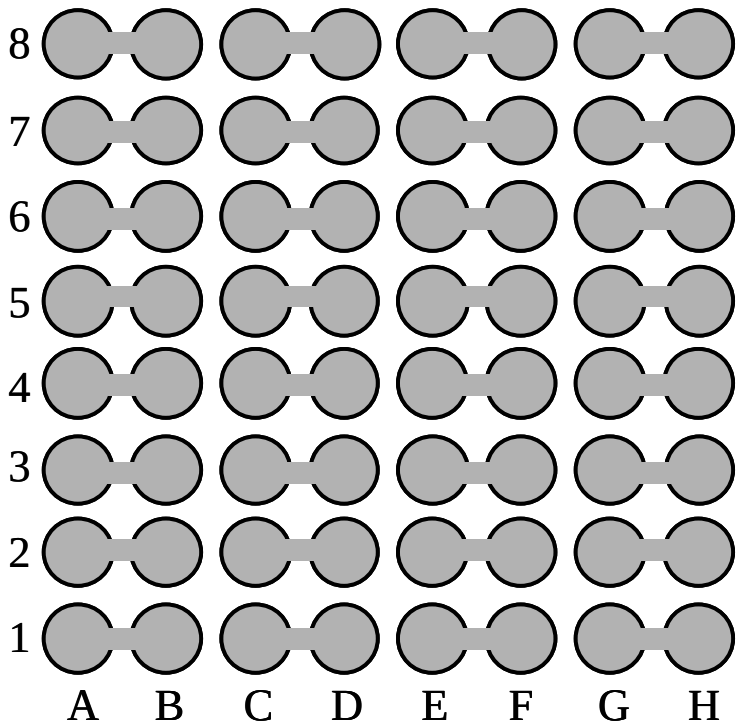


Figure 5-10. Fortified BGA 64-Ball Daisy Chain Schematic (Top View)

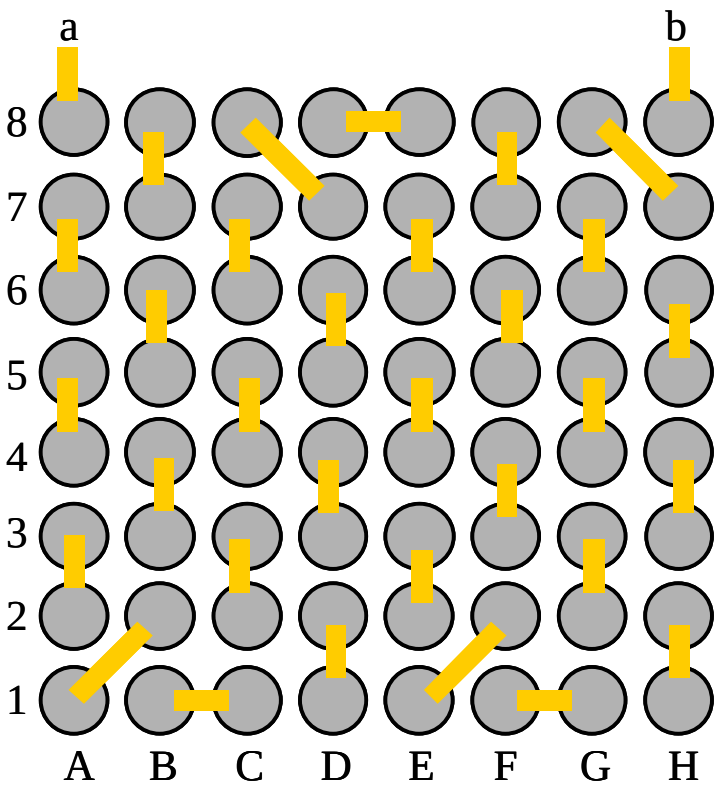


Figure 5-11. Fortified BGA 80-Ball Daisy Chain Schematic (Top View)

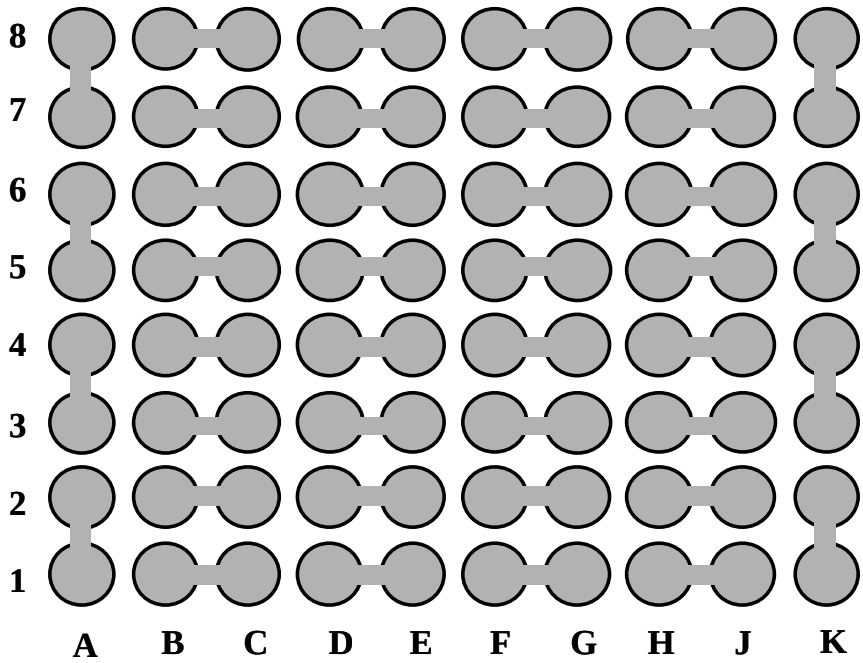
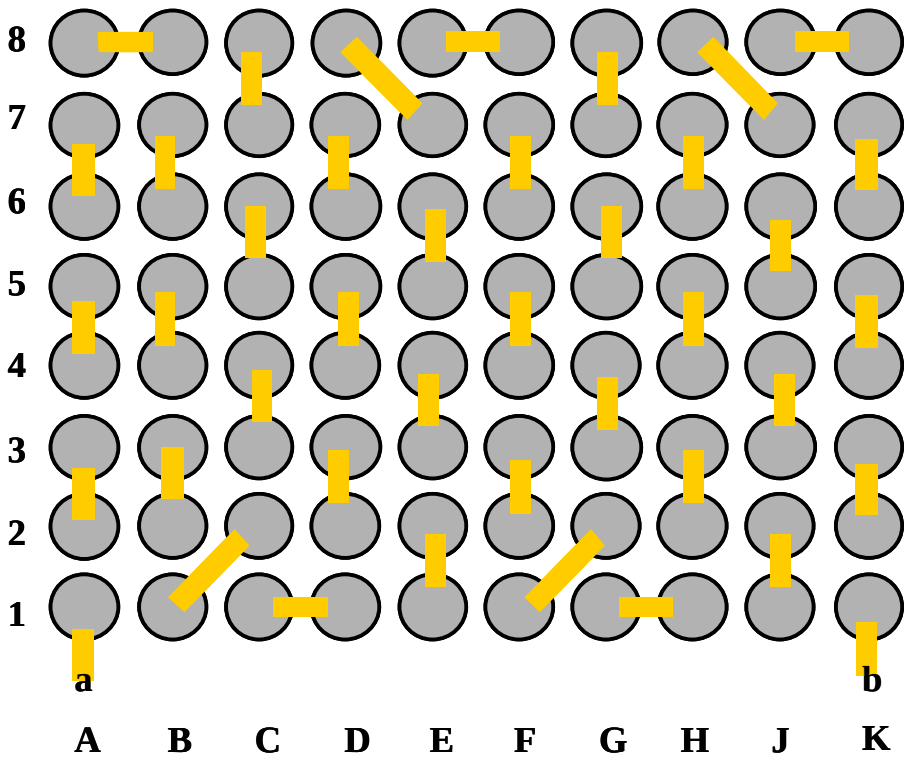


Figure 5-12. Fortified BGA 80-Ball Board Layout (Top View)



Chapter 6: Package Physical Description

KHANG:01-OCT-99:AE

4.1.2 FINEPITCH BALL GRID ARRAY, CSP FBGA (FB_)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010 .
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME .

△6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z .

△7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]

8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.

△10 FOR PACKAGE THICKNESS A IS THE CONTROLING DIMENSION.

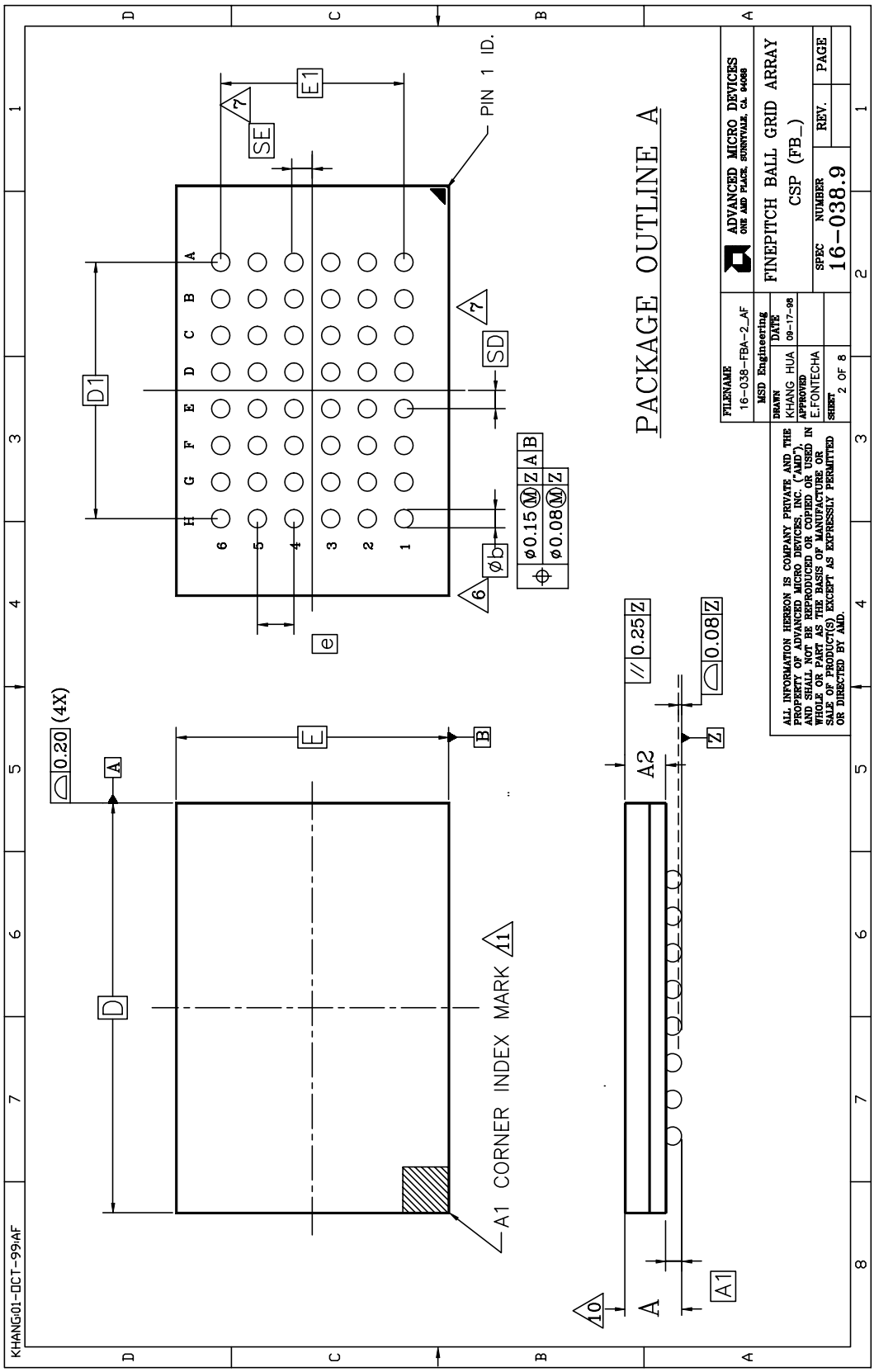
△11 A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

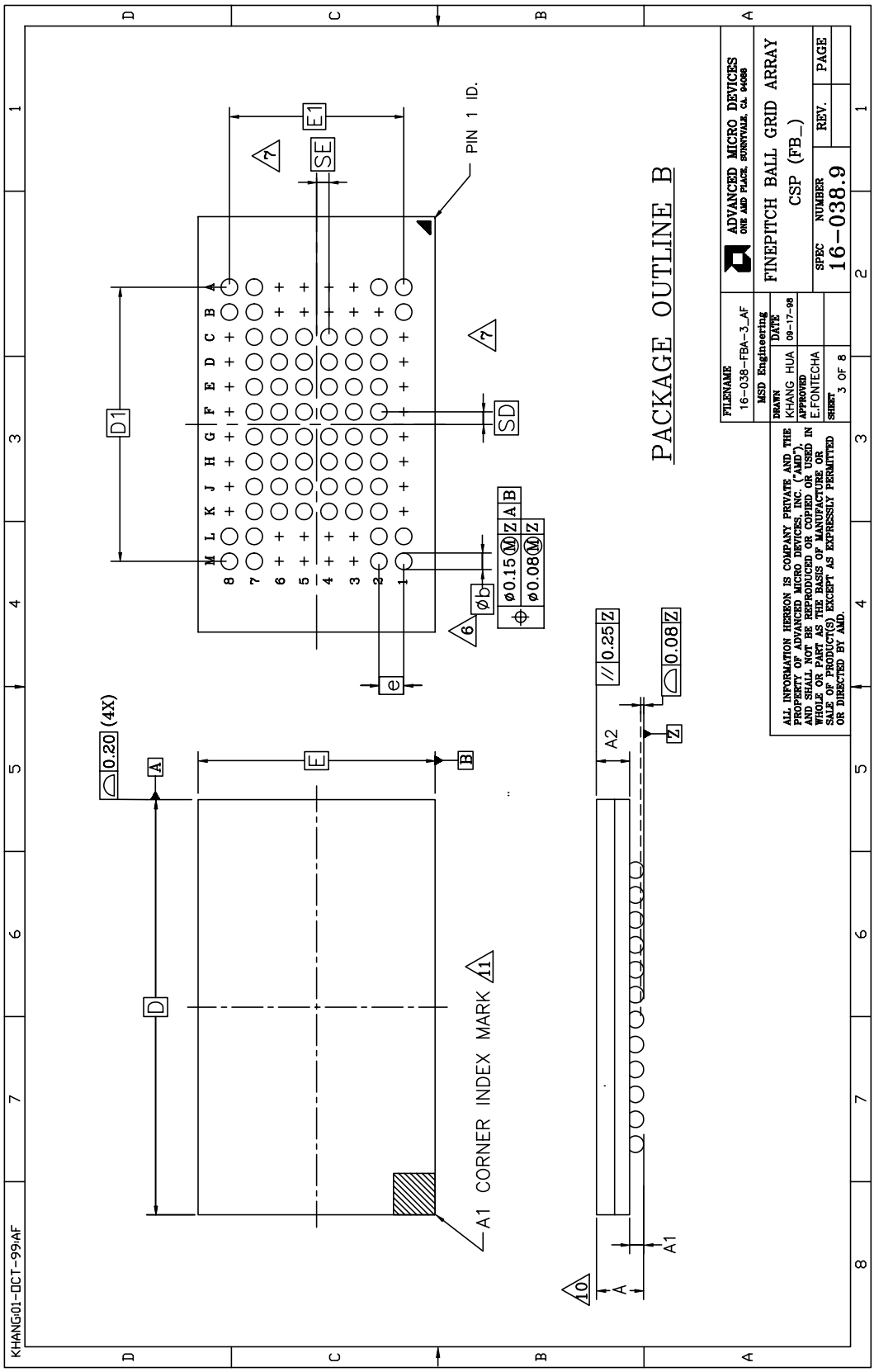
FILENAME	16–038–FBA–1_AE
	MSD Engineering
DRAWN	KHANG HUA
DATE	09–17–98
APPROVED	E.FONTECHA
SHEET	1 OF 8

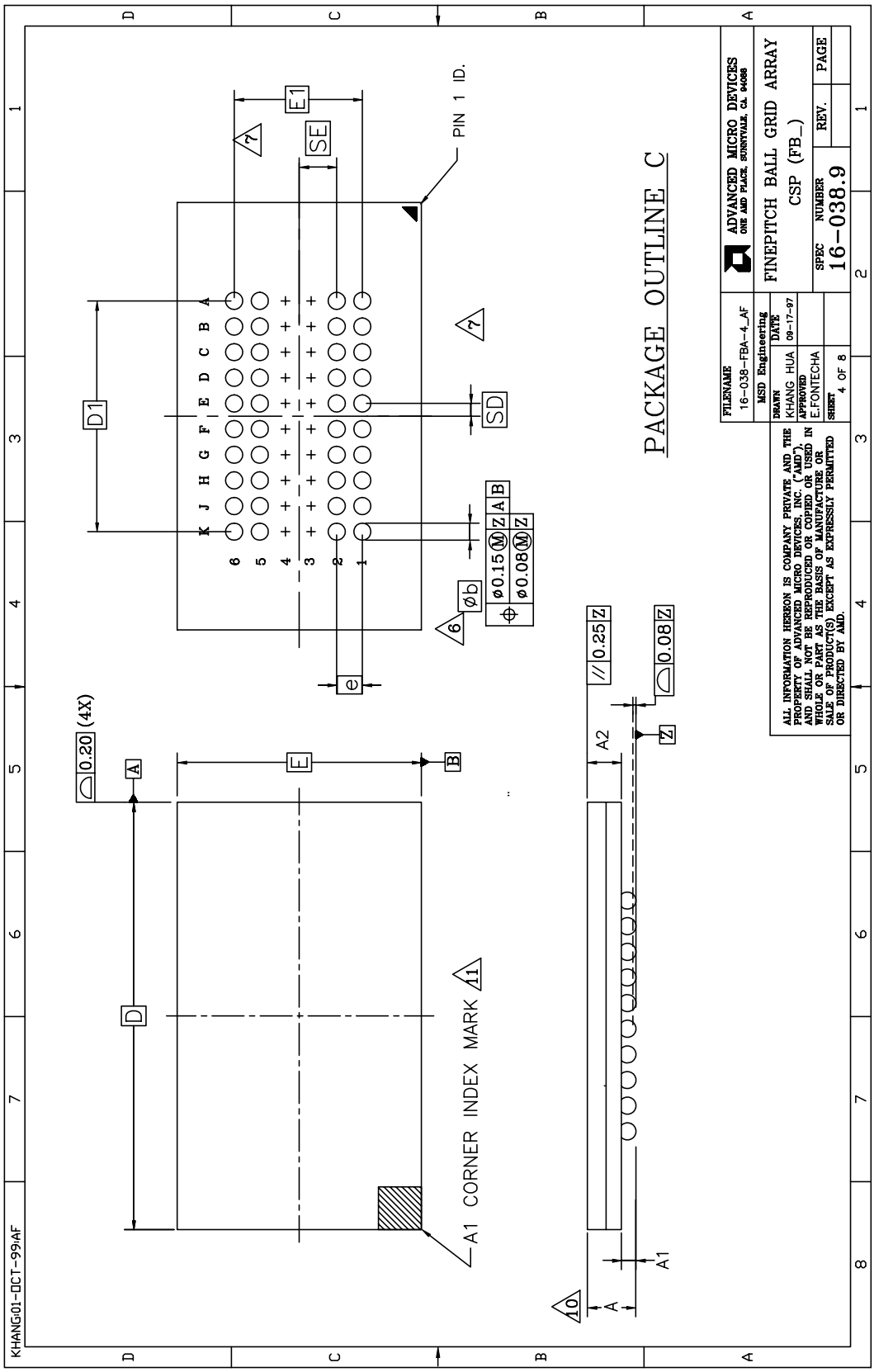
ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA. 94088

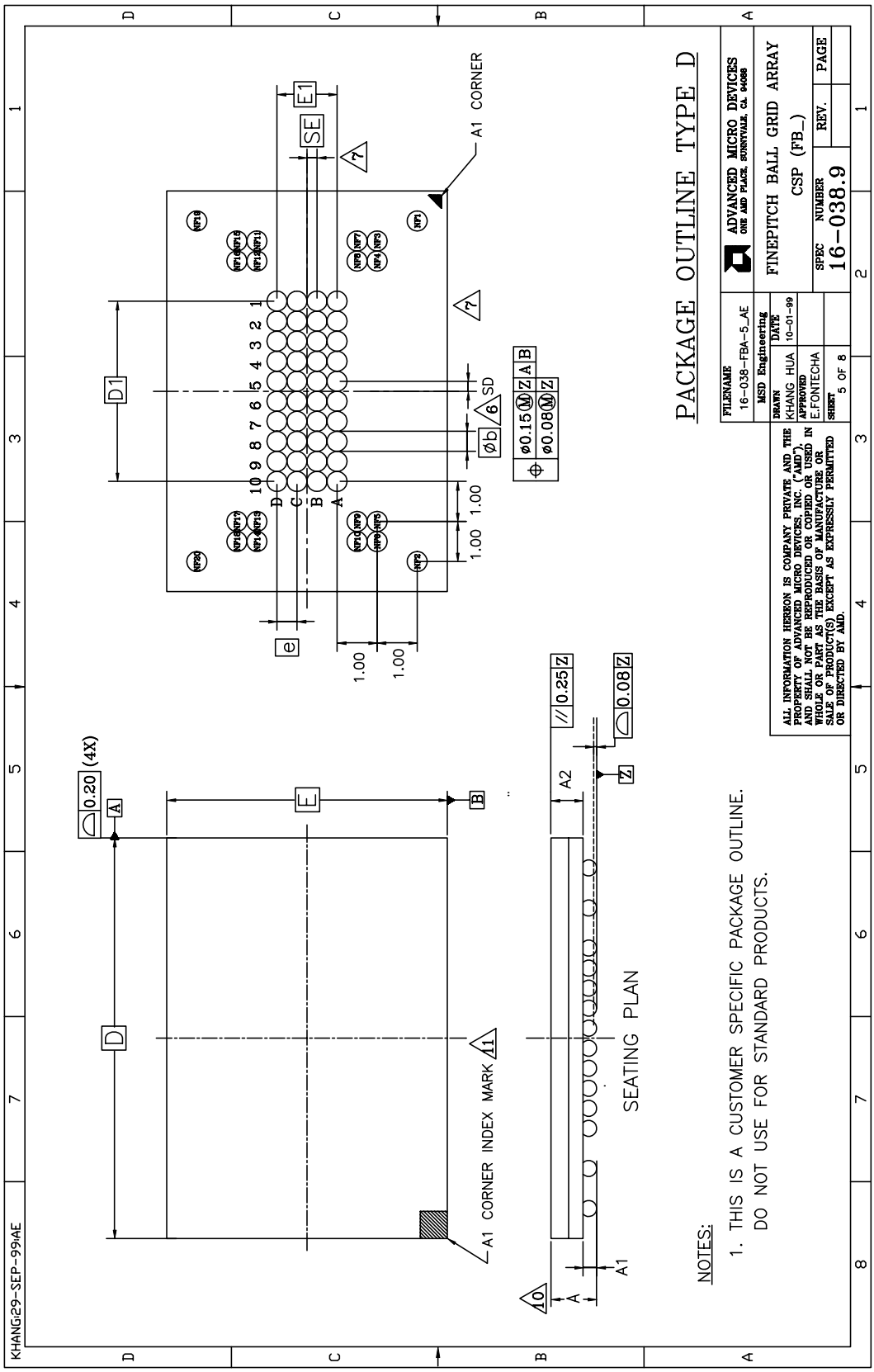
FINEPITCH BALL GRID ARRAY
CSP (FB_)

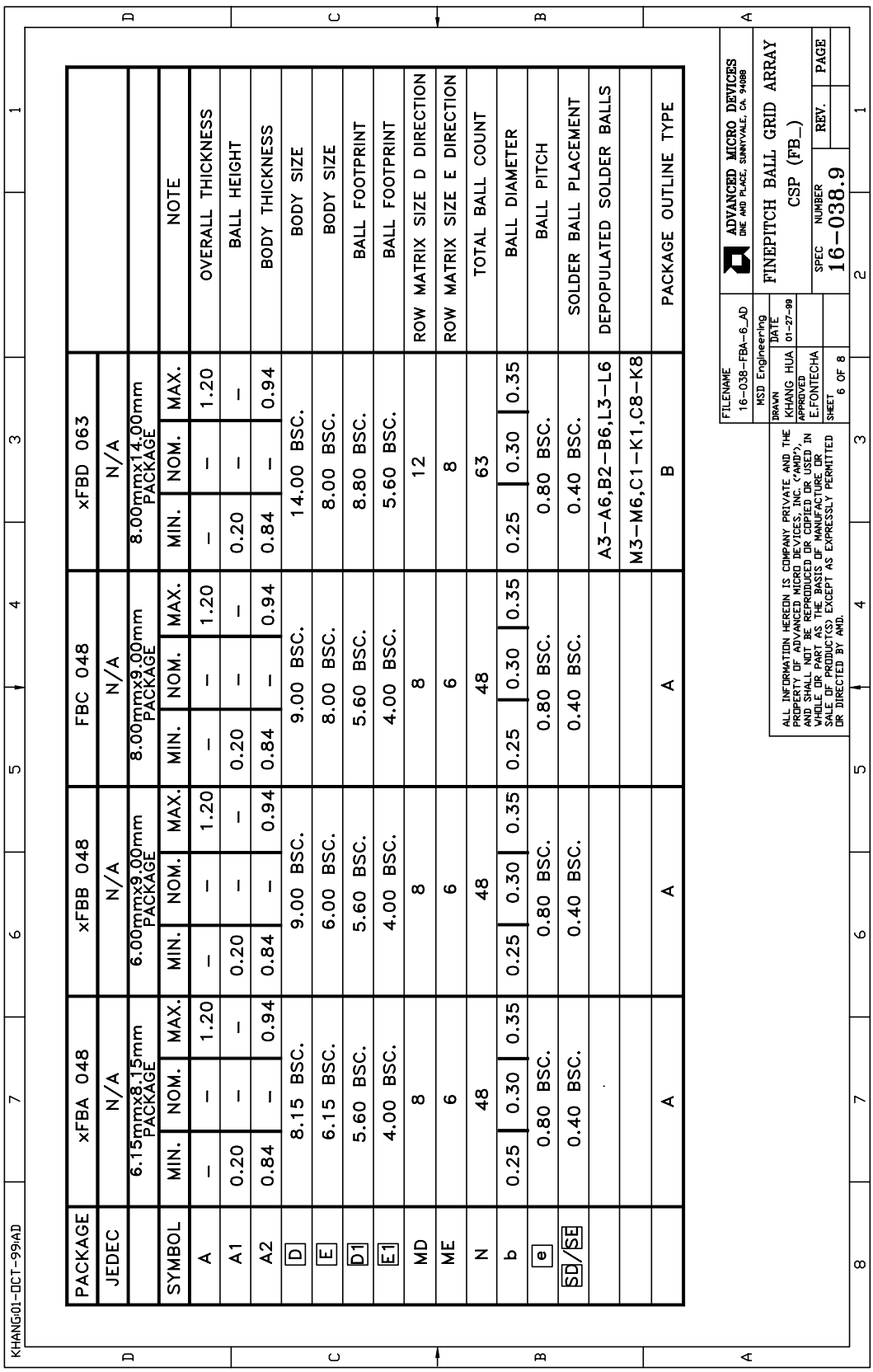
SPEC NUMBER	REV.	PAGE
16–038.9		


PACKAGE OUTLINE A
FINEPITCH BALL GRID ARRAY
CSP (FB_)
ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA. 94086
SPEC NUMBER
16-038.9
REV.
PAGE
FILENAME
16-038-FBA-2_AF
MSD Engineering
DRAWN
KHANG HUA
DATE
09-17-98
APPROVED
E.FONTECHA
SHEET
2 OF 8
ALL INFORMATION HEREON IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
PIN 1 ID.
A1 CORNER INDEX MARK
KHANG01-OCT-99-AF


PACKAGE OUTLINE B
PIN 1 ID.
A1 CORNER INDEX MARK
ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA. 94086
FINEPITCH BALL GRID ARRAY
CSP (FB_)
SPEC NUMBER
16-038.9
REV.
PAGE
FILENAME
16-038-FBA-3_AF
MSD Engineering
DRAWN
KHANG HUA
DATE
09-17-98
APPROVED
E.FONTECHA
SHEET
3 OF 8
ALL INFORMATION HEREON IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
KHANG01-OCT-99/AF


PACKAGE OUTLINE C
FINEPITCH BALL GRID ARRAY
CSP (FB_)
ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA. 94086
SPEC NUMBER
16-038.9
REV.
PAGE
FILENAME
16-038-FBA-4_AF
MSD Engineering
DRAWN
KHANG HUA
DATE
09-17-97
APPROVED
E.FONTECHA
SHEET
4 OF 8
ALL INFORMATION HEREON IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
PIN 1 ID.
A1 CORNER INDEX MARK
KHANG01-OCT-99-AF


PACKAGE OUTLINE TYPE D
A1 CORNER
A1 CORNER INDEX MARK
SEATING PLAN
NOTES:
1. THIS IS A CUSTOMER SPECIFIC PACKAGE OUTLINE.
DO NOT USE FOR STANDARD PRODUCTS.
ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA. 94086
FINEPITCH BALL GRID ARRAY
CSP (FB_)
SPEC NUMBER
16-038.9
REV.
PAGE
FILENAME
16-038-FBA-5_AE
MSD Engineering
DRAWN
KHANG HUA
10-01-99
APPROVED
E.FONTECHA
SHEET
5 OF 8
ALL INFORMATION HEREON IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
KHANG:29-SEP-99:AE



PACKAGE	xFBA 048			xFBB 048			FBC 048			xFBD 063			
JEDEC	N/A			N/A			N/A			N/A			
	6.15mmx8.15mm PACKAGE			6.00mmx9.00mm PACKAGE			8.00mmx9.00mm PACKAGE			8.00mmx14.00mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	NOTE
A	–	–	1.20	–	–	1.20	–	–	1.20	–	–	1.20	OVERALL THICKNESS
A1	0.20	–	–	0.20	–	–	0.20	–	–	0.20	–	–	BALL HEIGHT
A2	0.84	–	0.94	0.84	–	0.94	0.84	–	0.94	0.84	–	0.94	BODY THICKNESS
D	8.15 BSC.			9.00 BSC.			9.00 BSC.			14.00 BSC.			BODY SIZE
E	6.15 BSC.			6.00 BSC.			8.00 BSC.			8.00 BSC.			BODY SIZE
D1	5.60 BSC.			5.60 BSC.			5.60 BSC.			8.80 BSC.			BALL FOOTPRINT
E1	4.00 BSC.			4.00 BSC.			4.00 BSC.			5.60 BSC.			BALL FOOTPRINT
MD	8			8			8			12			ROW MATRIX SIZE D DIRECTION
ME	6			6			6			8			ROW MATRIX SIZE E DIRECTION
N	48			48			48			63			TOTAL BALL COUNT
b	0.25	0.30	0.35	0.25	0.30	0.35	0.25	0.30	0.35	0.25	0.30	0.35	BALL DIAMETER
e	0.80 BSC.			0.80 BSC.			0.80 BSC.			0.80 BSC.			BALL PITCH
SD/SE	0.40 BSC.			0.40 BSC.			0.40 BSC.			0.40 BSC.			SOLDER BALL PLACEMENT
										A3–A6,B2–B6,L3–L6			DEPOPULATED SOLDER BALLS
										M3–M6,C1–K1,C8–K8			
	A			A			A			B			PACKAGE OUTLINE TYPE

KHANG01-OCT-99-AD

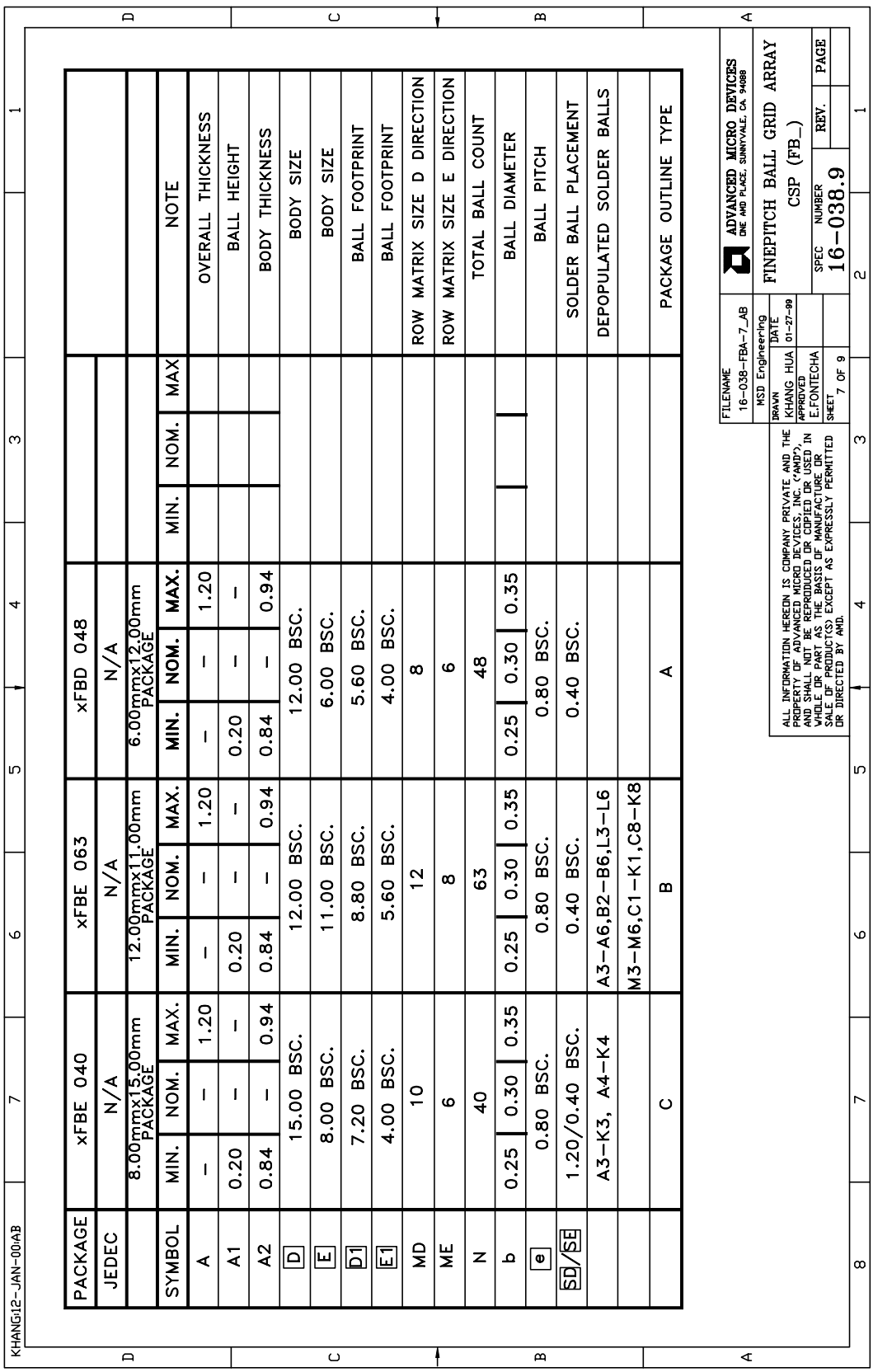
ALL INFORMATION HEREIN IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.

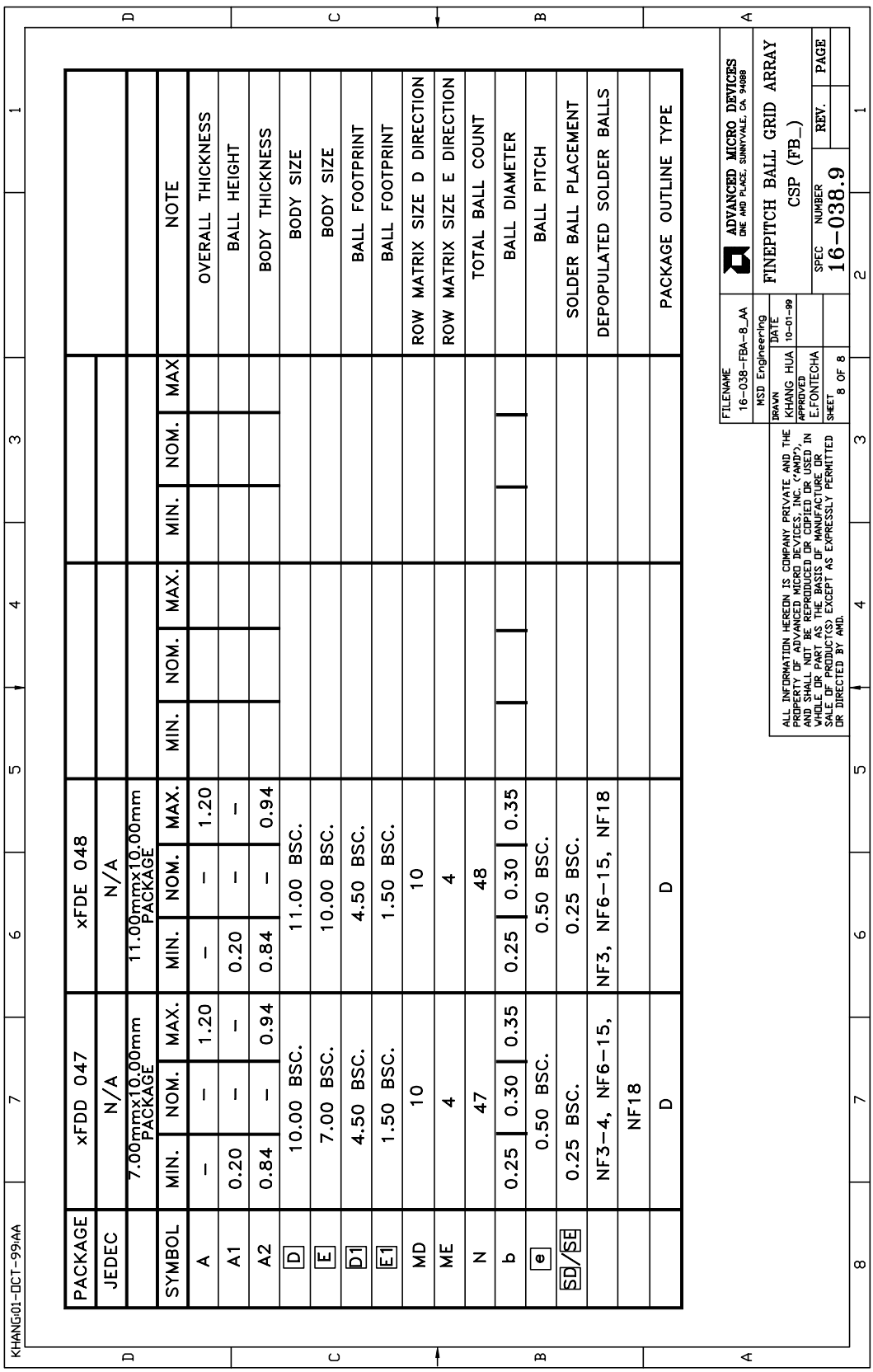
FILENAME 16-038-FBA-6_AD
MSD Engineering
DRAWN KHANG HUA DATE 01-27-00
APPROVED E.FONTECHA
SHEET 6 OF 8

ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA. 94088

FINEPITCH BALL GRID ARRAY
CSP (FB_)

SPEC NUMBER 16-038.9 REV. PAGE


KHANG12-JAN-00AB
PACKAGE xFBE 040 xFBE 063 xFBD 048
JEDEC N/A N/A N/A
8.00mmx15.00mm PACKAGE 12.00mmx11.00mm PACKAGE 6.00mmx12.00mm PACKAGE
SYMBOL MIN. NOM. MAX. MIN. NOM. MAX. MIN. NOM. MAX. MIN. NOM. MAX. NOTE
A – – 1.20 – – 1.20 – – 1.20 OVERALL THICKNESS
A1 0.20 – – 0.20 – – 0.20 – – BALL HEIGHT
A2 0.84 – 0.94 0.84 – 0.94 0.84 – 0.94 BODY THICKNESS
D 15.00 BSC. 12.00 BSC. 12.00 BSC. BODY SIZE
E 8.00 BSC. 11.00 BSC. 6.00 BSC. BODY SIZE
D1 7.20 BSC. 8.80 BSC. 5.60 BSC. BALL FOOTPRINT
E1 4.00 BSC. 5.60 BSC. 4.00 BSC. BALL FOOTPRINT
MD 10 12 8 ROW MATRIX SIZE D DIRECTION
ME 6 8 6 ROW MATRIX SIZE E DIRECTION
N 40 63 48 TOTAL BALL COUNT
b 0.25 0.30 0.35 0.25 0.30 0.35 0.25 0.30 0.35 BALL DIAMETER
e 0.80 BSC. 0.80 BSC. 0.80 BSC. BALL PITCH
SD/SE 1.20/0.40 BSC. 0.40 BSC. 0.40 BSC. SOLDER BALL PLACEMENT
A3–K3, A4–K4 A3–A6,B2–B6,L3–L6 DEPOPULATED SOLDER BALLS
M3–M6,C1–K1,C8–K8
C B A PACKAGE OUTLINE TYPE
ALL INFORMATION HEREIN IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
FILENAME 16-038-FBA-7_AB
MSD Engineering
DRAWN KHANG HUA DATE 01-27-00
APPROVED E.FONTECHA
SHEET 7 OF 9
ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA 94088
FINEPITCH BALL GRID ARRAY
CSP (FB_)
SPEC NUMBER 16-038.9
REV.
PAGE


KHANG01-OCT-99-AA
PACKAGE xFDD 047 xFDE 048
JEDEC N/A N/A
7.00mmx10.00mm PACKAGE 11.00mmx10.00mm PACKAGE
SYMBOL MIN. NOM. MAX. MIN. NOM. MAX. MIN. NOM. MAX. NOTE
A – – 1.20 – – 1.20 OVERALL THICKNESS
A1 0.20 – – 0.20 – – BALL HEIGHT
A2 0.84 – 0.94 0.84 – 0.94 BODY THICKNESS
D 10.00 BSC. 11.00 BSC. BODY SIZE
E 7.00 BSC. 10.00 BSC. BODY SIZE
D1 4.50 BSC. 4.50 BSC. BALL FOOTPRINT
E1 1.50 BSC. 1.50 BSC. BALL FOOTPRINT
MD 10 10 ROW MATRIX SIZE D DIRECTION
ME 4 4 ROW MATRIX SIZE E DIRECTION
N 47 48 TOTAL BALL COUNT
b 0.25 0.30 0.35 0.25 0.30 0.35 BALL DIAMETER
e 0.50 BSC. 0.50 BSC. BALL PITCH
SD/SE 0.25 BSC. 0.25 BSC. SOLDER BALL PLACEMENT
NF3-4, NF6-15, NF3, NF6-15, NF18 DEPOPULATED SOLDER BALLS
NF18
D D PACKAGE OUTLINE TYPE
ALL INFORMATION HEREIN IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
FILENAME 16-038-FBA-8_AA
MSD Engineering
DRAWN KHANG HUA DATE 10-01-99
APPROVED E.FONTECHA
SHEET 8 OF 8
ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA 94088
FINEPITCH BALL GRID ARRAY
CSP (FB_)
SPEC NUMBER 16-038.9
REV.
PAGE

BOB:25-FEB-02

SECTION 4.1 : LFRBGA-R PACKAGE – FLA 069

NOTES:

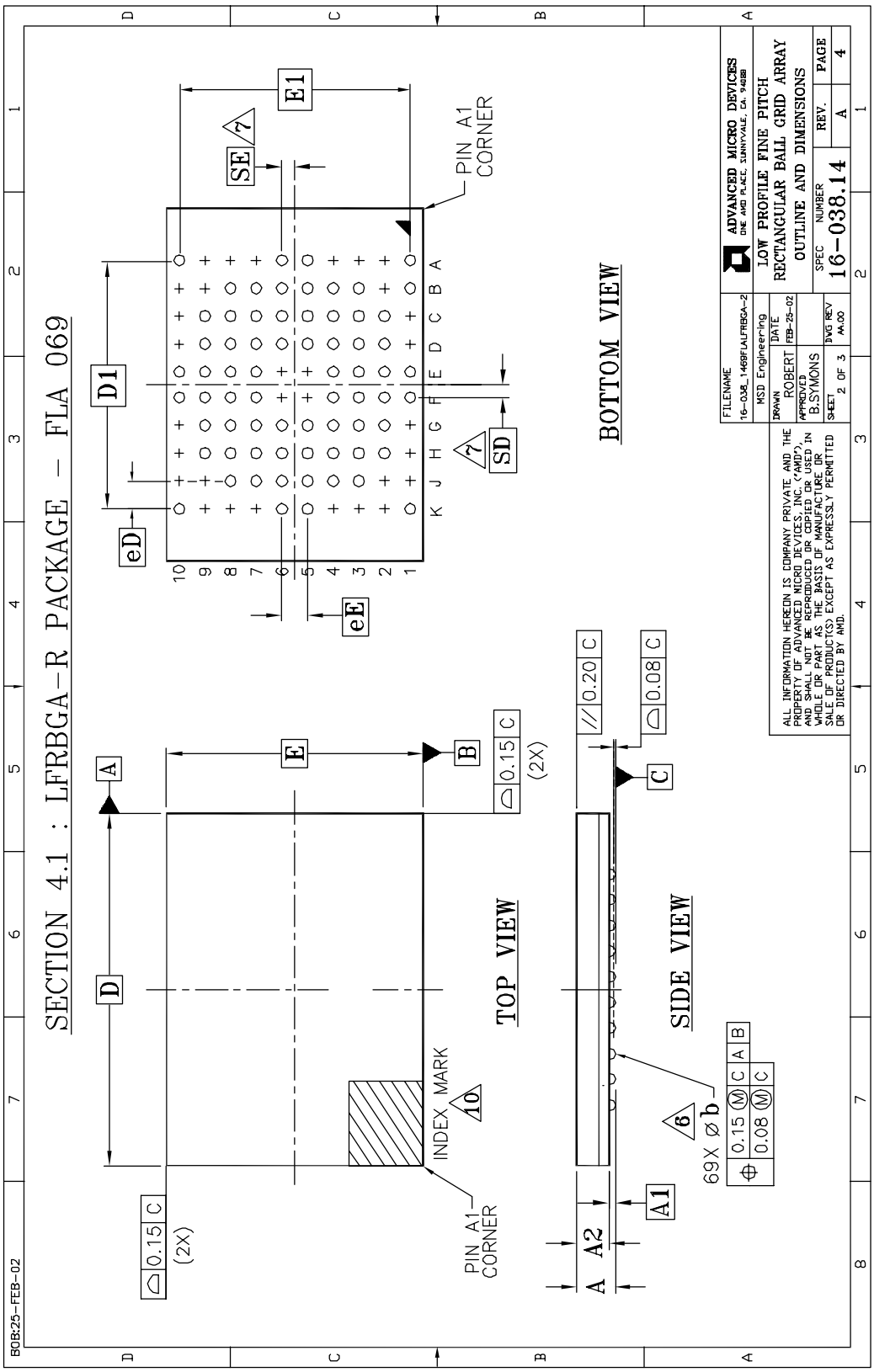
1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

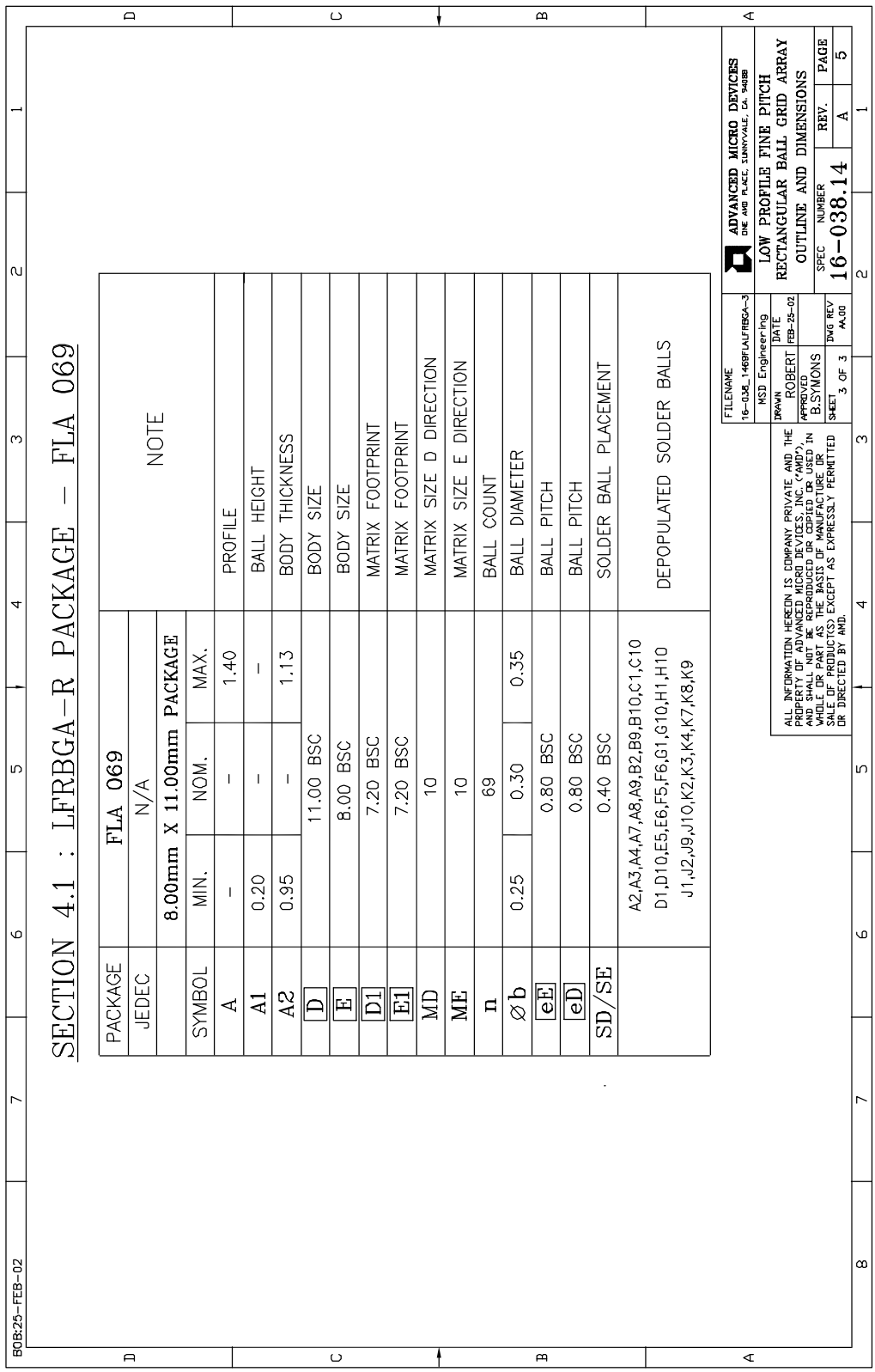
FILENAME	16-038_1469FLAlFRBGA-1
	MSD Engineering
DRAWN	ROBERT
DATE	FEB-25-02
APPROVED	B.SYMONS
SHEET	1 OF 3
DWG REV	AA.00

ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA. 94088

LOW PROFILE FINE PITCH
RECTANGULAR BALL GRID ARRAY
OUTLINE AND DIMENSIONS

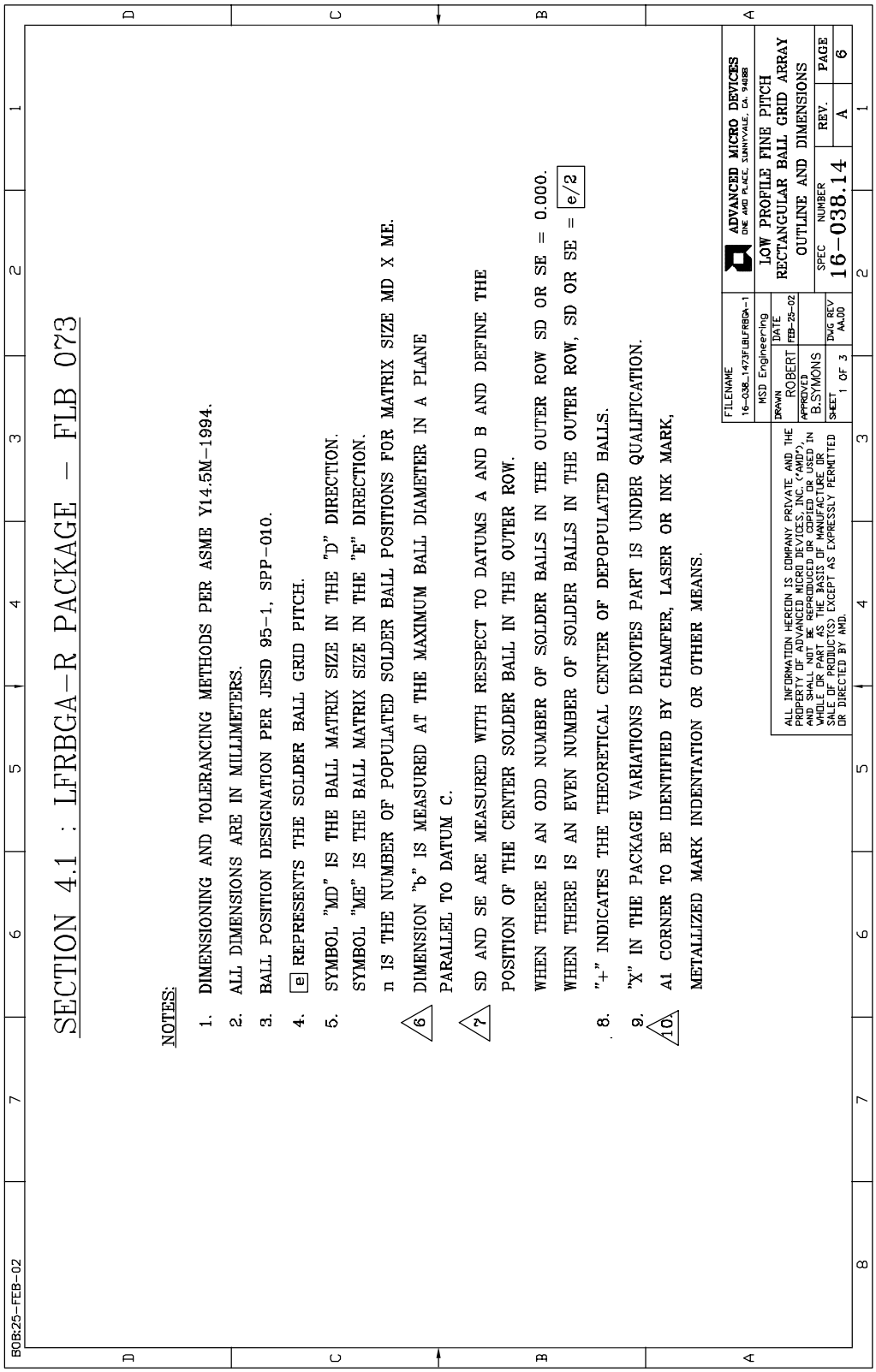
SPEC NUMBER	REV.	PAGE
16-038.14	A	3

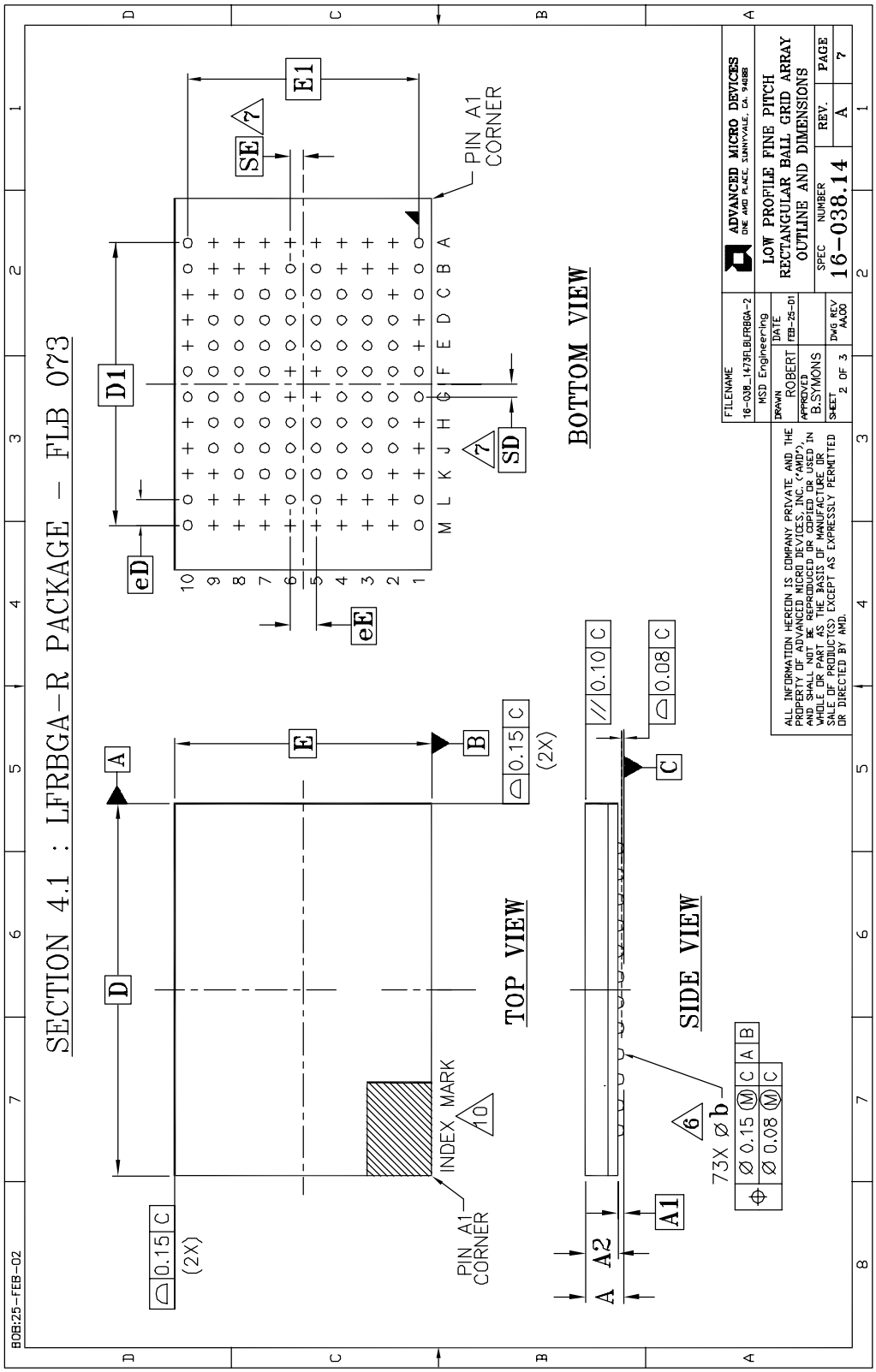

SECTION 4.1 : LFRBGA-R PACKAGE – FLA 069
BOTTOM VIEW
TOP VIEW
SIDE VIEW
PIN A1 CORNER
INDEX MARK
ADVANCED MICRO DEVICES
LOW PROFILE FINE PITCH
RECTANGULAR BALL GRID ARRAY
OUTLINE AND DIMENSIONS
SPEC NUMBER 16-038.14
REV. A
PAGE 4
ALL INFORMATION HEREIN IS COMPANY PRIVATE, AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"). AMD SHALL NOT BE REPRODUCED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED BY AMD.

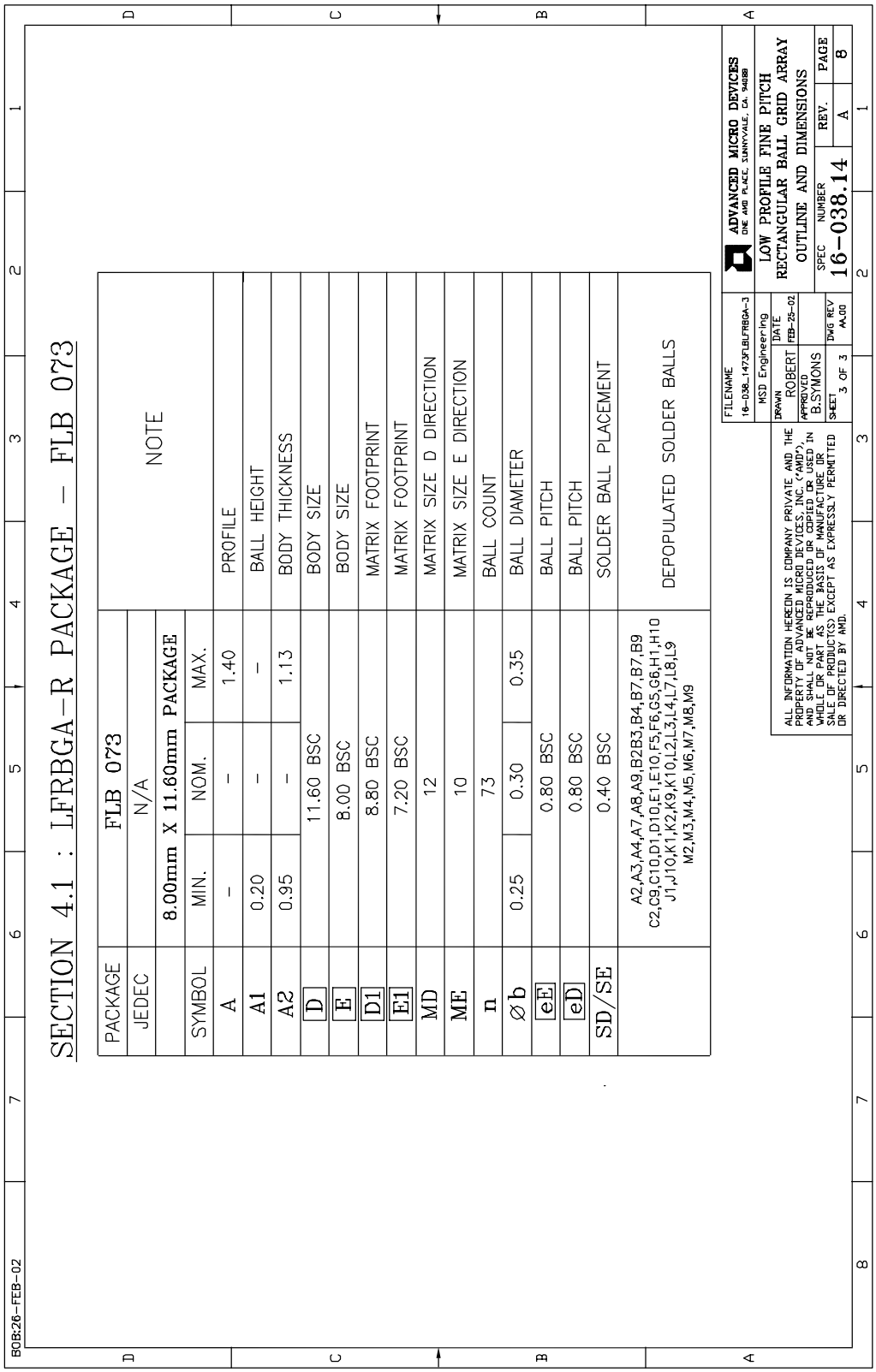


SECTION 4.1 : LFRBGA–R PACKAGE – FLA 069

PACKAGE	FLA 069			NOTE
JEDEC	N/A			
	8.00mm X 11.00mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	–	–	1.40	PROFILE
A1	0.20	–	–	BALL HEIGHT
A2	0.95	–	1.13	BODY THICKNESS
D		11.00 BSC		BODY SIZE
E		8.00 BSC		BODY SIZE
D1		7.20 BSC		MATRIX FOOTPRINT
E1		7.20 BSC		MATRIX FOOTPRINT
MD		10		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		69		BALL COUNT
Ø b	0.25	0.30	0.35	BALL DIAMETER
eE		0.80 BSC		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD/SE		0.40 BSC		SOLDER BALL PLACEMENT
	A2,A3,A4,A7,A8,A9,B2,B9,B10,C1,C10 D1,D10,E5,E6,F5,F6,G1,G10,H1,H10 J1,J2,J9,J10,K2,K3,K4,K7,K8,K9			DEPOPULATED SOLDER BALLS


BOB:25-FEB-02
SECTION 4.1 : LFRBGA-R PACKAGE – FLB 073
NOTES:
1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
10 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
ALL INFORMATION HEREON IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
FILENAME 16-038_147FLBLFRBGA-1
MSD Engineering
DRAWN ROBERT DATE FEB-25-02
APPROVED B.SYMONS
SHEET 1 OF 3
DWG REV AA.00
ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA. 94088
LOW PROFILE FINE PITCH
RECTANGULAR BALL GRID ARRAY
OUTLINE AND DIMENSIONS
SPEC NUMBER 16-038.14
REV. A
PAGE 6


SECTION 4.1 : LFRBGA-R PACKAGE – FLB 073
BOTTOM VIEW
TOP VIEW
SIDE VIEW
PIN A1 CORNER
INDEX MARK
ADVANCED MICRO DEVICES
LOW PROFILE FINE PITCH
RECTANGULAR BALL GRID ARRAY
OUTLINE AND DIMENSIONS
16-038.14
ALL INFORMATION HEREON IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.


SECTION 4.1 : LFRBGA-R PACKAGE – FLB 073
PACKAGE FLB 073
JEDEC N/A
8.00mm X 11.60mm PACKAGE
SYMBOL MIN. NOM. MAX. NOTE
A – – 1.40 PROFILE
A1 0.20 – – BALL HEIGHT
A2 0.95 – 1.13 BODY THICKNESS
D 11.60 BSC BODY SIZE
E 8.00 BSC BODY SIZE
D1 8.80 BSC MATRIX FOOTPRINT
E1 7.20 BSC MATRIX FOOTPRINT
MD 12 MATRIX SIZE D DIRECTION
ME 10 MATRIX SIZE E DIRECTION
n 73 BALL COUNT
Ø b 0.25 0.30 0.35 BALL DIAMETER
eE 0.80 BSC BALL PITCH
eD 0.80 BSC BALL PITCH
SD/SE 0.40 BSC SOLDER BALL PLACEMENT
A2,A3,A4,A7,A8,A9,B2B3,B4,B7,B7,B9
C2,C9,C10,D1,D10,E1,E10,F5,F6,G5,G6,H1,H10
J1,J10,K1,K2,K9,K10,L2,L3,L4,L7,L8,L9
M2,M3,M4,M5,M6,M7,M8,M9
DEPOPULATED SOLDER BALLS
ALL INFORMATION HEREIN IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
FILENAME 16-038_147FLBLFRBGA-3
MSD Engineering
DRAWN ROBERT DATE FEB-25-02
APPROVED B.SYMONS
SHEET 3 OF 3 DWG REV A4.00
ADVANCED MICRO DEVICES
LOW PROFILE FINE PITCH
RECTANGULAR BALL GRID ARRAY
OUTLINE AND DIMENSIONS
SPEC NUMBER 16-038.14 REV. A PAGE 8
BOB:26-FEB-02

HEROS:08-MAR-02

SECTION 4.1: LBGA PACKAGES.

LOW PROFILE BALL GRID ARRAY, LBGA (LA_)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE TOTAL NUMBER OF SOLDER BALLS.

△6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C .

△7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]

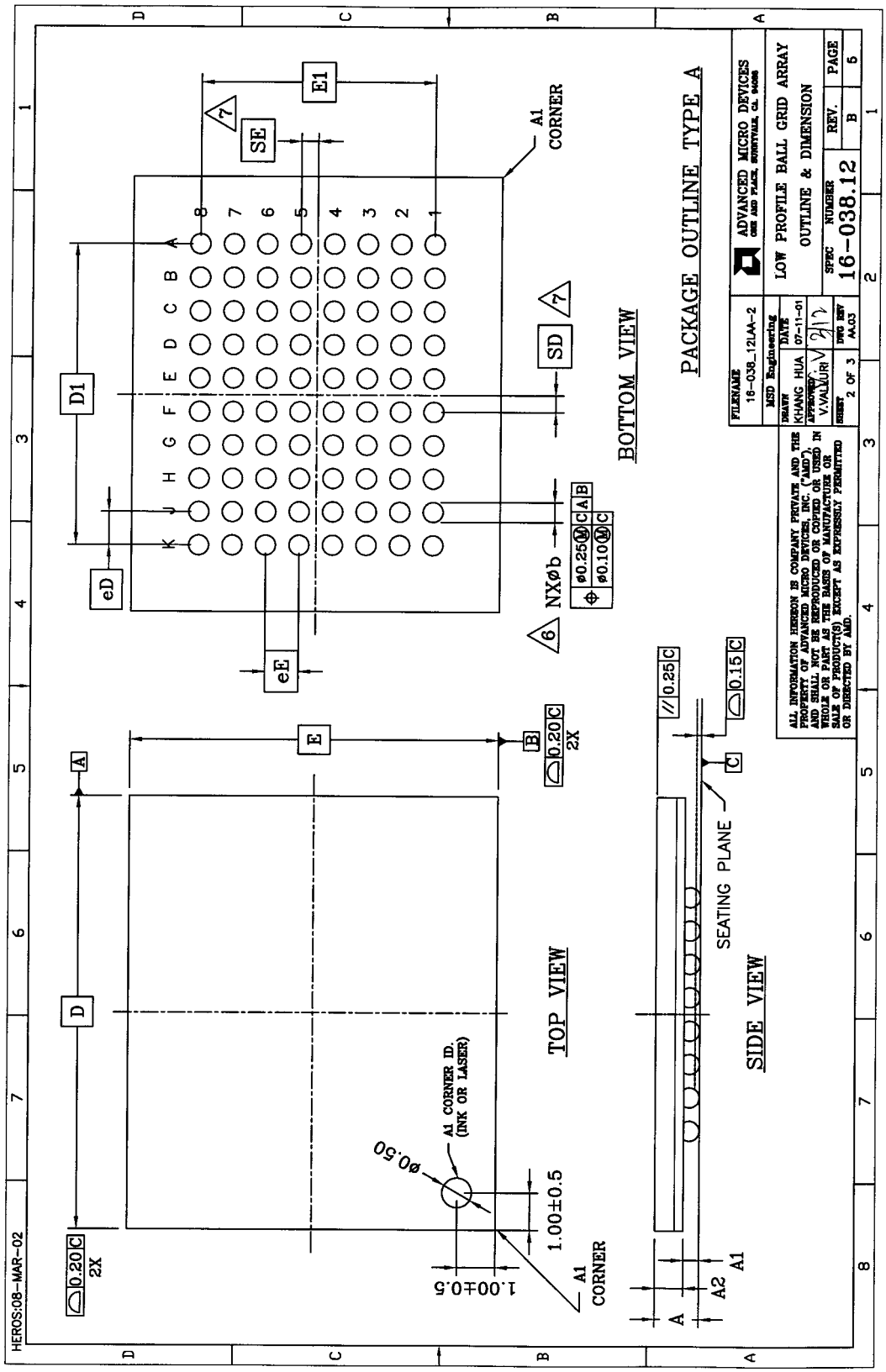
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

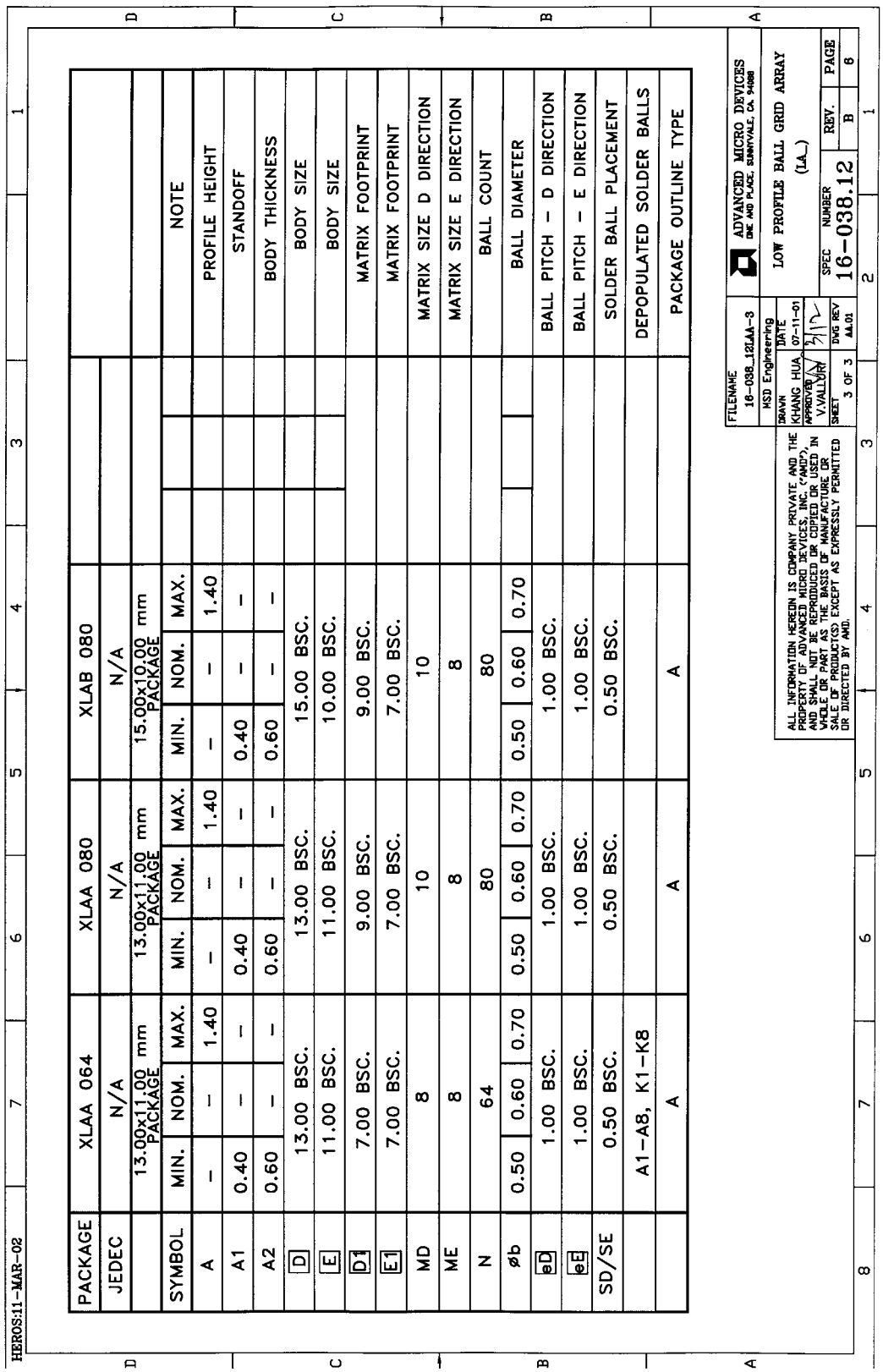
FILENAME	16-038_12LAA-1
	MSD Engineering
DRAWN	KHANG HUA
DATE	07-11-01
APPROVED	V.VALLURI
SHEET	1 OF 3
DWG REV	AA.02

ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA. 94088

LOW PROFILE BALL GRID ARRAY
OUTLINE & DIMENSION

SPEC NUMBER	REV.	PAGE
16-038.12	B	4


PACKAGE OUTLINE TYPE A
BOTTOM VIEW
TOP VIEW
SIDE VIEW
SEATING PLANE
A1 CORNER
A1 CORNER ID. (INK OR LASER)
ø0.50
1.00±0.5
1.00±0.5
NXøb
ø0.25Ⓜ C A B
ø0.10Ⓜ C
0.20 C 2X
0.15 C
0.25 C
D
D1
eD
E
E1
eE
SD
SE
A
A2
A1
ADVANCED MICRO DEVICES
LOW PROFILE BALL GRID ARRAY
OUTLINE & DIMENSION
SPEC NUMBER 16-038.12
REV. B
PAGE 6
FILENAME 16-038_12LA4-2
DRAWN KHANG HUA
APPROVED V.VALURI
DATE 07-11-01
DWG REV AA.03
SHEET 2 OF 3
ALL INFORMATION HEREON IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
HEROS:08-MAR-02



PACKAGE	XLAA 064			XLAA 080			XLAB 080				
JEDEC	N/A			N/A			N/A				
	13.00x11.00 mm PACKAGE			13.00x11.00 mm PACKAGE			15.00x10.00 mm PACKAGE				
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		NOTE
A	–	–	1.40	–	–	1.40	–	–	1.40		PROFILE HEIGHT
A1	0.40	–	–	0.40	–	–	0.40	–	–		STANDOFF
A2	0.60	–	–	0.60	–	–	0.60	–	–		BODY THICKNESS
D	13.00 BSC.			13.00 BSC.			15.00 BSC.				BODY SIZE
E	11.00 BSC.			11.00 BSC.			10.00 BSC.				BODY SIZE
D1	7.00 BSC.			9.00 BSC.			9.00 BSC.				MATRIX FOOTPRINT
E1	7.00 BSC.			7.00 BSC.			7.00 BSC.				MATRIX FOOTPRINT
MD	8			10			10				MATRIX SIZE D DIRECTION
ME	8			8			8				MATRIX SIZE E DIRECTION
N	64			80			80				BALL COUNT
øb	0.50	0.60	0.70	0.50	0.60	0.70	0.50	0.60	0.70		BALL DIAMETER
eD	1.00 BSC.			1.00 BSC.			1.00 BSC.				BALL PITCH – D DIRECTION
eE	1.00 BSC.			1.00 BSC.			1.00 BSC.				BALL PITCH – E DIRECTION
SD/SE	0.50 BSC.			0.50 BSC.			0.50 BSC.				SOLDER BALL PLACEMENT
	A1–A8, K1–K8										DEPOPULATED SOLDER BALLS
	A			A			A				PACKAGE OUTLINE TYPE

HEROS:11-MAR-02

ALL INFORMATION HEREIN IS COMPANY PRIVATE, AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. (AMD), AND SHALL NOT BE REPRODUCED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.

FILENAME 16-038_12AA-3

MSD Engineering

DRAWN KHANG HUA DATE 07-11-01

APPROVED V.VALLVA

SHEET 3 OF 3

ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA 94088

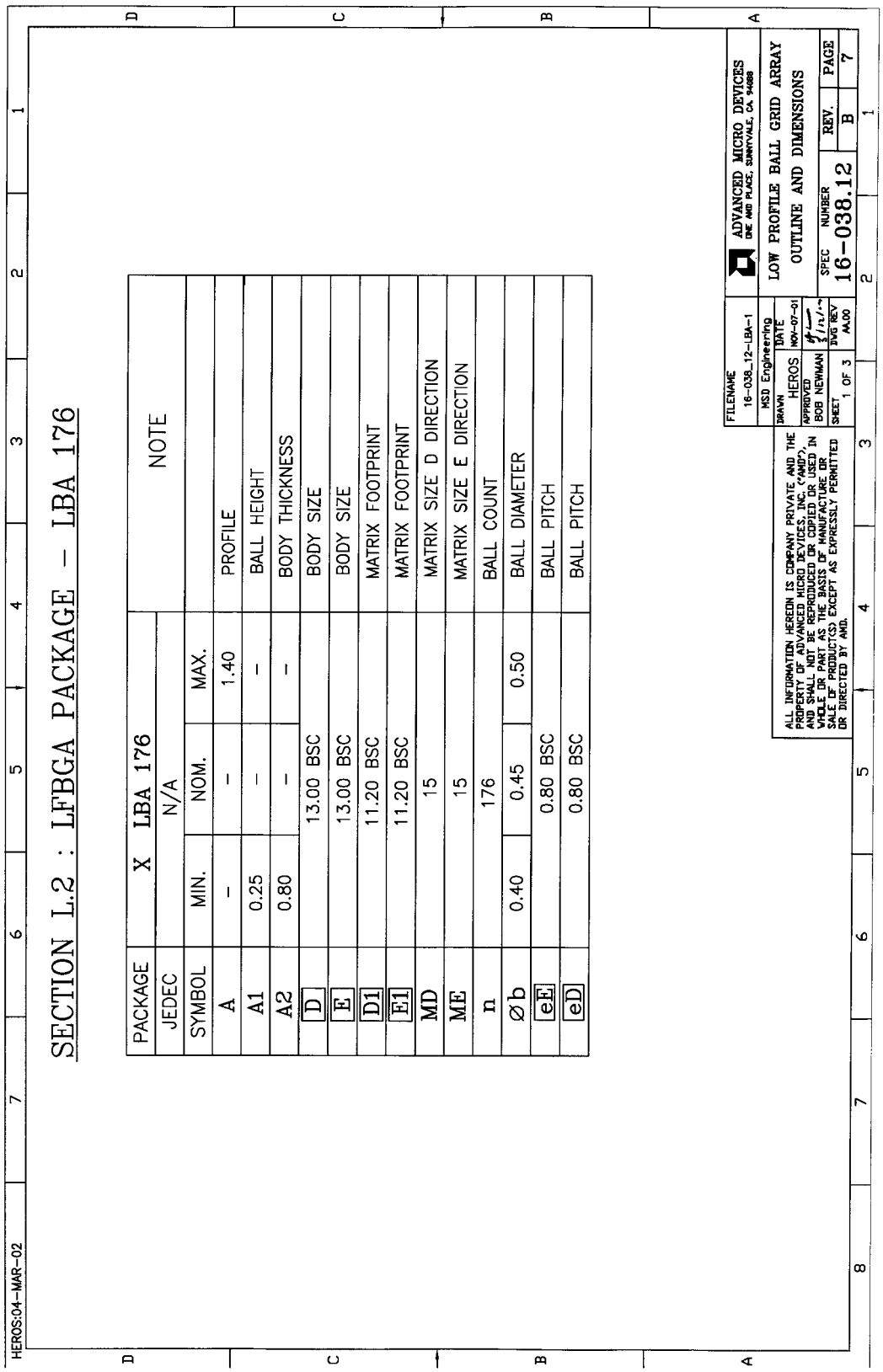
LOW PROFILE BALL GRID ARRAY
(LA_)

SPEC NUMBER 16-038.12

DWG REV 44.01

REV. B

PAGE 8



SECTION L.2 : LFBGA PACKAGE – LBA 176

PACKAGE	X	LBA 176		NOTE
JEDEC		N/A		
SYMBOL	MIN.	NOM.	MAX.	
A	–	–	1.40	PROFILE
A1	0.25	–	–	BALL HEIGHT
A2	0.80	–	–	BODY THICKNESS
D		13.00 BSC		BODY SIZE
E		13.00 BSC		BODY SIZE
D1		11.20 BSC		MATRIX FOOTPRINT
E1		11.20 BSC		MATRIX FOOTPRINT
MD		15		MATRIX SIZE D DIRECTION
ME		15		MATRIX SIZE E DIRECTION
n		176		BALL COUNT
Øb	0.40	0.45	0.50	BALL DIAMETER
eE		0.80 BSC		BALL PITCH
eD		0.80 BSC		BALL PITCH

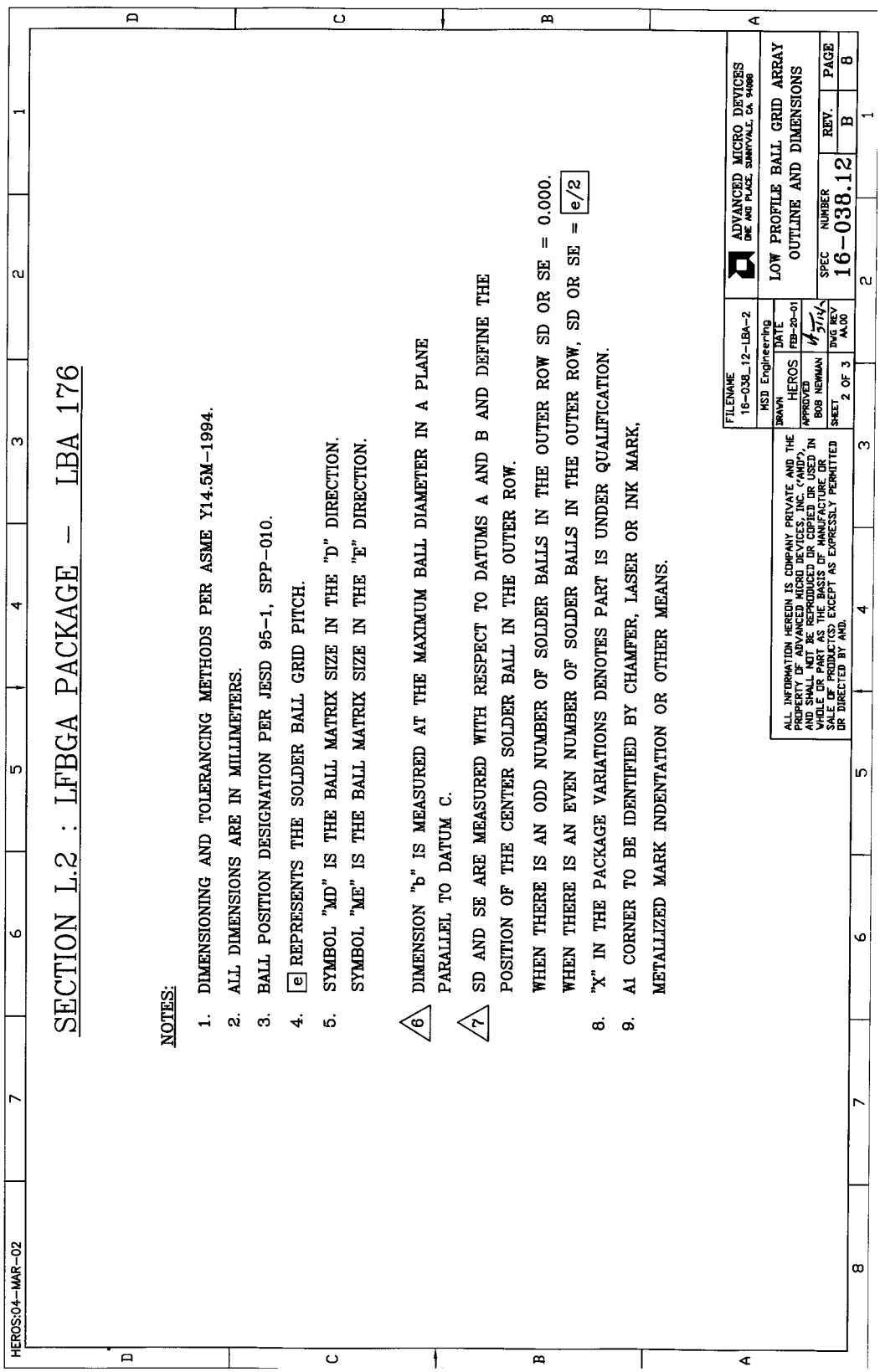
FILENAME 16-038_12-LBA-1
MSD Engineering
DRAWN HEROS DATE NOV-07-01
APPROVED BOB NEWMAN
SHEET 1 OF 3 DWG REV A4.00

ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA 94088

LOW PROFILE BALL GRID ARRAY
OUTLINE AND DIMENSIONS

SPEC NUMBER 16-038.12 REV. B PAGE 7

HEROS:04-MAR-02



SECTION L.2 : LFBGA PACKAGE – LBA 176

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

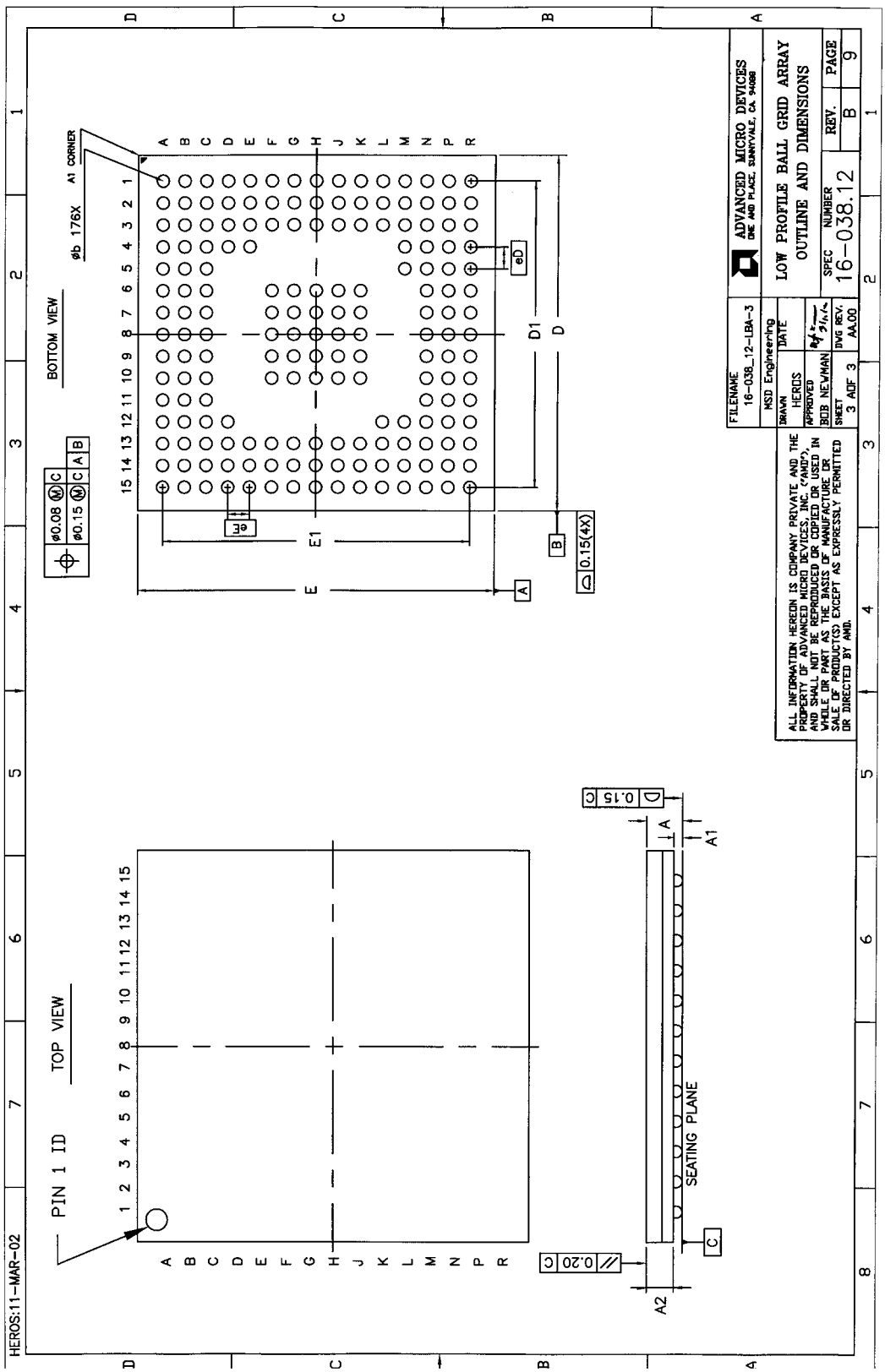
HEROS:04–MAR–02

FILENAME 16–038_12–LBA–2
MSD Engineering
DRAWN HEROS DATE FEB–20–01
APPROVED BOB NEWMAN
SHEET 2 OF 3 DWG REV A4.00

ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA 94088

LOW PROFILE BALL GRID ARRAY
OUTLINE AND DIMENSIONS

SPEC NUMBER 16–038.12 REV. B PAGE 8


ADVANCED MICRO DEVICES
ONE AMD PLACE, SUNNYVALE, CA 94088
LOW PROFILE BALL GRID ARRAY
OUTLINE AND DIMENSIONS
SPEC NUMBER
16-038.12
REV.
B
PAGE
9
FILENAME
16-038_12-LBA-3
MSD Engineering
DRAWN
HEROS
APPROVED
BOB NEWMAN
DATE
SHEET
3 ADF 3
DWG REV.
AA.00
ALL INFORMATION HEREIN IS COMPANY PRIVATE AND THE PROPERTY OF ADVANCED MICRO DEVICES, INC. ("AMD"), AND SHALL NOT BE REPRODUCED OR USED IN WHOLE OR PART AS THE BASIS OF MANUFACTURE OR SALE OF PRODUCT(S) EXCEPT AS EXPRESSLY PERMITTED OR DIRECTED BY AMD.
HEROS:11-MAR-02
TOP VIEW
PIN 1 ID
BOTTOM VIEW
A1 CORNER
ø0.08 M C
ø0.15 M C A B
ø0.15(4X)
SEATING PLANE
0.20 C
0.15 C D

FBGA Package Materials Descriptions

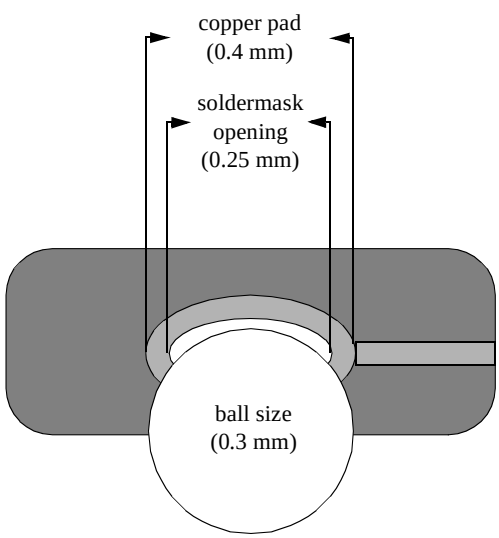
Table 6.1: FBGA-BT

Material Type	Thickness (µm)	Material Name	Young's Modulus (Pa)	CTE ppm/c	Poisson's Ratio
Mold Compound	530	SMT-B-1N	1.50E+10	1.60	0.25
Die Attach	25.4	QMI 536	1.24E+09	8.00	0.4
Silicon Die	254	Silicon	1.31E+11	2.60	0.28
Eutectic Solder Ball	300	Sn/Pb 63/37	3.10E+10	2.40	0.4
Copper Metalli-zation	27	Cu	1.21E+11	1.70	0.34
Wire	25.4	Gold			
Pad Plating	13	NI	2.00E+11	1.34	0.31
Solder Resist	50	Epoxy Res-in	2.75E+09	6.90	0.3
Substrate Core	200	BT resin	2.60E+10 (Ex = Ey); 1.10E+10 (Ez)	1.50 (CTEx = CTEy); 5.20 (CTEz)	0.11

FBGA-BT Ball Attach Detail

The ball attach for the FBGA-BT package used a 0.4 mm pad size and a soldermask opening of 0.25 mm, therefore it is soldermask defined. The ball size is 0.3 mm nominal. Note that Figure 6-1 shows ball-to-package attach, not ball-to-printed circuit board attach.

Figure 6-1. FBGA Package Ball Attach Detail



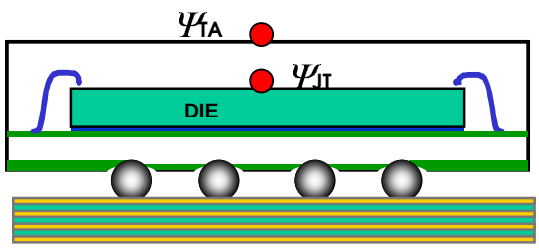
FBGA-BT

FBGA Thermal Management

Thermal energy management is important in today's rapidly changing microelectronics. To receive the best possible performance of any electronic product, proper heat dissipation is crucial. The temperature at which a microelectronic device operates determines among other things the speed and reliability of the product. Proper thermal management is achieved when heat is transferred or dissipated from the device to the system air, which is then vented out of the system. A few of the most important factors affecting device operation temperature are power dissipation, air temperature, package construction, and cooling mechanisms. The combinations of these factors determine the device's operation temperature.

How well FBGA packages dissipate heat can be measured or described by θ_{JA}, the junction to air thermal resistance value.

Figure 6-2. Path of Heat Dissipation



θ_{JA} – Junction to Air

Referring to Figure 6-2, θ_{JA} describes the path of heat dissipation from the active circuit surface of the die through the mold compound to the ambient air. The equations that govern this model are:

$\theta_{JA} = \Psi_{JT} - \Psi_{TA}$

$\Psi_{JT} = (T_{Jss} - T_{Tss})/P_d$

$\Psi_{TA} = (T_{Tss} - T_{Ass})/P_d$

Ψ_{JT} = Thermal characterization parameter from device junction to the top center of the package surface (°C/W).

θ_{JA} = Package thermal resistance from the die junction to the ambient air (°C/W). θ_{JA} is a measurement of the package internal thermal resistance as well as the conductive and convective thermal resistance from the package exterior to the ambient.

Ψ_{TA} = Thermal characterization parameter from top surface of the package-to-air (°C/W)

T_{Jss} = The junction temperature at steady-state. (^oC)

T_{Tss} = The package (top surface) temperature, at steady-state, measured by the thermocouple, infrared sensor, or fluoroptic sensor.

T_{ASS} = Temperature of Ambient Air at Steady State

P_d = Power (watts)

Table 6.2: Thermal Resistance Data

Pkg Type	X Pad Dim. (mils)	Y Pad Dim. (mils)	Ext. Die Num.	X Die Dim. (mils)	Y Die Dim. (mils)	Pd (mW)	θ_{JA} (°C/W)	θ_{JMA} (°C/W)	Ψ_{J-T} (°C/W)	SPD (LFPM)	Test Code
FBA048	281	200	Thermal	208	102	770 790 806 815 821	95.8	 81.6 71.0 65.8 62.3	14.1	0 200 400 600 800	1S0P
FBA048	281	200	Thermal	208	102	1417 1437 1445 1453 1456	49.2	 45.5 43.6 42.2 41.4	6.1	0 200 400 600 800	2S2P
FBB048	330	212	Thermal	208	102	697 716 728 735 739	89	 74.0 65.2 59.8 56.9	10.5	0 200 400 600 800	1S0P
FBB048	330	212	Thermal	208	102	1439 1461 1469 1476 1480	46	 42.0 40.3 39.0 38.1	4.4	0 200 400 600 800	2S2P
FBC048	319	315	Thermal	208	102	878 901 917 926 933	78.8	 65.4 56.9 51.9 48.7	5.3	0 200 400 600 800	1S0P
FBC048	319	315	Thermal	208	212	2010 2044 2057 2069 2077	35.7	 32.2 30.6 29.4 28.5	3.9	0 200 400 600 800	2S2P
FGC048	354	315	Thermal	208	212	729 752 767 775 779	89.2	 74.0 63.1 54.6 53.9		0 200 400 600 800	1SOP
FGB048	354	236	Thermal	102	212	2412	42.5			0	2S2P

Table 6.2: Thermal Resistance Data (Continued)

Pkg Type	X Pad Dim. (mils)	Y Pad Dim. (mils)	Ext. Die Num.	X Die Dim. (mils)	Y Die Dim. (mils)	Pd (mW)	θ_{JA} (°C/W)	θ_{JMA} (°C/W)	Ψ_{J-T} (°C/W)	SPD (LFPM)	Test Code
FGB048	354	236	Thermal	102	212	1134	91			0	1S0P
FBD063	528	315	Thermal	420	212	1042 1073 1090 1101 1109	64.5	 51.1 44.2 39.8 37.1	5.2	0 200 400 600 800	1S0P

Notes:

1. All measurement date are following SEMI G38-87 (in a wind tunnel), unless marked.
2. TEST CODE describes test PCB. "2 signal layer+2 power layer" or "1 signal layer+0 power layer"
3. For more information on Thermal Management please refer to "Memo on Ψ_{J-T} Case level Thermal Parameter" in the Appendix.
4. θ_{JMA} = Theta of junction to moving air.
5. SPD (LFPM) = Speed of moving air, in terms of "Linear Feet Per Minute".

Chapter 7: Board Design and Layout Considerations

General Design Considerations

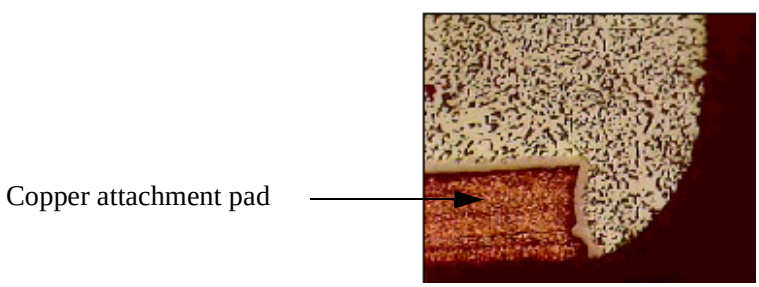
One of the first decisions to be made when designing boards for chip scale packages is whether it will be possible to use conventional PCB technology and design rules, or whether microvia technology will be necessary. Recently, microvia HDI (High Density Interconnects) boards have been adopted in several volume applications, particularly in cell-phones and camcorders, and the prices of microvia boards have been falling quickly. HDI are defined as having vias with a diameter less than 0.006 inch on pad size of 0.014 inch or smaller. However they are still more expensive. Measured on the basis of price per unit area per metal layer, microvia boards are at least twice as expensive as high-density conventional multilayer PCBs, even with blind and buried vias. Furthermore, there is also the question of availability: it may not be easy to find suppliers with production capacity for microvia boards.

It is for this reason that a pitch of 0.8 mm has been chosen for AMD's FBGA. As shown in the next section, single-layer routing for Flash Memory FBGA can be accomplished with line and space widths of 0.005 inch or more. Because of the relatively low lead count, this can be done in one layer, but if desired, connections down to inner layers can be accomplished through interstitial vias.

Solder-Mask Defined Versus Non-Solder-Mask Defined

There has been much discussion about the relative merits of solder-mask defined (SMD) and non-solder-mask defined (NSMD) lands for attaching area array packages such as conventional BGA and fine pitch BGA. AMD's FBGA can be used with either, but there are two important benefits of NSMD pads. One is that smaller copper pads can be used, thus providing more generous clearance for the routing channels. (Another is that the solder can wet around the sides of the pad during reflow (see Figure 7-1) thus providing a stronger joint.)

Figure 7-1. Solder Wetting Around Pad During Reflow



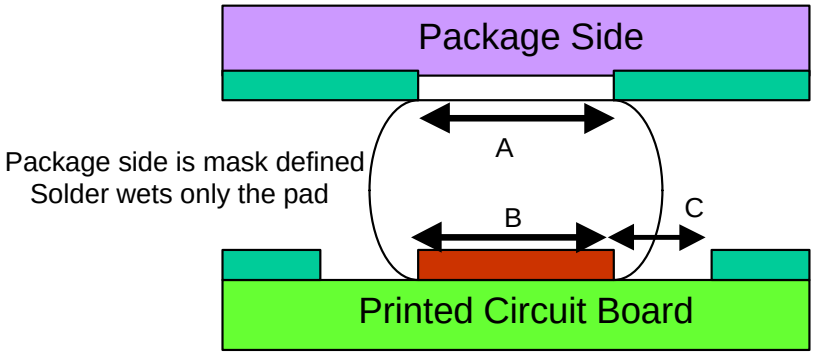
Note that if the kind of wetting shown in Figure 7-1 is desired, it is important to provide sufficient clearance of solder mask around the pad. The PCB supplier may consider the edge of the solder mask touching the edge of the pad to be acceptable, however, this condition would prevent the solder from completely wetting the side of the pad.

PC Board Surface Finish

Another design consideration is the selection of the surface finish for the board. While hot air solder leveled (HASL) boards have been successfully used for FBGA, it is generally felt that the domed shape of the pads makes it more difficult to achieve consistent assembly yields. On the other hand, excellent yields have been achieved with both Ni/Au plated pads and also with bare copper pads coated with organic solderability preservatives (OSP). In the case of Ni/Au plated pads, it is important to control the plating quality to prevent embrittlement of the solder joint. This can occur if the gold is too thick; gold thickness of 5 mils maximum is recommended. There has been some concern in the industry that certain kinds of nickel plating can cause embrittlement—your PCB supplier should be able to give advice on this subject.

Recommended Board Design Dimensions

Figure 7-2. Recommended Dimensions for the AMD 0.30 mm Solder Ball



Dimension	Function	Recommended Design Value		
		0.30 mm Solder Ball	0.35 mm Solder Ball	0.60 mm Solder Ball
A	Solder Mask Opening on the Package	0.25 ± 0.03 mm	0.30 ± 0.03 mm	0.50 ± 0.03 mm
B	Copper Pad Dimension	0.23 ± 0.01 mm	0.27 ± 0.015 mm	0.40 ± 0.03 mm
C	Copper Pad to Solder Mask Clearance	0.075 ± 0.025 mm	0.075 ± 0.025 mm	0.075 ± 0.025 mm
—	Trace Width	0.125 ± 0.25 mm	0.125 ± 0.25 mm	0.125 ± 0.25 mm

Routing Considerations

Figure 7-3. Example of 48-Ball Single Layer Board Routing

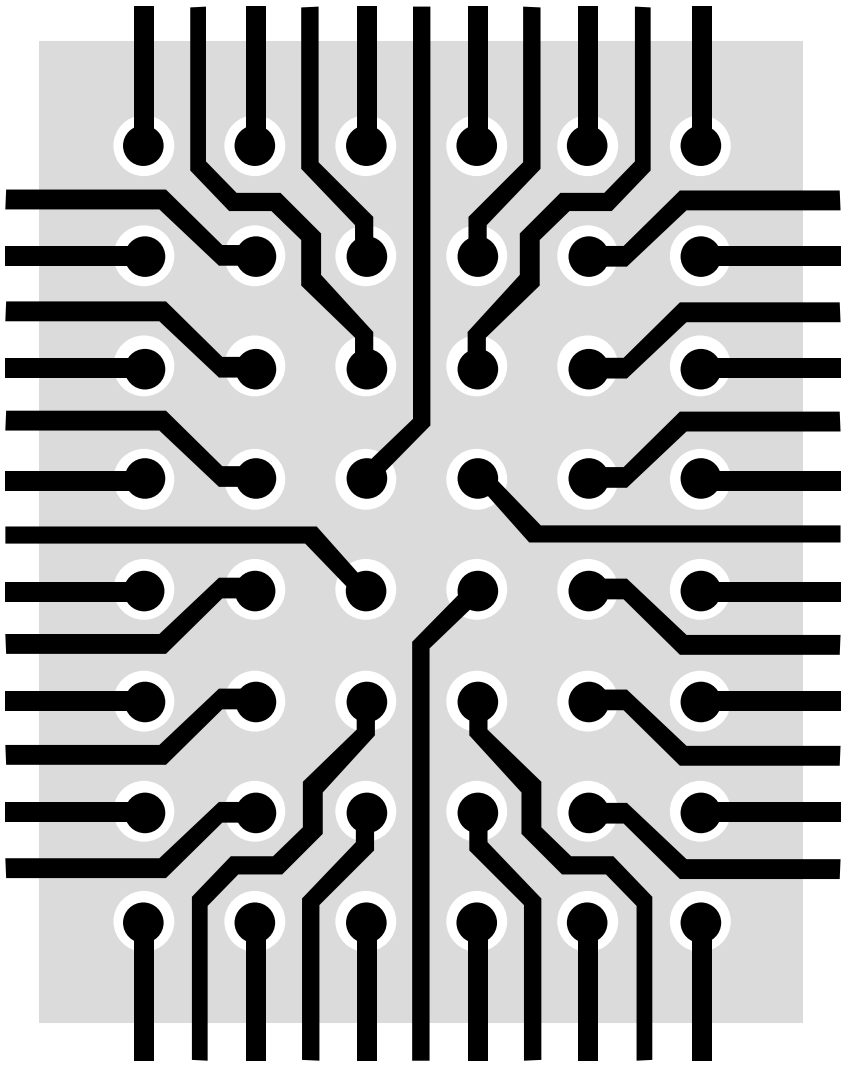
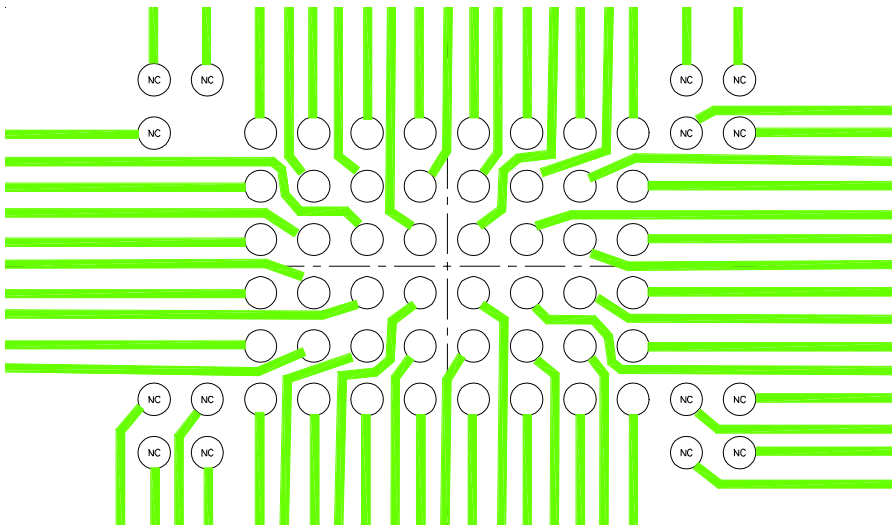
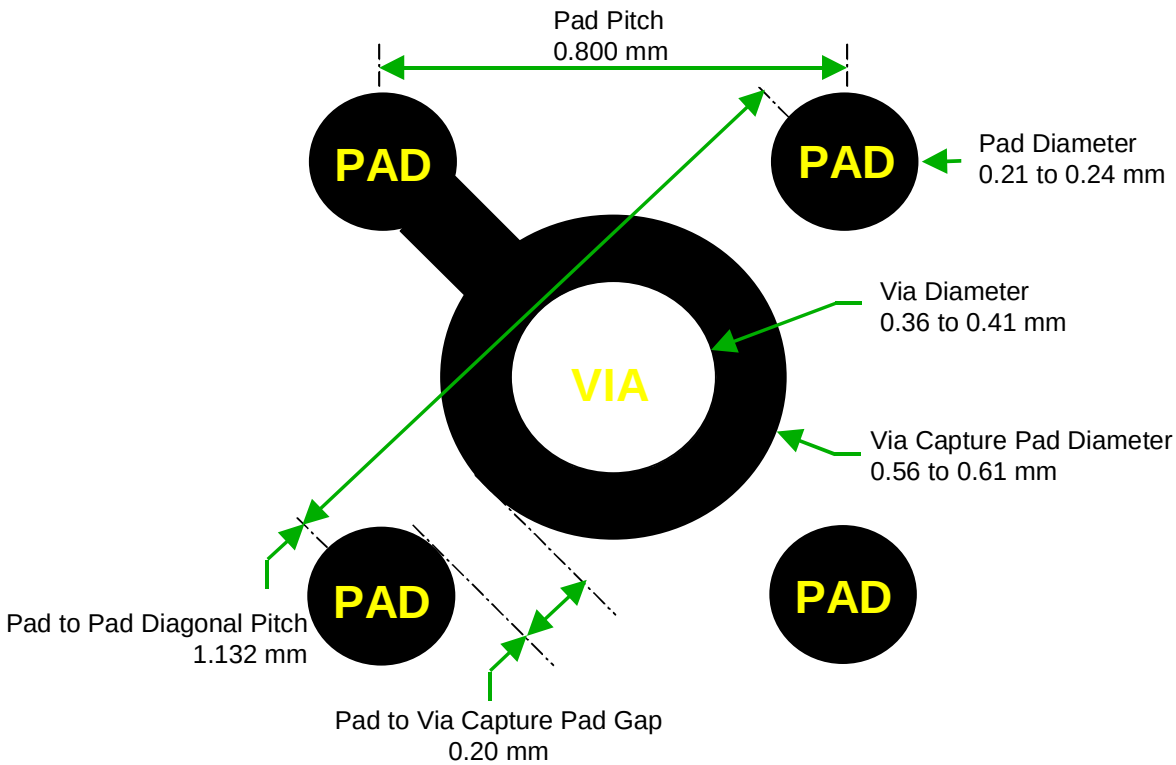


Figure 7-4. Example of 63-Ball Single Layer Board Routing Recommendation



Note: Recommended dimensions are the same as the 48-ball FBGA.

Figure 7-5. Example of Interstitial Via Design for High Ball Count Packages



Chapter 8: Component Qualification Testing

AMD has one of the highest reliability standards in the industry. Beginning from wafer sort to shipping of products, AMD has implemented vary stages of testing to ensure high quality and reliability. Samples are subjected to accelerated stress tests.

The advantages of accelerated stress testing are that these tests use fewer parts and can make failures occur faster. The stress levels used for these tests are more severe than that seen in the field with well-designed tests resulting in the same failure mechanisms. Component level testing includes:

1. Preconditioning (Moisture Level Testing)
2. Temperature Cycling
3. Highly Accelerated Stress Test (HAST)
4. Thermal Shock
5. Data Retention Bake
6. High Temperature Operating Life (HTOL)
7. Latch-up
8. Electrostatic Discharge (ESD)

Preconditioning

The Moisture Level Testing is modeled after JEDEC/IPC Standard J-STD-020A. This test is designed to determine the safe environmental conditions for product exposure, thus reducing the risk of moisture induced damages. Moisture damages may include, delamination, package cracks during reflows of board assembly, and "popcorn" effects.

There are six level of moisture sensitivity (See Table 8.1). Products are tested at Level-1 conditions, if fail, the next higher level is tested until it passes. The only difference between each level is the parameter of the moisture soak (also know as preconditioning).

There are 3 basic components:

1. 24 hour dry bake at 125°C
2. Preconditioning: Moisture storage parameters depending on JEDEC Moisture Sensitivity Level at which the package is being qualified (See Table 8.1).

Table 8.1: Moisture Sensitivity Levels

Level	Floor Life		Soak Requirements			
			Standard		Accelerated Equivalent	
	Time	Conditions	Time (Hours)	Conditions	Time (Hours)	Conditions
1	Unlimited	≤ 30°C/85% RH	168	85°C/85% RH		
2	1 Year	≤ 30°C/60% RH	168	85°C/60% RH		
2a	4 Weeks	≤ 30°C/60% RH	696	30°C/60% RH	120	60°C/60% RH
3	168 Hours	≤ 30°C/60% RH	192	30°C/60% RH	40	60°C/60% RH
4	72 Hours	≤ 30°C/60% RH	96	30°C/60% RH		
5	24 Hours	≤ 30°C/60% RH	48/72	30°C/60% RH		
6	6 Hours	≤ 30°C/60% RH	6	30°C/60% RH		

3. Three exposures to conditions to simulate passage through IR Convection Reflow. The first two passes are intended to simulate the assembly of a double-sided board, and the third pass to simulate a rework operation—as follows.

   Ramp-up rate: +3°C/second max.
   Temperature maintained at 125 ±25°C: 120 seconds max.
   Time at maximum temperature: 10–20 seconds
   Maximum temperature: 235+5/–0°C
   Ramp-down rate: –6°C/second max.

Temperature Cycling

Temperature cycling is designed to simulate stress that the device may experience at temperature range of –40°C to 150°C for 1000 cycles, at a rate of 3 cycles/hour.

HAST

Highly Accelerated Stress Test (HAST) is design to accelerate possible corrosion, delamination, possible wirebond failure, and intermetallic growths. HAST is performed at constant temperature and relative humidity for a duration of time. Example: 110°C/85% unbiased for 264 hours.

Thermal Shock

Thermal shock test the integrity of the device under extreme temperate gradients.

Data Retention Bake

This test ensures that the device loses no data. Test is performed at constant temperature with a specific duration, example, 150°C for 168 hours.

HTOL

High Temperature Operating Life (HTOL) is sometimes refer to as Infant Mortality. This test is used to weed out any early life failures and is typically performed for 168 hours at 150°C.

Latch-up

To withstand accidental shorting, all the device pins must meet the specification requirements to withstand up to 200 mA stress from –1 V to V_{CC} + 1 V.

ESD

Electrostatic Discharge (ESD) test the sensitivity of the device. Two kinds of ESD tests are:

HBM: Human Body Model simulates the ESD event from a human finger to a pin

CDM: Charge Device Model simulates the spark between a single pin of a charged leadframe and a metallic ground.

Component level testing consists of but is not limited to the above accelerated tests. As it is not feasible to monitor the reliability of each device types that AMD produces, device representative and extend of test are selected based on complexity of wafer fabrication process and package type.

FBGA-BT Component Level Test Results

Package Qualification Data—Contingent Release

Package: Fine Pitch BGA (FBGA-BT)

Package Body Size: 8 x 9 mm

Product: Am29LV160, 16 Mb Flash

Test	16 Mb FBGA-BT 8 x 9 mm package
Preconditioning JEDEC Level 3 235+5/-0 degrees	0/448
Temp cycle (-40 to 150°C) T = 1000 cycles	0/150
HAST (110°C/85%) unbiased T = 264 hrs	0/150
Thermal Shock T = 15 cycles	0/32
Data Retention Bake T = 168 hrs	0/195
HTOL T = 500 hours	0/150
Latch-up	Pass
ESD-HBM ±1.1 kV	Pass

Chapter 9: Board Level Characterization Studies

As part of an internal characterization study and ongoing product improvement program, AMD has conducted board-level testing of the FBGA package for Flash memory.

The testing includes copper lead frame TSOP as a benchmark. As of late January 1999, the results are as follows.

16 Mb FBGA-BT (ASE)	
Test: **0/100°C**	
Cycles completed: **7847**	
Sample size: **54**	
Failure #	**Cycle #**
1st	5800
2nd	6521
3rd	6581
4th	7312
5th	7512
6th	7512
7th	7662

16 Mb TSOP I 48-Pin	
Test: **0/100°C**	
Cycles completed: **7847**	
Sample size: **40**	
Failure #	**Cycle #**
1st	5560
2nd	5708
3rd	5868

AMD intends to continue the testing until 63% failures occurs or until 9,000 cycles are completed, whichever occurs sooner.

Experimental Design and Procedure

Board Design

CSP test boards were designed to have six packages (of one package type) on each board, to ensure adequate spacing between adjacent packages. Space considerations limited the TSOP boards to four TSOPs per board. On each board, half the packages were oriented at 90° to the other half. These precautions ensure that the data collected is free of any effects of location / orientation.

All the packages have a daisy chained die in them. The daisy chain circuit is completed on the board level so that each package consists of a single net. Any failure on any solder ball can be immediately captured as a break in the daisy chain.

The board is 20 mils thick, which replicates the construction of a standard PCMCIA card.

Board Fabrication

Standard printed circuit board (PCB) processes were used in the fabrication of the boards.

Materials

Most of the laminates for PCBs in the industry are produced using epoxy resins. The choice of epoxy resin is made because of its outstanding electrical, mechanical, and thermal properties. FR-4 epoxy fiberglass laminate is the standard for all high technology and professional electronic assemblies, and is the material selected for this study.

Design Parameters

Pad defined land pattern for the CSPs was chosen in order to achieve a good interface between the solder balls and the PCB pads. The circular pad has a diameter of 12 mils, and is dipped with eutectic 63Sn/37Pb solder with thickness of 0.5 to 0.8 mils. The clearance (or spacing) between solder mask and pads is 3 mils; and the registration is +/- 2 mils. No solder mask is allowed on the pads. Liquid photo imageable solder mask is coated over base Copper with maximum thickness of 3 mils. 5 mil nominal trace width is used for all trace routing.

Assembly of Packages

The test boards were not panelized during assembly. Only one piece of board was on each panel. Fixtures were used at all stages of the process, including printing. The boards were taped onto the fixtures using Kapton tape. No clean process was used for this study because the stand off height for CSPs is very low, and cleaning and drying under the CSP package could lead to contamination.

Solder Paste Screen Printing

DEK 265Lt screen printer with 300 mm metal squeegee was the equipment used for the solder paste printing process. LR737 rosin, a no-clean paste from Alpha Metals was used for the study. It is designed for stencil application in surface mounting process where post reflow cleaning is not required. It has mesh size of –325, which is equivalent to a particle size of less than 45 µm diameter.

The key criteria of stencil performance are vertical wall straightness, wall smoothness and dimensional precision. Laser cut stencils were used, since the laser cutting processes can produce stencils with smooth and straight vertical walls.

While screen printing solder paste, the stencil thickness and aperture dimensions are combined to achieve a balance between printing resolution and the avoidance of either starved solder joints or pad bridging. The stencil was designed to have a thickness of 3 mils and aperture of 12 mils in this study.

During the solder printing process, visual inspection for smear, slump, missing, and bridging is performed for each board. Paste height at random locations is measured through scanning laser microscopy (LSM) for one of every five boards. The average paste height is controlled at 3.6 mils with deviation of 0.3 mils.

Convection Reflow

The Heller 1800, a forced air convection reflow system was used in the assembly of the boards.

High concentrations of Oxygen (if using air reflow) can degrade the components due to oxidation when they are at elevated temperatures. In particular, the problem of combustion of the flux in air gives rise to only a small available process-temperature window for the reflow process. Using Nitrogen can significantly eliminate the oxidation of the parts and extends the available process-temperature window for the test boards and fluxes. Therefore, Nitrogen was used for the reflow process.

AMD preferred to control the Oxygen level below 20 ppm during the reflow process. However, there was no Oxygen analyzer available at the contractor manufacturer site to measure the actual Oxygen level when processing AMD test boards. We can only state at this time that the maximum Oxygen level was 100ppm during reflow.

The reflow profile characteristics were as follows:

- Ramp to 110°C with rate of 1.2°C/sec.
- Dwell between 110 and 135°C for 90 seconds.
- Maintain time above liquidus (183°C) for 45 seconds.
- Reach peak temperature at 213 to 215°C.
- Cool down with ramp rate of 1.5°C/sec.

Stress Testing

The assembled boards were subjected to temperature cycling. This is the appropriate stress test to accelerate the wearout failure mechanism being investigated which is solder joint fatigue, primarily driven by coefficient of thermal expansion (CTE) mismatches.

The 0/100°C temperature cycling range is the most commonly used test condition in the industry for the board level reliability assessment of CSPs and it accelerates the correct failure mechanism. It is also probably going to be the future High Density Packaging Users Group (HDPUG) standard, and there is consensus among North American users and manufacturers for this test condition.

The exact temperature profile used was:

- 30 min cycles
- 10 min ramp up/down
- 5 min soak at hot and cold temperatures

This profile is again consistent with the future HDPUG standard for CSPs.

Test Procedure

The following is a brief description of the various steps involved in carrying out the board level temperature cycling experiment.

Initial Resistances / Harnessing

The initial resistance values of each of the nets (each package forms a single net) being monitored are recorded. These resistance values serve as the baseline. Any packages that are open at Time-Zero are not considered in the experiment. This can occur due to manufacturing or assembly defects. In this study however, there were no Time-Zero failures. The individual boards are then harnessed, so that they can be connected to the event detection equipment. Harnessing is essentially the soldering of Teflon coated ribbon wire to the end connectors on the test boards.

Temperature Cycling Chamber Profiling

This is done to ensure a uniform temperature across the different boards in the chamber. The Fluke Hydra Data Bucket is used to collect the thermal mapping data. Measurements are made on three boards (top, middle, and bottom). On each board, measurements are made at three locations, i.e. the two sides and the center. These precautions ensure that all the boards are subjected the exact temperature cycling profile conditions.

Event Detection / Continuous Monitoring

The AnaTech LY515 (Analysis Technology) 256 channel event detector is used to monitor the nets in real time. Event detectors detect resistance spikes over some preset resistance level. Any instance of measured resistance value exceeding the threshold resistance value shall be considered as OPEN. An OPEN followed by 10 additional OPENS within 10% of the time of the first OPEN shall be considered as a FAILURE and the TIME TO FAILURE shall be the time at which the first OPEN occurred. This is to avoid any measurement glitch or noise.

Test Strategy

Data collected includes the number of failures, if any, cycles to failure and their location (specific board, specific net, etc.). It is intended to continue the tests to approximately 63% failure. At the completion of the testing, the failed units will be analyzed by microsectioning to confirm the validity of the failures.

Chapter 10: Miscellaneous

Shipping Container Information

Up to date shipping container information for the FBGA package can be found at the AMD web site: IC Packages and Packing.

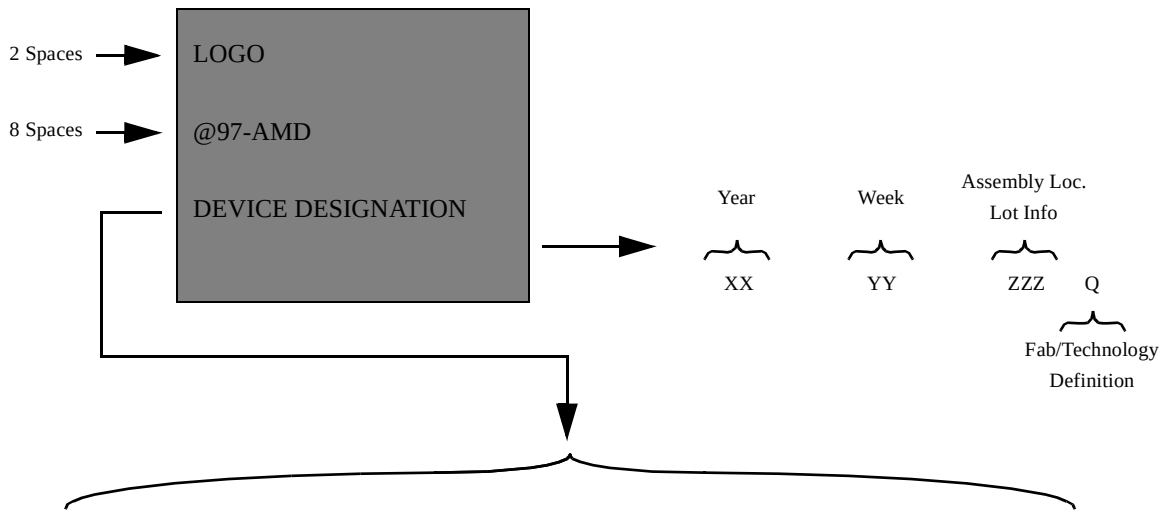
http://www.amd.com/products/packaging/toc.html

Sockets for FBGA-BT Packages

Vendor	SOCKET
	FBGA 6x9 mm
Wells	Open Top # 703-1048-07
	FBGA 8x9 mm
Wells	Open Top # 703-1048-04 Rev A
Yamaichi	Open Top # NP351-04878 Rev C
	FBGA 8x14 mm (63 Balls)
Wells	Open Top # 703-1063-01
Yamaichi	Open Top # NP351-06377-N

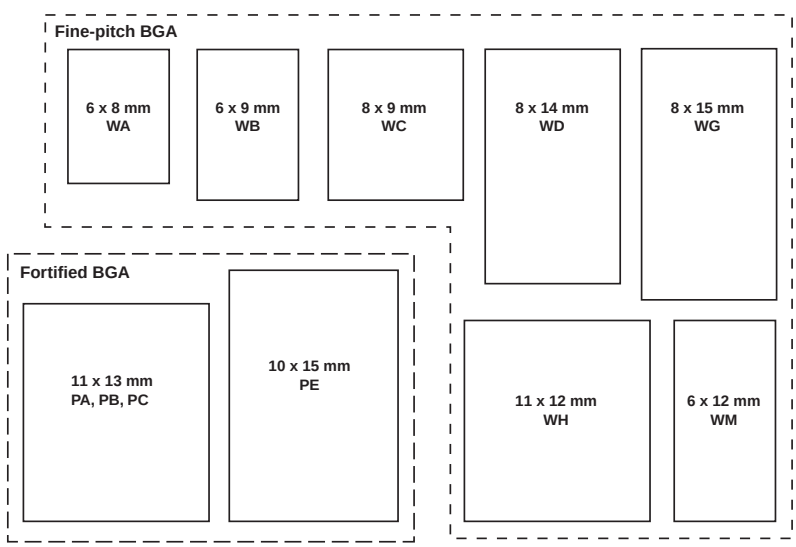
* Closed top socket may be available. Contact socket vendor.

FBGA Package Marking



Architecture and Voltage	Density and Sector Org.	Technology	Boot or Uniform	Speed (ns)	Voltage Range	Temp. Range
L = LV D = DL F = F S = DS	400 800 017 160 162 163 033 322 323 640	B = 0.32µm/CS39S C = Thin Oxide 0.32 µm/CS39LS D = 0.23 µm/CS49S	T = Top B = Bottom U = Uniform	55 70 80 90 12 = 120 15 = 150	R = Regulated V = Full	C I E

FBGA Package Designators



Note: These package codes are not marked on the package — for ordering purposes only.

Appendix A: Article Reprints

RELIABILITY EVALUATION OF CHIP SCALE PACKAGES

Ranjit Gannamani, Viswanath Valluri, Sidharth, and MeiLu Zhang
Advanced Micro Devices
Sunnyvale, California

ABSTRACT

This paper evaluates various Chip Scale Packages (CSP's) with respect to board level reliability under accelerated temperature cycling stress tests. The solder joint reliability of three different types (based on substrate material) of Fine Pitch Ball Grid Array (FBGA) packages and the MicroBGA package is compared. The results are analyzed using Weibull data analysis and extrapolated to low cumulative percentage fails. The effect of package and board design parameters such as solder ball size and board thickness is also presented.

Key words: CSP, BGA, FBGA, solder joints, reliability.

INTRODUCTION

The goal of smaller and portable electronic products is driving the development of CSPs. CSPs are close to the die size and are much smaller than conventional packages. In 8Mb density Flash memory for example, a TSOP48 (Thin Small Outline Package) measures about 18.4mm x 12mm whereas a comparable CSP (FBGA) would measure only 6mm x 9mm.

Often, different CSPs offer similar reliability at the component or package level. Once they are mounted on boards, their 'second level' or 'board level' reliability could however be very different, and is based on the unique material set and construction of each package type. This study was undertaken to evaluate (i) the board level reliability of some CSPs of different construction, and (ii) the effect of package and board design parameters such as solder ball size and board thickness.

PACKAGES EVALUATED

The following packages were evaluated: (i) FBGA with Polyimide (PI) tape substrate, or FBGA-PI, (ii) FBGA with BT (Bismaleimide Triazine) substrate, or FBGA-BT (BT is the rigid epoxy glass laminate used in the conventional plastic ball grid arrays), (iii) FBGA with ceramic substrate, or FBGA-Cer, and (iv) MicroBGA. Each package has a different material set and structural construction.

Figure 1, Figure 2 and Table 1 illustrate the key differences between the various FBGAs. The FBGA-PI uses a thin 0.08mm PI tape substrate, while the FBGA-BT uses a relatively thick 0.36mm BT substrate. Both packages conform to the same overall package height of ≤ 1.2mm, which is the maximum package body height specified in the JEDEC FBGA specification. Consequently, the FBGA-BT uses 0.3mm solder balls while the FBGA-PI uses 0.4mm solder balls. The differences between the physical dimensions of the FBGA-Cer and FBGA-BT are minimal.

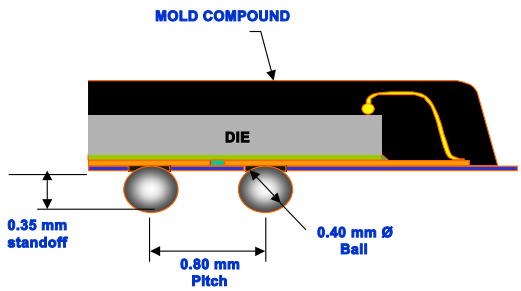


Figure 1. Cross-section of FBGA-PI

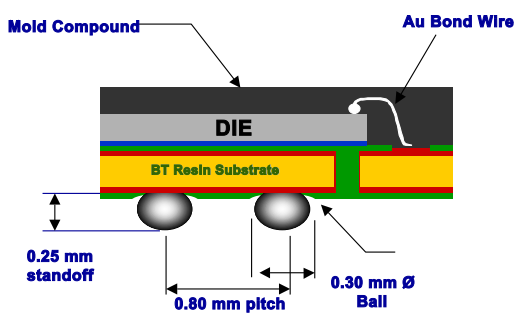


Figure 2. Cross-section of FBGA-BT

	FBGA-PI	FBGA-BT	FBGA-Cer
Ball size	0.4mm	0.3mm	0.3 mm
Solder	eutectic	eutectic	eutectic
Substrate thickness	0.08 mm	0.36 mm	0.35 mm
Substrate material	Polyimide	BT resin	Alumina
Die thickness	0.3 mm	0.26 mm	0.26 mm
Avg Pkg height (measured) when mounted on boar	0.96 mm	1.07 mm	1.18 mm

Table 1. Differences in FBGA construction

The basic construction of these FBGA packages is to some extent similar to that of conventional ball grid arrays. The MicroBGA (Figure 3) however has a unique construction. It uses a compliant elastomer material between the die and the polyimide tape. TAB type beam leads are bonded onto

the die, and the die is 'face down' and exposed on the back side.

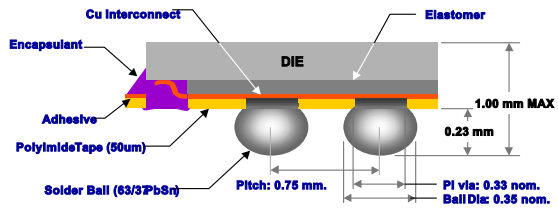


Figure 3. Cross-section of MicroBGA

TEST BOARDS

Each FR-4 test board measured 3.5" x 2". Both 20mil and 62mil boards were used in this study. Six CSPs were assembled on each board (Figure 4). On each board, half the packages were oriented at 90 degrees to the other half, and precautions were taken in the layout of the board to ensure that the data collected is free of any effects of location or orientation. The boards had Non Solder Mask Defined pads with a HASL finish. Standard best practices such as no-clean solder paste, laser cut stencils, and Nitrogen convection reflow were used in the assembly of the CSPs on the boards. Each CSP contains a daisy chained die. The daisy chain circuit is completed on the board such that each package consists of a single net through all the joints.

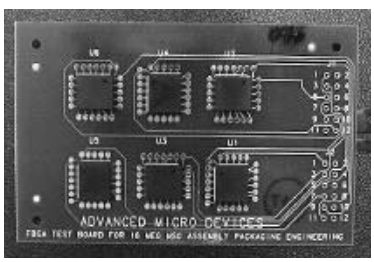


Figure 4. A typical CSP test board

TEMPERATURE CYCLING

A 0°C to 100°C, 30 minute single chamber air-to-air temperature cycling profile with 10 minute ramps and 5 minute dwells was used. This is one of the commonly used test profiles in the industry. An event detector was used to monitor the daisy chained test boards in real time. The event detector was set to record resistance spikes greater than 300 ohms for 200 nanoseconds. Any spike greater than 300 ohms was considered as "open". A package was considered failed when the first open was followed by 10 additional opens within 10% of the time of the first open. The thermal cycling chamber was profiled before starting the test, to ensure a uniform temperature across the different boards in the chamber. Wherever possible, the tests were continued to 63% fail or greater.

MODELING TECHNIQUE

After temperature cycling was completed, the failure data was fitted to a Weibull statistical distribution. The Weibull parameters α ($N_{63.2\%}$) and β (slope) were obtained for the test, and the data extrapolated to a low cumulative failure percentage (100 PPM). The test data was then extrapolated to field use conditions and the projected field life (at 100 PPM) calculated, in order to enable a more intuitive comparison of the reliability of the different packages. The Norris-Landzberg modified Coffin-Manson equation [1] was used to calculate the acceleration factor. The two example field conditions used in this paper are shown in Table 2.

Example Field Conditions	
Temperature Swing	**Cycles / Day**
40 C / 60 C	1
-15 C / 25C	1

Table 2. Example field conditions

RESULTS

Extensive temperature cycling data on the different CSPs was collected. The test program included various experimental splits with different combinations of package and board types. For clarity, the presentation of the results has been divided into the following five sections.

(A) Comparison of Different Package Types

The Weibull plots for the 8x9mm FBGA-BT, 8x9mm FBGA-PI, MicroBGA, and 6x9mm FBGA-Cer are shown in Figure 5. Here, the FBGA-Cer CSP contains the 8Mb density Flash device, while the other three CSPs contain the 16Mb density Flash device. This data was collected on 20mil (0.5mm) boards under 0/100 degC cycling.

The Weibull slope and cycles to 63.2% failure (N63.2%) are shown in Table 3. The Weibull plots show that the FBGA-BT and MicroBGA packages have significantly larger N63.2% values than the FBGA-PI and FBGA-Cer packages. It is too be noted that the initial MicroBGA failures are not solder joint failures and a discussion follows in a later section. From Figure 5 and Table 3, it can be seen that the slope of the distribution is different for various sets of data and hence a direct comparison of N63.2% fails is not feasible for the whole set of data. It is pertinent to compare the results at low PPM cumulative percentage failure mark. Hence, the 100 PPM number, which seems to be a very conservative number accepted in the industry, was chosen. Figure 6 shows comparative life projections in the two example field conditions defined in Table 2.

In termsof board level reliability, it can be seen from Figure 6 that the FBGA-BT and MicroBGA ranked much higher than the other packages. Both these packages demonstrated

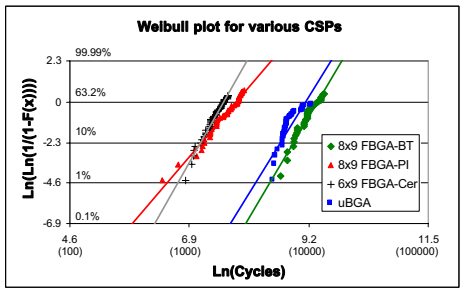


Figure 5. Weibull plots for various CSPs

Package	N63.2 (cyc)	Beta	# fails / SS
8x9 mm FBGA-BT	11586	5.0	39 / 48
8x9 mm FBGA-PI	2295	3.9	52 / 60
6x9 mm FBGA-Cer	1918	5.2	46 / 60
MicroBGA	9240	4.8	35 / 60

Table 3. Weibull parameters for various CSPs

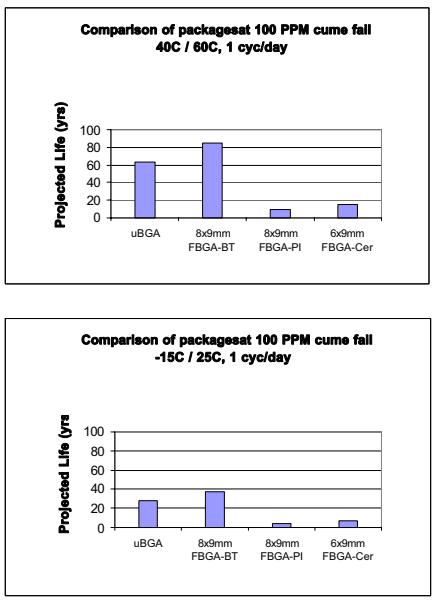


Figure 6. Field life projections

lifetimes considerably higher than the requirements of most customer applications. The 8x9mm FBGA-PI and 6x9mm FBGA-Cer data translated to lower field life projections. The life projections in "years" shown in Figure-6 are for those two specific field conditions only. The estimation of lifetimes would vary depending upon the specific field conditions and the model used to calculate the acceleration factors between test and field. However, the key observation to be made is that the relative size of the different bars is a true representation of the comparative reliability of the different CSPs at the board level.

The higher reliability of the FBGA-BT package can be attributed to the thick and rigid BT substrate isolating the silicon die (low CTE) from the solder joint and the board. In the case of the MicroBGA package, the compliant elastomer material isolates the silicon die from the solder joint and the board, and contributes to the high reliability. The comparatively lower reliability of the FBGA-PI is due to the fact that the package construction is dominated by the low CTE Silicon die. As seen in the package cross section, it is only the die attach layer and the Copper traces on the PI substrate that separate the solder ball from the die. The PI tape itself is not in the path; it has openings that define the pads for ball attachment. The lower reliability of the FBGA-Cer packages was expected since there is both global and local CTE mismatch with the FR-4 board. A potential use of this package might be on Ceramic boards, but that issue is not discussed in this study.

On completion of the tests, failure analysis was carried out on a sample of the test vehicles. Figure 7 shows micro-sections of the FBGA-PI and FBGA-BT test boards. Solder joint cracks at the interface on the component side are seen. This is consistent with the classic BGA solder joint failure mechanism that is well documented in the literature. Figure 8 shows the results of the failure analysis on some of the initial MicroBGA failures. A lifted beam lead was detected. The isolation of the low CTE die by the compliant elastomer results in the beam leads absorbing most of the cyclic fatigue stress in temperature cycling.

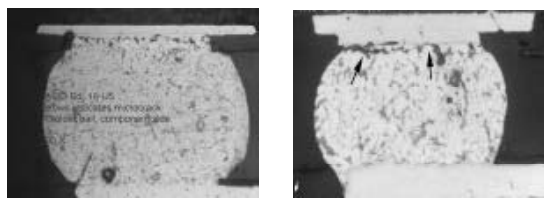


Figure 7. Failure analysis of FBGA-PI (left) and FBGA-BT (right). Cracks on component side.

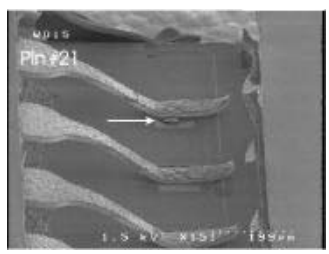


Figure 8. Failure analysis of MicroBGA

In these experiments, the FBGA-BT packages (0.3mm solder balls) were assembled on test boards that were initially designed for the FBGA-PI package (0.4mm solder balls). The test boards were designed to have 0.3mm pads that matched the 0.3mm openings in the PI tape (where the solder balls are attached) of the FBGA-PI package. The corresponding opening in the solder mask of the FBGA-BT package is 0.25mm. It is hence expected that the use of test boards designed or optimized for the FBGA-BT package could result in even better FBGA-BT data than that presented here.

(B) Effect of Package Body Size in FBGA-PI

The FBGA-PI test discussed in the earlier section was on the 8x9mm body size, which is the package for the 16Mb density Flash product. The 6x9mm FBGA-PI, the package size for the 8Mb density device, was also put on the 0/100 degC test. In this case also, 20mil test boards were used. Figure 9 shows the Weibull plots for both the 8x9mm and 6x9mm FBGA-PI packages. The relevant Weibull parameters are in Table 4 and field life projections in Figure 10. As seen in the Weibull plots and the field life projections, the larger 8x9mm package demonstrated a lower lifetime than the 6x9mm package. This difference is attributed to the larger package body size and the larger die size of the 16Mb device, i.e. the domination of the low CTE Silicon die is more pronounced in the larger package for the higher density Flash product. Based on these findings, it was anticipated that even larger packages for higher density products (32/64Mb) would show poorer solder joint lifetimes in the FBGA-PI package due to the same reasons.

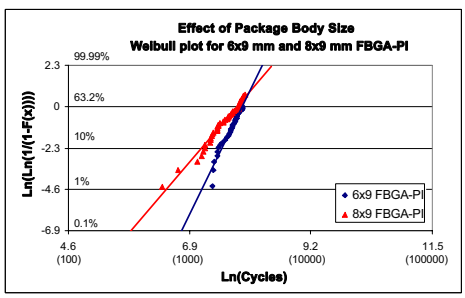


Figure 9. Effect of package body size in FBGA-PI

Package	N63.2 (cyc)	Beta	# fails / SS
8x9 mm FBGA-PI	2295	3.9	52 / 60
6x9 mm FBGA-PI	2685	6.0	38 / 60

Table 4. Weibull parameters for different body sizes

(C) Use of Larger Solder Balls on FBGA-PI

Design / package changes to improve the board level reliability of the FBGA-PI were investigated. Design parameters that may impact the board level reliability are substrate material, substrate thickness, mold compound

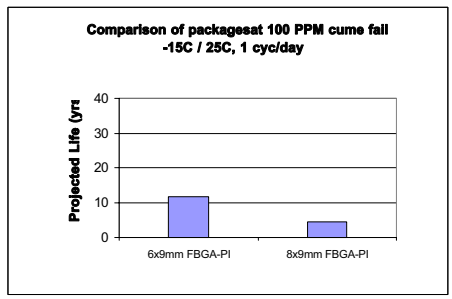


Figure 10. Field life projections

material, die attach compliancy, solder ball size, etc. The package design variable evaluated here was solder ball size. The solder ball size on the initial FBGA-PI package was 0.40mm nominal. This ball size was increased to 0.45mm nominal. Though the ball size was increased, the overall height of the package was maintained below 1.2mm. The PI tape opening was increased from 0.3mm to 0.38mm. The new test boards had 0.35mm pads. Based on industry practice, this was deliberately maintained a little smaller than the 0.38mm PI tape openings on the new FBGA-PI package.

Figure 11 shows the Weibull plots for both the 0.4mm ball and 0.45mm ball FBGA-PI packages. The relevant Weibull parameters are in Table 5. Figure 12 shows the field life projections for the FBGA-PI packages with 0.40mm and 0.45mm solder balls. As expected, the use of the larger solder balls results in an improved solder joint lifetime.

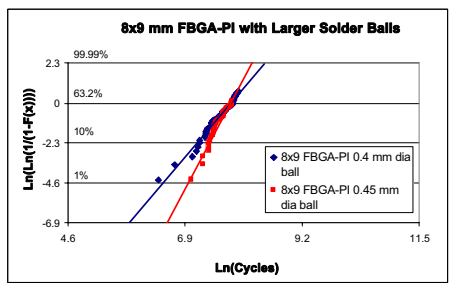


Figure 11. Use of larger solder balls on FBGA-PI

Package	N63.2 (cyc)	Beta	# fails / SS
8x9 mm FBGA-PI, 0.40 ball	2295	3.9	52 / 60
8x9 mm FBGA-PI, 0.45 ball	2424	5.5	40 / 60

Table 5. Weibull Parameters for solder ball size

From the Weibull plots it can be seen that it is challenging to quantify the improvement due to the use of larger solder

balls. While the N63.2% values are relatively close, the different slopes tend to amplify the difference between the two datasets, especially when projected to lower PPM. For example, if a 1000 PPM criterion is used, the improvement obtained (of 1.8X) is significantly lower than that shown in Figure 12 (2.1X). To get an average picture of the whole data the slopes from the two datasets were pooled to obtain a common slope of 4.7, and an N63.2% fitted to both datasets. Now comparing N63.2% values results in an improvement of 1.13X with the use of larger solder balls.

From this analysis it is seen that even in a best case scenario for the larger solder balls, the improved lifetime is still lower than that of the FBGA-BT and MicroBGA packages.

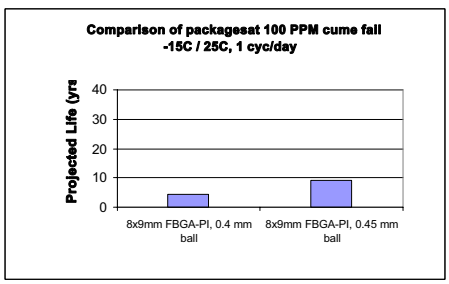


Figure 12. Field Life Projection

It should also be noted that at 0.45mm, the solder ball size is quite close to the maximum possible for the solder ball array with a pitch of 0.8mm, in order to retain sufficient room to route traces to internal solder balls. Additionally, the eventual move to a 0.5mm pitch solder ball array (necessitated by shrinking die sizes due to improved fab processes, and the need for smaller form factor packages) will make the use of a 0.45mm ball impossible. The FBGA-BT package that currently uses 0.3mm solder balls would be able to transition to a 0.5mm solder ball pitch without requiring a change in ball size.

(D) Evaluation of Test Vehicles built on 62 mil Boards

All the data discussed in earlier sections was collected on test boards that were 20mil thick. Testing (0/100 degC cycling) was also carried out on 62mil (1.6mm) boards to evaluate the effect of these thicker boards on the solder joint lifetimes. Figure 13 shows the Weibull plots for the 6x9mm FBGA-PI on both 20mil and 62mil boards. Figure 14 shows similar plots for the 8x9mm FBGA-BT package. The relevant Weibull parameters are listed in Table 6. It should be noted here that the FBGA-BT / 62mil board data presented here is preliminary. This will be updated as more failures are collected.

It can be seen from Figure 13 that the same challenge of quantifying the difference (as outlined in the previous section) exists for these two sets of FBGA-PI data as well. Using the technique of pooling to a common slope of 7 and recomputing the N63.2% values, it is found that on an average, the solder joint life on thinner board exceeds that on the thicker board by 1.34X for FBGA-PI package. The slope (beta) for the thicker board was higher than that for thinner board, and so projections to a low PPM value showed minimal difference (Figure 15).

For the FBGA-BT package the results are preliminary as the tests on 62mil boards are still in progress. Initial data shows minimal difference as the failures obtained so far have lined up on the existing data on the 20mil boards (see Figure 14 and preliminary life projections in Figure 15).

It should also be noted that that the 62mil boards were assembled at a different site. Hence, while these may not be exact comparisons the information presented is still useful to demonstrate that there is no significant difference in the lifetimes projected even when the same packages are assembled on thicker boards.

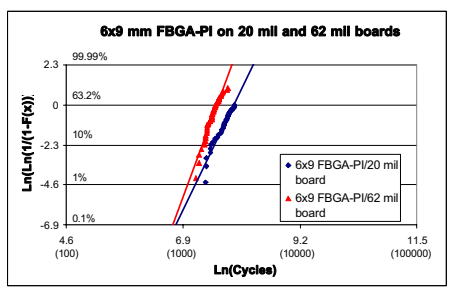


Figure 13. FBGA-PI on 20 and 62mil boards

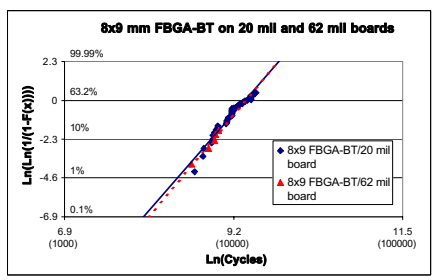


Figure 14. FBGA-BT on 20 and 62mil boards

Package	N63.2 (cyc)	Beta	# fails / SS
6x9 mm FBGA-PI, 20mil board	2685	6.0	38 / 60
6x9 mm FBGA-PI, 62mil board	1932	7.9	45 / 48
8x9 mm FBGA-BT, 20mil board	11586	5.0	39 / 48
8x9 mm FBGA-BT, 62mil board	11757	5.2	5 / 30

Table 6. Weibull parameters

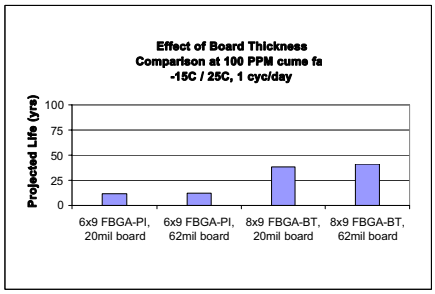


Figure 15. Evaluation on 62mil boards

(E) Temperature Cycling at -40 / 100 degC

A limited amount of data was also collected at the -40/100 degC, 30 minute cycle test condition on 20mil boards. Table 7 is a summary of that data. The 8x9mm FBGA-BT and the 8x9mm FBGA-PI packages were evaluated. The test was terminated at 2507 cycles. At that point, there were zero fails (0/60) of the FBGA-BT test vehicles and extensive failures (49/60) in the FBGA-PI test vehicles. While no field projections are included here, this information again gives an indication of the relative robustness of the two packages.

Test Condition: -40 / 100 degC		
	8x9 FBGA-BT	8x9 FBGA-PI
Cycles completed	2507	2507
Data	No fails out of 60	49 fail out of 60
First fail at:	n/a	754
Test status	Stopped	Stopped

Table 7. Board Level Reliability Data at –40/100 degC test condition

CONCLUSIONS

(i) In the packages evaluated, the FBGA-BT and MicroBGA demonstrated lifetimes considerably higher than the FBGA-PI and FBGA-Ceramic packages. These differences in board level reliability can be explained by the differences in package construction and material sets.

(ii) In the FBGA-PI package, the larger 8x9mm package for the higher density 16Mb device (larger Silicon die) demonstrated lower reliability than the 6x9mm package for the 8Mb device. Based on this trend, it was anticipated that even larger packages (for 32/64Mb) would show lower solder joint lifetimes in the FBGA-PI construction.

(iii) The use of the larger solder balls (0.45mm vs. 0.4mm) on the FBGA-PI package resulted in an improved solder joint fatigue life. Even in the best case scenario for the larger solder balls, the improved lifetime was still lower than that of FBGA-BT and MicroBGA packages. Feasibility of using a 0.45mm ball size would be challenged as migration to 0.5mm ball pitch is made.

(iv) At 100 PPM no significant difference in the board level reliability was detected for both the FBGA-BT and FBGA-PI packages assembled on the thicker 62mil boards when compared to those mounted on the 20mil boards.

(v) Limited data at the -40/100 degC test condition indicates the relative robustness of FBGA-BT over FBGA-PI with respect to board level reliability, that is consistent with the rest of the 0/100 degC data discussed in this paper.

ACKNOWLEDGMENT

The authors would like to acknowledge Melissa Lee, John Hunter, Bruce Schupp, James Hayward, and Ed Fontecha for their guidance and support, Dave Morken for the SEM analysis and Robert Dudero for cross-sectioning of the samples.

REFERENCES

[1] K. Norris and A. Landzberg, IBM Journal of Research and Dev, 13, pp 266, 1969.

[2] K. Ano, et al, "Reliability study of the chip scale package using flex substrate", SMI Proc, pp44-47, 1997.

[3] R. Darveaux, J. Heckman, A. Mawer, "Effect of test board design on the 2nd level reliability of a fine pitch BGA package", Proc of SMI, pp 105-111, 1998.

[4] C.F. Coombs Jr., "Printed Circuits Handbook", McGraw Hill, NY, 1995.

THE CSP OF CHOICE

FBGAs

FOR FLASH MEMORIES

MSG

2000

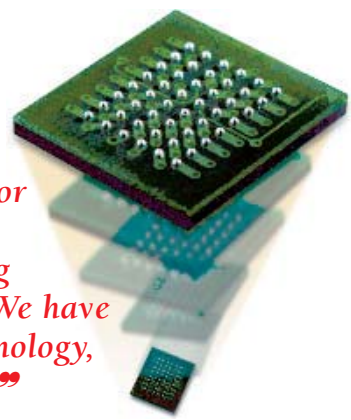
a publication of the manufacturing services group

AMD

AMD RECENTLY PLAYED A pivotal role in the emergence of the FBGA (fine pitch ball grid array) as the new chip scale package (CSP) of choice for flash memory devices. This time two years ago, the micro ball grid array (µBGA) was the only CSP available for downsizing from the larger, traditional leaded packages used for flash memories (such as the thin small outline plastic (TSOP) package). That changed last year when AMD began offering an FBGA design that afforded so many advantages, it put a fork in the package roadmap for flash memories in automotive, telecom, and new consumer product applications (e.g., cellular phones, pagers, hand-held computers, etc.). As this story unfolds, you will see how AMD persevered in the face of an established preference for Intel's µBGA to win overwhelming acceptance of the FBGA as the preferred CSP in these applications.

PACKAGE SIZE MATTERS

In applications where miniaturization is a priority, CSPs are a crucial stepping stone on the way to direct chip attach (DCA), in which the die is bonded directly



"When it comes to package technology for flash memories, AMD can do anything that can be done. We have the licenses, the technology, and the ability."

Bruce Schupp, NVD product marketing

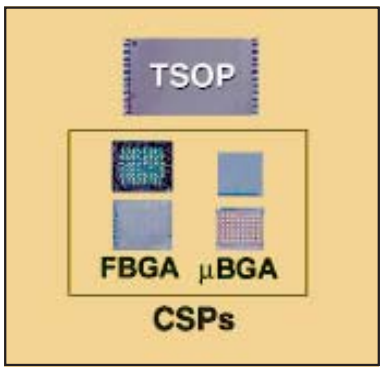


Figure 1 shows the smaller size of CSPs next to a comparable density TSOP.

to the end-use printed circuit board (PCB). While DCA technology offers the ultimate in miniaturization, the infrastructure for it is not established enough for DCA to be cost competitive. Moreover, DCA is not a viable option when the die has been designed for wirebonded interconnects (i.e., the bond pads are located around the periphery of the die), as is the case with all flash memories in traditional leaded packages. DCA is better suited for die having the bond pads in an array across the die surface, enabling the connections to be made with flip-chip technology instead of conventional wirebonding.

Figure 1 shows the smaller footprint of a CSP next to a comparable density TSOP. The smaller form/fit factor saves considerable board space and provides a lower profile – all of which is needed when trying to cram more memory capacity onto ever smaller motherboards, or in products striving to fit into the palm of your hand.

NOT JUST ANY CSP WILL DO

In addressing the demand for a flash memory CSP, AMD first looked at the µBGA, since market acceptance of it was already established. AMD's LV800 flash family was initially offered in a µBGA, and we shipped modest quantities of it. But these early µBGA package designs included polyimide tape embedded with solid gold traces for routing the signals from the die to the external terminals, and this was too costly. So we had the polyimide tape replaced with a copper core tape that had gold-plated copper traces ("beam leads") instead of solid gold. This flash gold was bondable and kept oxidation from growing, and the copper brought the costs down. We ran into a roadblock, however, when our supplier was unable to produce the copper core tape in sufficient quantities. It was a roadblock that soon proved to be a blessing in disguise.

Faced with no reliable, cost-effective CSP to offer flash customers, we turned to Fijitsu, AMD's FASL business partner. Fijitsu had an FBGA with a polyimide tape substrate that looked promising, so we got permission to adopt their package technology. Besides being cheaper than the µBGA, the FBGA construction was appealing because the package size could remain the same even if the die size became smaller. To better understand this, it helps to look at the configuration of an FBGA versus a µBGA.

µBGA CONSTRUCTION – ONE DIE SIZE ONLY PLEASE

The µBGA package is not like a standard IC package in which you attach a die. It is a construction that is built on top of the die, so the package is nearly the same size as the die itself. The cross-section drawing in Figure 2 shows the die-down configuration, interconnected by gold-plated beam leads to traces that route through the polyimide tape to an array of external solder balls.

This package construction presented a problem for AMD because of our die size. For many of the popular densities of the time, our die size was smaller than any other flash manufacturer's. While this is good for keeping fab costs down (more die per wafer), our die size was too small to provide room for the size of the solder ball array while keeping the pitch (the distance between the centerlines of adjacent solder balls) at a manageable 0.75 mm for board assembly. Moreover, even if our die could have fit initially, every time we implemented a die shrink we would face the

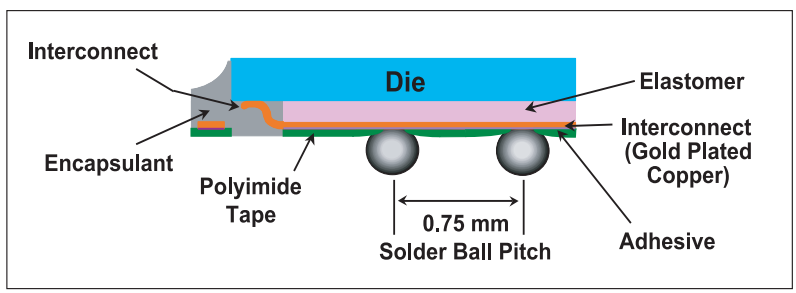


Figure 2 shows a cross-section of the die-down configuration of a µBGA package.

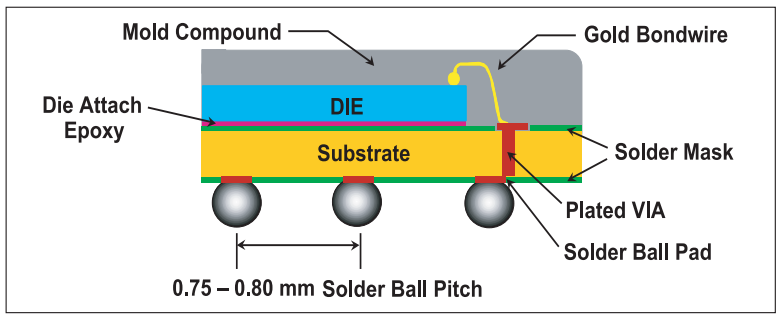


Figure 3 shows a cross-section of the die-up configuration of an FBGA package.

same size problem. Thus, with die shrinks occurring regularly, µBGAs are not an attractive CSP solution for flash memories – either for us or for our customers – because the form/fit of the package must change with every die shrink. This was becoming painfully apparent to several top-tier OEMs who were attempting to use the µBGA package for flash memories.

FBGA CONSTRUCTION – DIE SHRINK FRIENDLY

In the FBGA construction, the die is wirebonded to a substrate and then overmolded with epoxy, a construction very much like that of a standard BGA (see Figure 3). The minimum package size winds up being about 1.2 times the size of the die, slightly larger than a comparable density µBGA. But this size advantage wins no points when it comes to die shrinks. Because of the FBGA construction, it can do what the µBGA cannot: accommodate a reduction in die size with no change to the package dimensions. This renders a die shrink transparent mechanically to both AMD's and our customers' manufacturing lines – clearly, a win-win situation.

BUILDING INFRASTRUCTURE

For any new package technology, it is critical that there be a supporting industry infrastructure. We already knew that in the flash market OEMs want:

- the smallest, most powerful flash memory they can get in a package that has the largest pitch;
- multiple supply sources;
- package designs that do not change with every die shrink.

So we set our sights on qualifying the FBGA and on fortifying the infrastructure for it, the latter of which was no small task in a market where the µBGA was already synonymous with CSP. With no appreciable tooling or reliability data available at the time for the FBGA, we knew we needed to tackle these four prerequisites to market acceptance:

- board level reliability;
- board level rework ability;
- socket suppliers;
- alternative supply sources.

Board Level Reliability

We began testing the reliability of the FBGA after it was mounted onto a PCB similar to those in use by our major customers. We soon learned that the substrate of the FBGA – the polyimide tape – was too thin to absorb the stress incurred from the different CTE (coefficient of thermal expansion) rates of the silicon versus the PCB (using FR4 material). When heated, the PCB expands at a much higher rate than the silicon, and the package substrate has to manage this difference. Although the polyimide substrate proved reliable enough for many applications, it did not meet the long-lifetime reliability that is needed in commercial and industrial outdoor applications, such as in the telecommunications infrastructure or automotive environments.

Tape vs Rigid Substrate

While we were testing the tape FBGA, we also evaluated an FBGA design that had an organic substrate of BT (Bismaleimide Triazine) resin. Because this material was thicker and had a CTE closer to that of the PCB, it could better manage the stress than could the thinner polyimide tape. So we switched. The results of the extensive tests on the board level reliability performance can be found in the white paper, "Reliability Evaluation of Chip Scale Packages," published in 1999 by the following AMDers: Ranjit Gannamani, Vis Valluri, Sidharth Sidharth, and MeiLu Zhang. A copy of this paper can be obtained from MSD Engineering (x26415).

As for the µBGA, its board-level reliability performance is comparable to that of the FBGA due to the ability of its elastomer layer to absorb the stress from the different CTE rates. These reliability

results are also presented in the white paper referenced earlier.

■ Board Level Rework Ability and Socket Suppliers

NVD and MSD engineers teamed up to familiarize board-level rework companies with the FBGA package. They also worked with socket suppliers, for those customers who do programming prior to system assembly, to arrange support for AMD's FBGA package.

■ Alternative Supply Sources

NVD Marketing contacted some of our competitors and showed them footprints and pinouts for our flash memory parts. After negotiating some pinout changes, NVD got their commitment to support both the µBGA and the FBGA pack-age styles for the same flash memories. NVD also worked with the industry-wide JEDEC JC-42.4 Committee to establish AMD's version of the FBGA pinout as an official industry standard. Because of this, all FBGA packaged flash memories manufactured in the world today conform to the AMD footprint. We are continuing to work with JEDEC for the adoption of additional FBGA footprints designed to accommodate future generations of very high-density, high-performance flash memories.

THE FRUITS OF OUR LABORS

This infrastructure work took about a year to come to fruition and, because of AMD's success in this effort, FBGAs are now the most preferred CSP package for flash memories used in commercial and industrial applications. µBGA shipments still outnumber FBGAs due to the top two or three cellular telephone OEMs using them in large quantities; however, the number of OEMs now choosing FBGAs for flash far exceeds those preferring the µBGA. With AMD able to produce flash memory roadmaps knowing what the package footprint will look like years in the future, whether it be burst mode, page mode, or random access types of flash memory, even the OEMs committed to µBGA are now wanting FBGAs for future designs.

Thanks go to the following AMDers for their valuable contributions to this article and for the instrumental roles they played in bringing the industry around to embracing the FBGA: Bruce Schupp, Melissa Lee, Ranjit Gannamani, Vis Valluri, and Sidharth Sidharth. ◄

MSD Engineering

AMD

Memo on Ψ_{J-T}, Case Level Thermal Parameter

Introduction

A new thermal parameter has been developed by the EIA/JEDEC JC15.1 subcommittee on thermal phenomenon in electronic packaging. The parameter is called Ψ_{J-T}, (psi j-t) and is a modification and replacement of the much abused junction-to-case thermal resistance, θ_{JC}, value for plastic packages. This memo outlines the history and physical description of θ_{JC} measurements, and shows why they are poor performance indicators for plastic packages. The Ψ_{J-T} parameter is introduced and its use is explained.

History

θ_{JC} is a measurement that is used to describe the internal thermal resistance of a packaged semiconductor device. Originally, the measurement was developed as a method of calculating junction temperature (T_J) from a known reference point on the outside of the package. The natural place for this reference point is defined as "the shortest thermal path from the junction to the outside of the package," which is also the best heat sinking surface. In the days when the specification was generated, the mainstream package was the ceramic DIP, which for the military, were mounted onto 'cold rails'; flat liquid cooled tubes that contacted the bottoms of the DIPS in the application. These cold rails were held at a constant temperature and served as a reference point for calculating T_J.

The test method is performed by bringing the desired package surface to thermal equilibrium, an isothermal case condition at some defined temperature, by using a large cold plate or heat sink. The idea is to keep the external package temperature constant while the device is powered up. Heating voltage and current are supplied to the device to power up the die while keeping the package surface at the initial defined temperature. When the device comes to steady-state temperature and power conditions, the junction temperature is measured and junction to case thermal resistance is calculated using equation (1).

$$\theta_{JC} = T_J - T_R / P_D \quad (1)$$

where:

T_J = junction temperature
T_R = reference temperature (case)
P_D = Power dissipation

Heat Flow In Microelectronic Packaging

Heat flow in a hermetic package is well defined as illustrated in figure 1. In the diagram it is seen that the die is attached to a ceramic substrate inside of a cavity. When the package is assembled, the cavity is left intact, that is, only air or some other gas comes in contact with the die surfaces not bonded to the cavity. Since the thermal conductivity of the ceramic is

quite high when compared to air or other gasses, most of the heat generated (~90%) from the circuitry on the die surface is conducted through the silicon and into the ceramic substrate. The heat travels through the ceramic and is dissipated into the air or into a heat sink. Some spreading occurs in the ceramic (at an approximate 45° angle), so the analysis can be almost purely one-dimensional. This approach works well in any type of hermetic package including PGAs, CQFPs, CBGAs, and other ceramic packages.

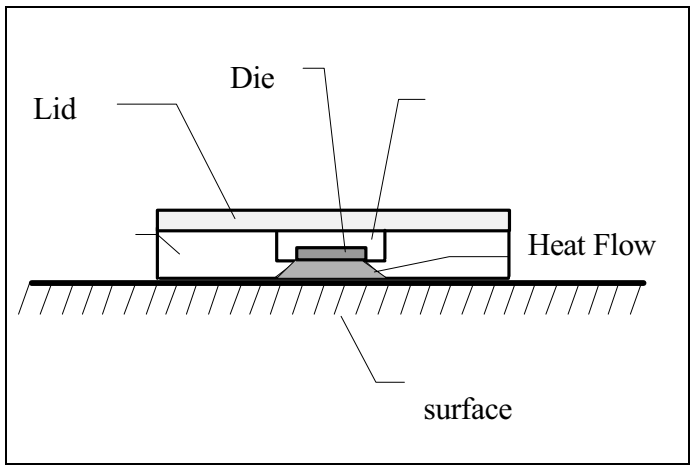


Figure 1. Heat Flow in Hermetic Package

When plastic packages gained popularity, much of the thermal analysis was left intact, such as the θ_{JA} (junction-to-air thermal resistance) parameter, and θ_{JC}. It was assumed, incorrectly, that the junction-to-case value could be used in plastic packages to predict junction temperature the same way it was used for hermetic packages. The problem with θ_{JC} for plastic packages is fundamental, and it is easily seen how the physical construction of plastic packages negates the use of this simple parameter.

Figure 2 shows the typical construction and heat flow in a plastic quad flat pack (PQFP). Heat flow paths are represented by a resistor network analogy in the diagram. As can be seen from the figure, heat flow in the plastic package is very complex when compared to the hermetic package. In plastic packages, the die is usually mounted onto a copper alloy die pad, wire bonded to the lead fingers which radially or orthogonally emanate from the die area, and is finally encapsulated in plastic moulding compound. Because the die is contacted on all sides by solid matter, heat can flow easily in a multitude of directions. Due to the copper alloy's high thermal conductivity, the heat immediately spreads into the die attach paddle, and subsequently into the lead frame. Some heat also flows into the moulding compound and is released by convection from the package external surfaces. It is due to this complex heat flow that θ_{JC} is ill defined for plastic packages.

Problematic θ_{JC} for Plastic

First, the shortest thermal path is difficult to determine. If the package is thin, and the die paddle is close to the exterior of the package, this may be the shortest path. On the other hand, if the lead fingers are close to the die paddle, the most direct path may be through the lead frame and into the printed circuit board(PCB). The latter of these two possible paths

is more likely, but in any case, the external environment plays a crucial role in the thermal performance of plastic surface mount devices. As an example, if the PCB is relatively low in thermal conductivity, e.g. no internal planes and minimized metal traces on the surface, then the shortest path may well be through the bottom of the package. But, if the PCB has internal voltage and heat spreading planes, the leads may dominate the heat flow. Secondly, how are these surfaces made to be isothermal as to satisfy the original intent of the ceramic based measurements? It was believed that using a well stirred fluid bath with a fluorinert liquid would force all surfaces on the plastic package to an isothermal state. Due to the nature of stirred fluids, the measurement breaks down to a moving fluid measurement and the package surfaces are not isothermal. Recently methods have been developed to use jet impingement to create high heat transfer coefficients on package surfaces, very nearly creating the isothermal specification. Although these methods are useful for creating specific boundary conditions for conduction models, the measurement is still not useful for predicting junction temperature from a known package temperature.

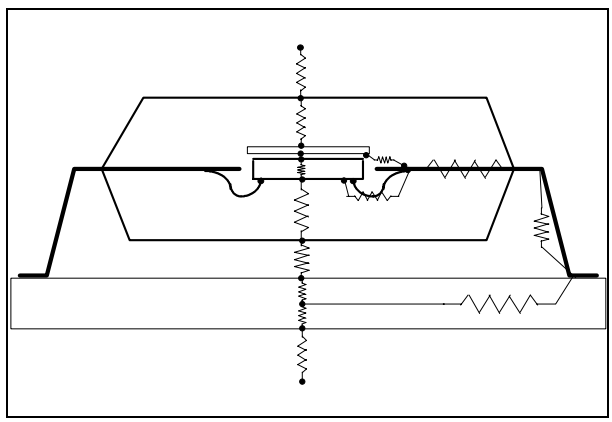


Figure 2. Heat Flow in Plastic Packages

Customer Use

Through the years, the real identity of θ_{JC} was diluted, and today most system houses predict temperature by placing a thermocouple on the package surface and using the manufacturer's published θ_{JC} values to compute junction temperature. This is a fallacy and is wholly inaccurate. Today, it is an all too common practice and is accepted as correct. For hermetic packages, the correct method is to install a heat sink on the surface identified as the isothermal reference plane, and then use a thermocouple imbedded in the heat sink and touching the case to properly calculate junction temperature using θ_{JC}. for plastic packages, there is no equivalent method.

Enter $\Psi_{J\text{-}T}$

During discussions with industry leading suppliers, it became obvious that the practices described above were in use regularly and without question. Users of semiconductors had grown accustomed to placing the thermocouple and calculating the junction temperature without really understanding the implications of their actions. To counter this trend and

provide a more meaningful method to predict junction temperature in plastic packaged devices, the parameter Ψ_{J-T} was created. An excerpt from the EIA/JESD51-2 standard follows describing the method and use of Ψ_{J-T}.

4.0 THERMAL CHARACTERIZATION PARAMETER - Ψ_{JT}
JUNCTION-TO-TOP CEN TER OF PACKAGE

The thermal characterization parameter, Ψ_{JT}, is proportional to the temperature difference between the top center of the package and the junction temperature. Hence, it is a useful value for an engineer verifying device temperatures in an actual environment. By measuring the package temperature of the device, the junction temperature can be estimated if the thermal characterization parameter has been measured under similar conditions.

The use of Ψ_{JT} should not be confused with θ_{JC} which is the thermal resistance from the device junction to the external surface of the package or case nearest the die attachment as the case is held at a constant temperature. The use and reporting of the case temperature during the junction to ambient thermal resistance test is optional.

The measurement may be made using a temperature transducer such as a thermocouple, fluoroptic sensor, or infrared sensor.

4.1 THERMOCOUPLE PLACEMENT LOCATION

The thermocouple bead shall be attached to the package at the geometric center of the top surface. The position must be reported, in all cases, along with the measurement data.

4.2 PACKAGE THERMOCOUPLE APPLICATION

CAUTION: Usefulness of this measurement is dependent on the procedure.

Application of the thermocouple is critical to ensure proper thermal contact to the package and to ensure that the θ_{JA} measurement is not disturbed. Determination of the package surface temperature, of a low conductance package body, requires that the following factors be considered:

4.2.1 The thermocouple wire and bead shall touch the surface of the package.

4.2.2 Best practice for attaching the wire and thermocouple bead is the use of a minimal amount of thermally conducting epoxy. The distance across the epoxy bead shall not exceed .1" (2.54 mm) in any direction.

4.2.3 The thermocouple wire shall be routed next to the package body down to the board and along the board. This reduces cooling of the thermocouple junction by heat flowing along the wire.

4.2.4 Thermocouple wire size shall be small such that heat loss along the wire does not cause anomalous low readings. Recommended maximum thermocouple sizes is 36 gauge. For type T thermocouples, 40 gauge is preferred.

4.3 PROCEDURE

The junction temperature and package temperatures are determined at the steady-state condition in the θ measurement as specified above. The junction-to-top center of package thermal characterization parameter, Ψ_{JT}, is calculated using the following equation:

4

$$\Psi_{JT} = (T_{Jss} - T_{Tss})/P_H \quad (4)$$

where Ψ_{JT} = thermal characterization parameter from device junction to the top center of the package surface(°C/W)

T_{Jss} = the junction temperature at steady-state.

T_{Tss} = the package (top surface) temperature, at steady-state, measured by the thermocouple, infrared sensor, or fluoroptic sensor.

The relationship between the junction-to-ambient thermal resistance, θ_{JA}, and the junction-to-top center of package thermal characterization parameter, Ψ_{JT}, is described by equation 5:

$$\theta_{JA} = \Psi_{JT} + \Psi_{TA} \quad (5)$$

where Ψ_{TA} = thermal characterization parameter from top surface of the package-to-air (°C/W)

The package-to-air thermal characterization parameter, Ψ_{TA}, is based on the steady-state ambient air temperature as shown here:

$$\Psi_{TA} = (T_{Tss} - T_{Ass})/P_H \quad (6)$$

The thermal characterization parameters, Ψ_{JT} and Ψ_{TA}, have the units °C/W but are mathematical constructs rather than thermal resistances because not all of the heating power flows through the exposed case surface. It is not necessary to report Ψ_{TA} because it can be determined from the relationship between θ_{JA} and Ψ_{JT}. Also, Ψ_{TA} is very dependent on the application-specific environment.

Conclusion

This memo has attempted to educate and inform package, process, and product engineers in the correct use of temperature measurements on the external surface of the package to determine junction temperature. If we educate our customers, system level thermal analysis will be more accurate, allowing a larger application range for our products, especially in critical situations. Because the measurement is relatively new, we are in the process of generating Ψ_{J-T} values for all AMD surface mount plastic packages. If a value is needed for a particular product, please contact the Package Characterization Group in MSD Engineering.

References

1. "Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device), EIA/ JESD51 Standard, Electronic Industries Association, 1995

2. "Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device), EIA/JESD 51-1 Standard, Electronic Industries Association, 1995

3. "Integrated Circuit Thermal Test Method Environmenatl Conditions - Natural Convection (Still Air), EIA/JESD 51-2 Standard, Electronic Industries Association, 1995

4. "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages," EIA/JESD 51-3 Standard, Electronic Industries Association, 1996

5. "Thermal Test Chip Guideline (Wire Bond Type Chip)," EIA/JESD 51-4 Standard, Electronic Industries Association, 1996

6. "Extension of Thermal Test Board Standards for Packages with Direct Attach Mechanisims", EIA/JESD 51-5, Electronic Industries Association, 1999

7. "Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air), EIA/JESD 51-6, Electronic Industries Association, 1999

8. "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages," EIA/JESD 51-7, Electronic Industries Association, 1999

9. "Accepted Practices for Making Microelectronic Device Thermal Characteristics Tests - A User's Guide," JEDEC Engineering Bulletin No. 20, Electronic Industries Association, Washington, DC.

10. "Thermal Characteristics," Method 1012.1, MIL-STD-883C Test Methods and Procedures for Microelectronics, Department of Defense, Washington, DC.

11. "Unencapsulated Thermal Test Chip," SEMI G32-86 Guideline, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.

12. "Junction-to-Case Thermal Resistance Measurements of Molded-Plastic Packages," SEMI G43-87 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.

13. "Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages," SEMI G42-88 Specification, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.

14. "Junction-to-Case Thermal Resistance Measurements of Ceramic Packages," SEMI G30-88 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.

15. "Thermal Transient Testing for Die Attachment Evaluation of Integrated Circuits," SEMI G46-88 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.

16. "Still-and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of Integrated Circuit Packages," SEMI G38-87 Test Method, 1989 Book of SEMI Standards, Vol. 4, Packaging Division, SEMI, Inc. Mountain View, CA.

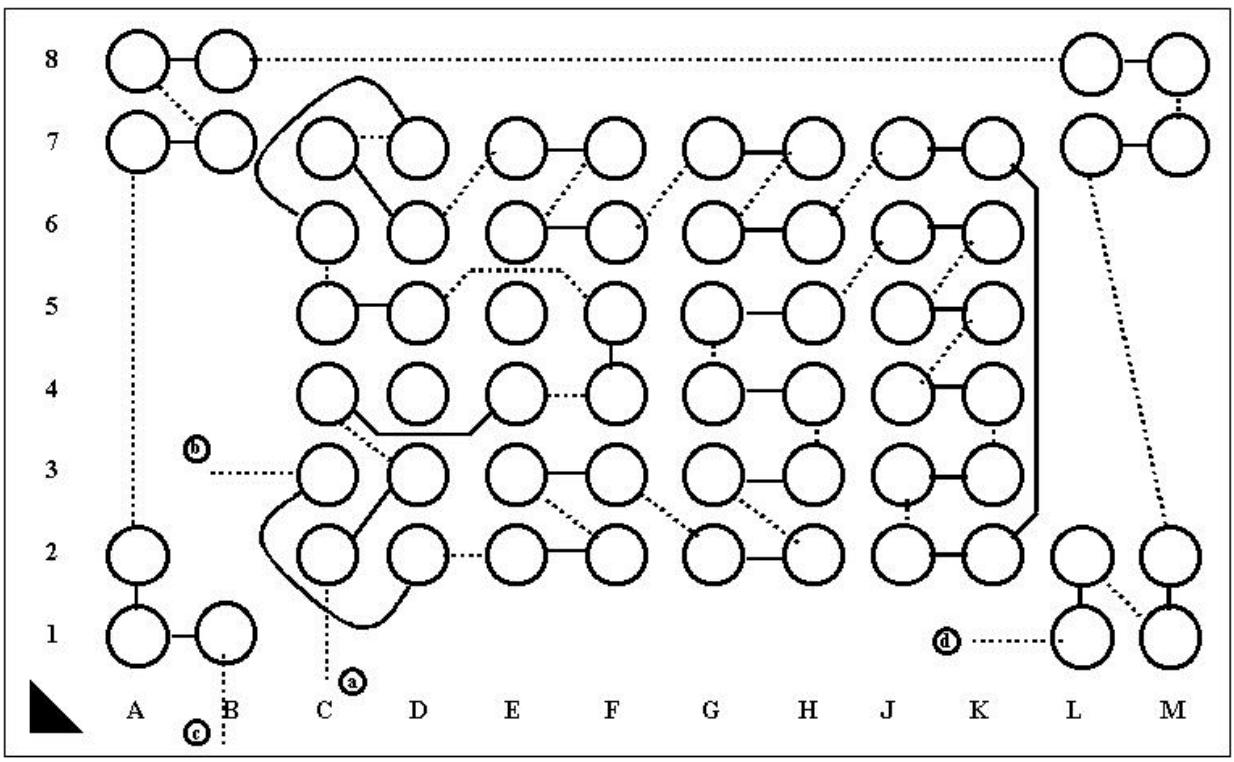
Appendix B: Application Note

The following information is excerpted from a published AMD Application Note, number 22142.

Daisy Chain Samples

Application Note

Daisy Chain samples are non-functional parts with a pattern of inter-connected balls. These samples are typically assembled onto a printed circuit board (PCB) with matching patterns. Once assembled on the matching PCB, all balls are connected creating a continuous network. Refer to Figure 1.



Notes:

1. *"_____" Solid traces are Daisy Chain patterns on the FBGA package.*
2. *"- - - - -" Dash traces are Daisy Chain patterns on the PCB.*
3. *'a', 'b' are the input and output of the network for the device.*
4. *'c', 'd' are the input and output of a separate network for the support balls.*

Figure 1. FBGA 32 Mb and 64 Mb Silicon Daisy Chain with Matching PCB Schematic (Top View)

Daisy Chain samples are primarily requested by OEMs to perform assembly evaluations. Prior to production, an OEM will generally solder daisy chain samples on to a daisy chain PCB and perform Open/Short testing to check for misalignments. This test will help an OEM characterize its assembly process and equipment prior to full production.

Daisy Chains are also used in Second Level Solder-Joint Board Reliability studies. The daisy chain samples are assembled onto the matching PCB and subjected to temperature cycling in an oven. Board Level Reliability tests are tools to help predict and measure the expected life of packages. For more in depth information on Second Level Solder-Joint Board Reliability,

Publication# **22142** Rev: **A** Amendment/**+2**
Issue Date: **April 15, 2002**

please refer to "Reliability Evaluation of Chip Scale Packages" by Ranjit Gannamani, Viswanath Valluri, Sidharth, and MeiLu Zhang.

Currently AMD has three types of FBGA daisy chains: Stitched Daisy Chains, Metal Mask Daisy Chains and Substrate Daisy Chains. Since the main purpose is to characterize assembly process and equipment, OEMs typically have no preference on the type of daisy chain used.

DESCRIPTIONS

Stitched Daisy Chains

The functional substrate is used with a dummy silicon slug. Daisy chain patterns are produced by shorting pairs of adjacent bond-fingers on the substrate via wire bonding. There are no wire bonds from the dummy silicon slug to the substrate.

Metal Mask Daisy Chains

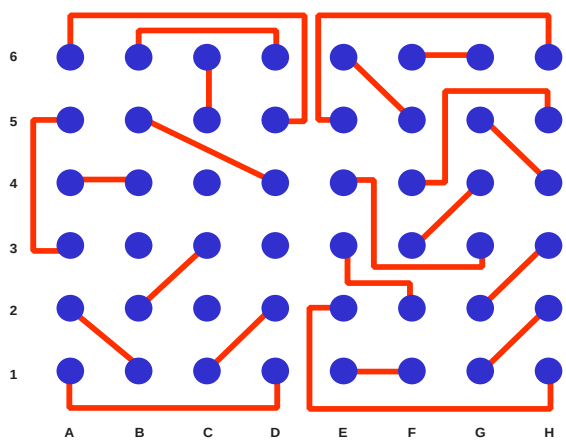
The functional substrate is used with a special daisy chained wafer. There is no active circuitry on the wafer, only the simulated bond-pads. Adjacent bond-pads are shorted via metal mask. Daisy chain patterns are produced by wire bonding the bond-fingers on the substrate to the bond-pads on the wafer.

Substrate Daisy Chains

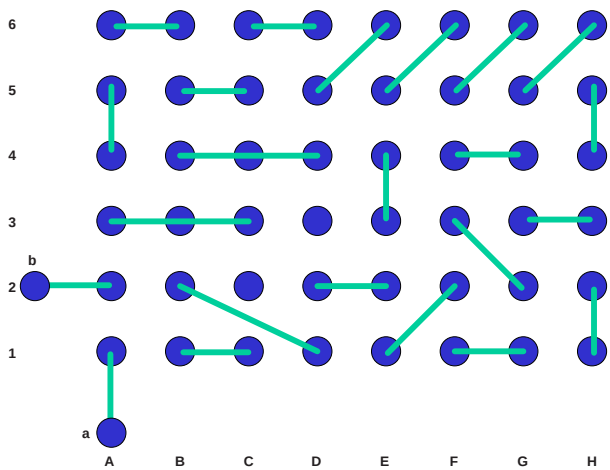
A dummy silicon slug is used with a special daisy chained substrate. Shorting adjacent balls on the substrate produces daisy chain patterns.

9 X 8 MM FINE PITCH-BGA (WC) DAISY CHAIN SCHEMATIC

Package Connection (Bottom View)



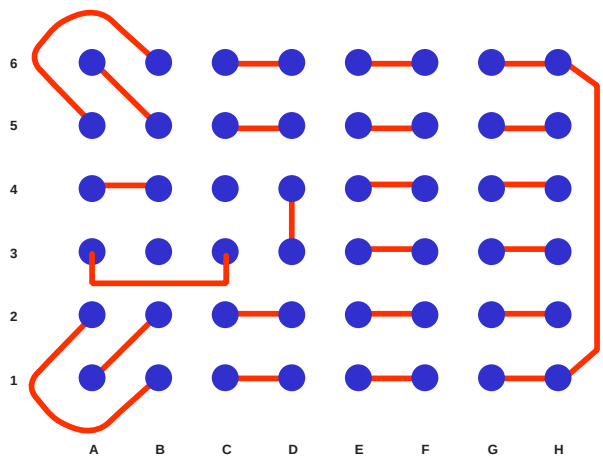
Board Connection (Top View)



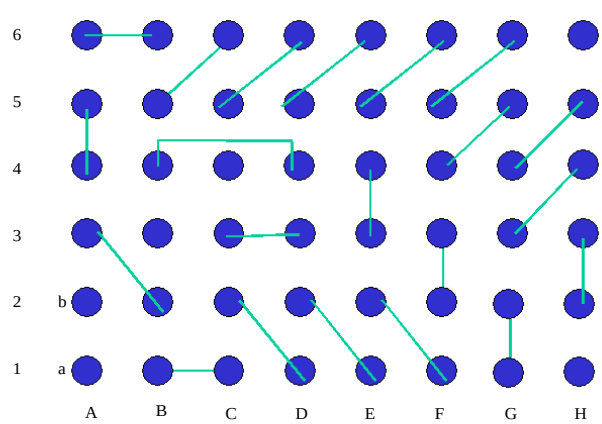
Note: *a and b are input and output of the network.*

12 X 6 MM 48-BALL FINE PITCH-BGA DAISY CHAIN SCHEMATIC

Package Connection (Bottom View)

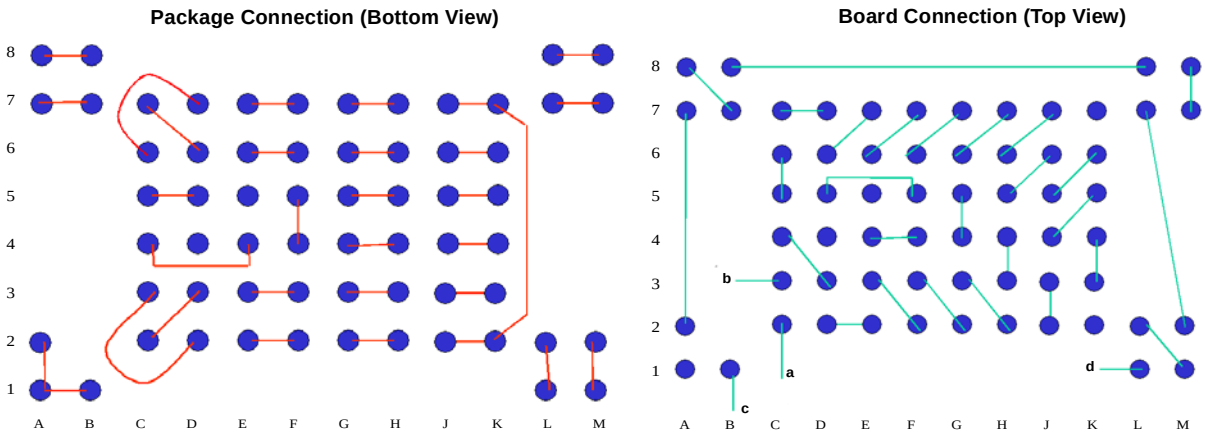


Board Connection (Top View)



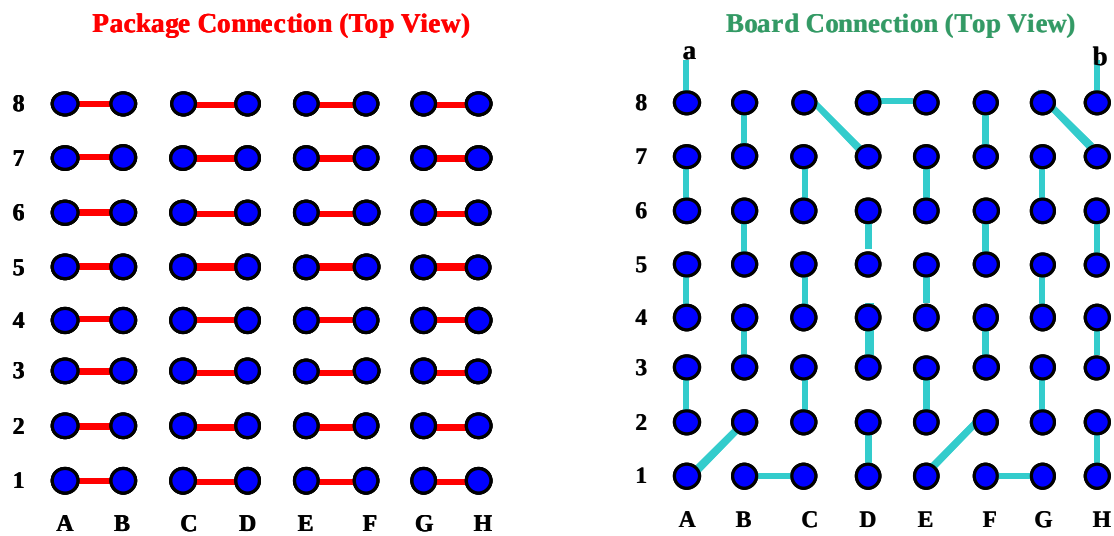
Note: *a and b are input and output of the network.*

12 X 11 MM 63-BALL FINE PITCH-BGA DAISY CHAIN SCHEMATIC '



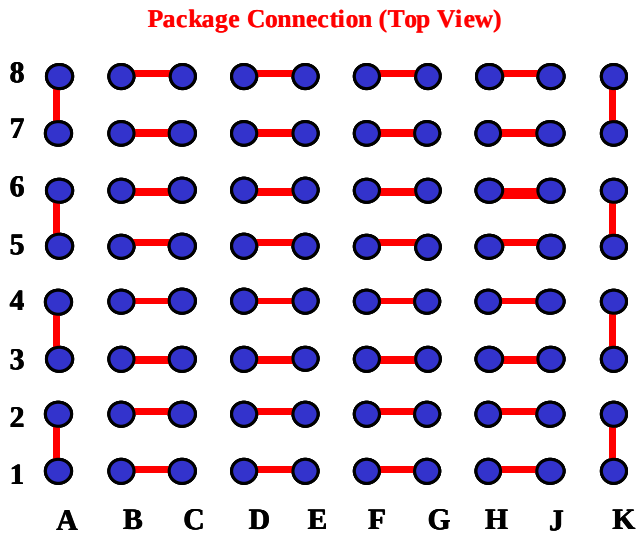
Note: *a and b are input and output of the network. c and d are input and output of a separate network for support balls.*

13 X 11 MM 64-BALL FORTIFIED-BGA DAISY CHAIN SCHEMATIC



Note: *a and b are input and output of the network.*

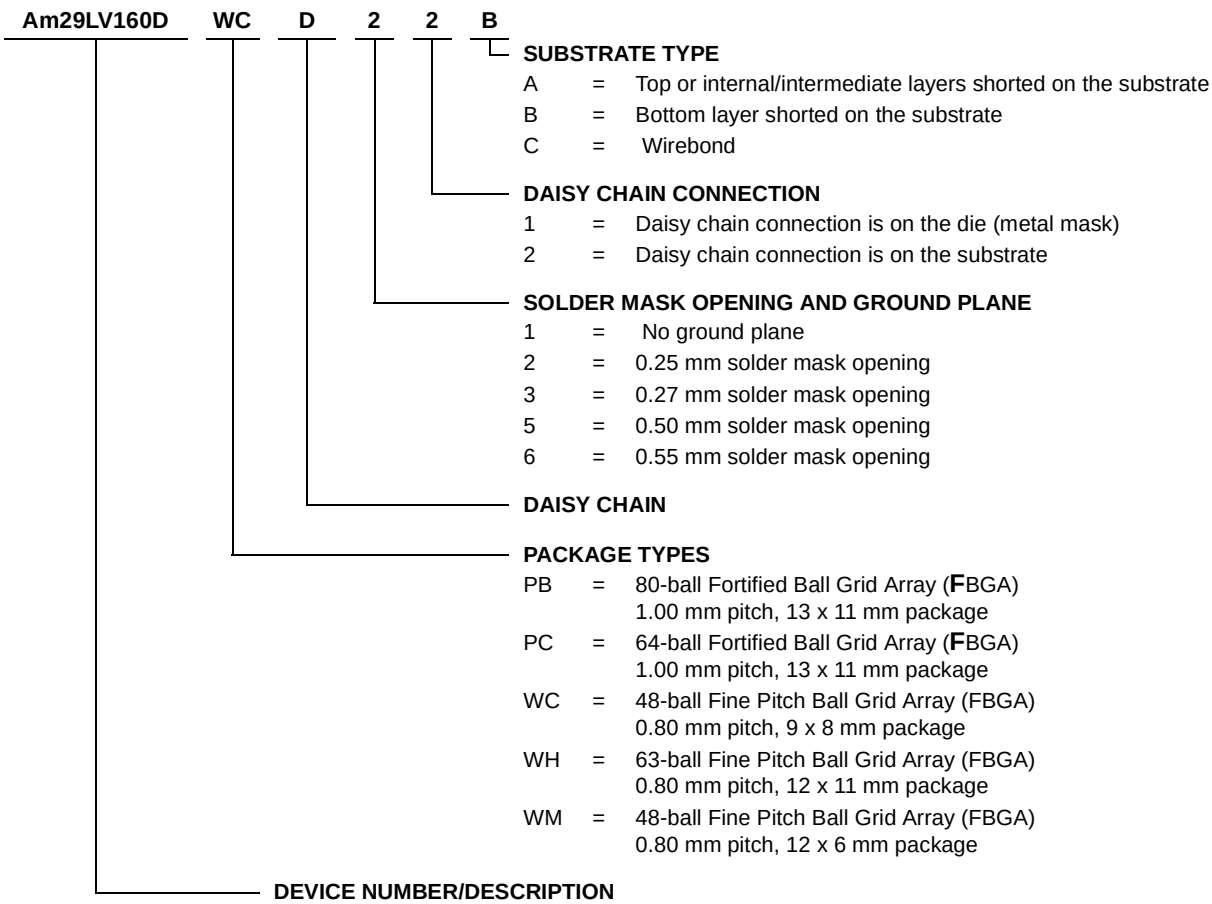
13 X 11 MM 80-BALL FORTIFIED-BGA DAISY CHAIN SCHEMATIC



Note: *a and b are input and output of the network.*

ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations for BGA Daisy Chain			
Density	**Package**	**Order Number**	**Package Marking**
16 Mb	9 x 8 Fine Pitch BGA (WC) 13 x 11 mm Fortified BGA (PB)	AM29LV160DWCD22B AM29BDD160GPBD62B	LV160DD22B BDAFGD62B
32 Mb	12 x 6 mm FBGA (WM)	AM29DL323DWMD22B	DL323DD22B
64 Mb	12 x 11 Fine Pitch BGA (WH) 13 x 11 mm Fortified BGA (PC)	AM29DL640DWHD22B AM29LV640DPCD62B	DL640DD22B LCEDD62B

To place an order, please contact your local AMD sales representative. For a current list of contacts via the Internet go to http://www.amd.com/support/sales.html

Revision Summary

Revision E (Version 2.2): March 13, 1999

Chapter 2

Modified 32 and 64 Mb daisy chain and board layout drawings. 32 and 64 Mb pinout drawings now show outrigger balls that are shorted.

Revision F (Version 2.3): May 17, 1999

Construction of the FBGA-BT figure

Revised the following callouts: Mold Compound (deleted "Multi-Functional"), Die Attach (deleted "Non-conductive"), Solder Mask (deleted "50µ Nom"), Copper Foil (deleted "12µ"), Plating (deleted thickness from Cu and Au).

FBGA Package Materials Descriptions

In the table, renamed the following parameters: Rigid Substrate; Molding Compound; Die Attach Material. Deleted "Interposer" from Copper Metallization.

FBGA Ball Attach Detail

Clarified type of attach.

Component Level Testing, FBGA-BT

Changed JC-14.1-98-135, Level 2 qualifications is planned for Q2, 1999 to JCB-98-104. In the table, added rows 4 through 6. In item 3, changed ramp-up rate to 3°C, time at max. temperature to 10–20 seconds.

FBGA-BT Component Level Test Results

Replaced and reformatted data in table.

Test Strategy

Deleted reference to data supplied to AMD weekly.

FBGA Package Marking

Added "D" technology designator. Revised explanatory table.

FBGA Package Dimensions

Renamed WE and WF designators to WG and WH, respectively.

Revision F+1 (Version 2.3.1): July 30, 1999

Chapter 2

16 Mb Daisy Chain and Board Layout figures. Added new 99xx date code daisy chain schematic and board layout. Added 98xx date code to previous drawings.

Revision G (Version 3.0): January 15, 2001

Chapter 2

Replaced all FGBA pinout figures with new illustrations.

Chapter 3

Updated package outline diagrams with specification 16-038-9 illustrations. Replaced Table 3-1 FBGA-BT with new information. Section on "FBGA Thermal Resistance Data" replaced with section on "FBGA Thermal Management".

Chapter 4

Added HDI information in the "General Design Considerations" section. Replaced "Routing Dimensions" section with "Routing Recommendation" section. Added "gold thickness of 5 mils max is recommended" to the "PC Board Surface Finish" subsection. Updated "Recommended Design Values" in the table below Figure 4-2. Replaced "Routing Dimensions" and "Routing for 32-Megabit" figure with "Example of Routing" figures.

Chapter 5

Replaced entire chapter with new information.

Appendix A

New article reprints.

Appendix B

New application note.

Revision G+1 (Version 3.1): March 12, 2001

Chapter 2—Daisy Chains

Added "Both are listed in the Appendices." to the end of the second paragraph.

Chapter 3—FBGA Thermal Management

Added "T_{ASS} = Temperature of Ambient Air at Steady State" to the "θ_{JA} – Junction to Air" equations

Table 3-2. Thermal Resistance Data: Changed table headings "θ_{JC} (°C/W)" to "θ_{JMA} (°C/W)" and "θ_{JMA} (°C/W)" to "Ψ_{J-T} (°C/W). Shifted down the values in the θ_{JMA} (°C/W) table column. Moved data of the FGC048 Ψ_{J-T} (°C/W) table cell to the FGC048 θ_{JMA} (°C/W) location. Added the following table notes: "4. θ_{JMA} = Theta of junction to moving air." and "5. SPD (LFPM) = Speed of moving air, in terms of "Linear Feet Per Minute"." Corrected the FBD063 θ_{JA} (°C/W) data.

Revision H (Version 4.0): January 24, 2002

Chapters 1–4

Chapters were completely rewritten. It is recommended that users of previous editions read through these chapters to familiarize themselves with the revised content.

Chapter 5

New daisy chain schematics and board layouts have been added. The first two figures from the previous User's Guide have been deleted.

Revision I (Version 4.1): April 12, 2002

Chapter 2

Figure 2-3: Added Am29PDS322D to list of devices in 8 x 9 mm package.

Figure 2-7: corrected 4Gb to 128 Mb.

Chapter 5

Corrected figure 5-7 from 80 to 84 ball; figure 5-8 from 64 to 84 ball, figure 5-10 from 80 to 64 ball.

Chapter 6

Table 6.1: Corrected units of measure in thickness column from mm to µm. Deleted E-05 from specifications in CTE ppm/c column.

Added descriptions for FLA069, FLB073, LAA064, LAA080, LAB 080, and LBA176

Chapter 7

Recommended Board Desin Dimensions: Modified table to show both 0.30 and 0.60 mm balls.

Chapter 10

FBGA Package Designators: Added 6 x 12, 11 x 13 , and 10 x 15 mm sizes.

Appendix B

Updated information from October 25, 2001 revision of application note.

Revision J (Version 4.2): November 1, 2002

Chapter 7

Modified table to include values for 0.35 mm solder balls. Changed tolerances on dimension A for 0.30 and 0.60 solder balls. Changed dimension C for 0.30 solder balls.

One AMD Place
P.O. Box 3453
Sunnyvale,
California 94088-3453
USA
(408) 732-2400
(800) 538-8450
TWX: 910-339-9280
TELEX: 34-6306

TECHNICAL SUPPORT
USA & CANADA non-PC CPU: (800) 222-9323
USA & CANADA PC CPU: (408) 749-3060
USA & CANADA PC CPU E-mail: hw.support@amd.com
EUROPE & UK: +44-(0)1276 803299
Fax: +44-(0)1276 803298
BBS: +44-(0)1276 803211
FRANCE: 0800 90 8621
GERMANY: 089-450-53199
ITALY: 1678-77224
EUROPE E-mail: euro.tech@amd.com
FAR EAST Fax: (852) 2956-0599
JAPAN: 03-3346-7550
Fax: 03-3346-7848
ARGENTINA: 001-800-200-1111,
after tone 800-859-4478
CHILE: 800-532-853
MEXICO: 95-800-222-9323

LITERATURE ORDERING
USA & CANADA: (800) 222-9323
EUROPE E-mail: euro.lit@amd.com
FAR EAST Fax: (852) 2956-0599
JAPAN Fax: 03-3346-9628

www.amd.com

Printed in USA
11/01/02
22142J