3.0 Volt-only Page Mode Flash Memory Technology

Technology Background

July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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Introduction

AMD, the technology leader in Flash memories, has developed a new generation of high-performance, single-power-supply flash memory devices. The Am29PL160C is the first page mode low-voltage flash memory device from AMD. This device allows read access times as fast as 25 ns, and performs all read, program, and erase operations using only a single 2.7 volt power supply. These devices offer all of the features of AMD's industry-standard 2.7 volt-only Am29LVxxx devices with substantially faster access times, making it the ideal choice for low-power, high performance applications. In addition, this device is 5 volt I/O tolerant allowing it to be easily used in 5 volt systems. The Am29PL160C device supports an industry standard 8-word page size. This 8-word page size gives system designers the added flexibility of being able to support not only 8-word page size processors, but also 4-word page size processors as well.

The following is an abbreviated list of the Am29PL160C distinctive characteristics:

- ❑ 25 ns page access time
- ❑ 65 ns initial access time
- ❑ 2.7 V to 3.6 V device V_{CC} operating range
- ❑ 5 V I/O tolerant on data, address, and control signals
- ❑ 8-word page size
- ❑ Minimum 1,000,000 program/erase cycles guaranteed per sector

For a complete list of features, operational description and specifications see publication number 22143 (Am29PL160C data sheet).

In many low cost consumer applications, the control code is typically stored in masked ROM. Masked ROM does not offer any flexibility as far as updating code stored in the ROM. This places severe limitations on time-to-market, as well as manufacturing efficiency. Typically during the prototyping phase of a product, the control code is updated several times to include new features and fix bugs. Each time there is a modification to the code, a new masked ROM must be spun to store the modified code, as masked ROM is not erasable. Given the average number of fixes to the code prior to production, this can add up to a significant amount of development time and money.

The Am29PL160C allows system designers to take advantage of the reprogrammability of flash during the design and initial production phases—when they need flexibility the most—and then switch to masked ROM when that flexibility is no longer needed. This is possible since the AC characteristics and pinout of the Am29PL160C are compatible with page mode

masked ROMs in the 44-pin SO package. In this scenario, a system designer will be able to use flash in the system while the code is still in development, and update the code as often as necessary with no time or cost impact. At the point where the code is determined to be stable, and no longer needs to be changed, a masked ROM may be dropped into the socket in place of the Am29PL160C, and the cost benefit of masked ROMs can then be realized. The combination of the flexibility of flash and the cost-savings of masked ROM can most optimally be realized with the Am29PL160C device.

The page mode device can also be used for pure performance advantage as well. This device offers initial access times as low as 65 ns, and page accesses as fast as 25 ns. In some cases, this may result in additional cost savings by reducing the amount of DRAM required in the system. In a typical embedded application, the memory system may contain DRAM for code execution and Flash for control code storage. Because of faster read access times of DRAM, the control code is typically downloaded from the flash into the DRAM and executed from there. The fast read access times of the Am29PL160C allows shadow DRAM to be eliminated in many cases. The code can be executed directly from the flash memory. The overall system cost is lowered because the redundant DRAM is eliminated.

In addition, many of today's systems still use mixed voltages. This is partly due to some 5.0 V devices such as ASICs, processors, etc. that must be used on the board. As these devices often control the system data and address buses, the system bus must operate at 5.0 volts. In order to interface these buses to a lower-voltage memory devices, voltage translators must be designed into the system to translate the higher system bus voltage down to the lower voltage tolerated by the memory device. Because the Am29PL160C has 5 volt I/O and control signal tolerance, DC-to-DC converters are no longer required. This leads to lower overall system cost.

Block Diagram

Internally, the Am29PL160C is designed with the same leading-edge design as the traditional 29LVxxx family of devices, with some additional read control logic. This read control logic was modified to allow the flash device to have 25 ns page access times. This additional logic is incorporated into the Data Latch block in the block diagram below.

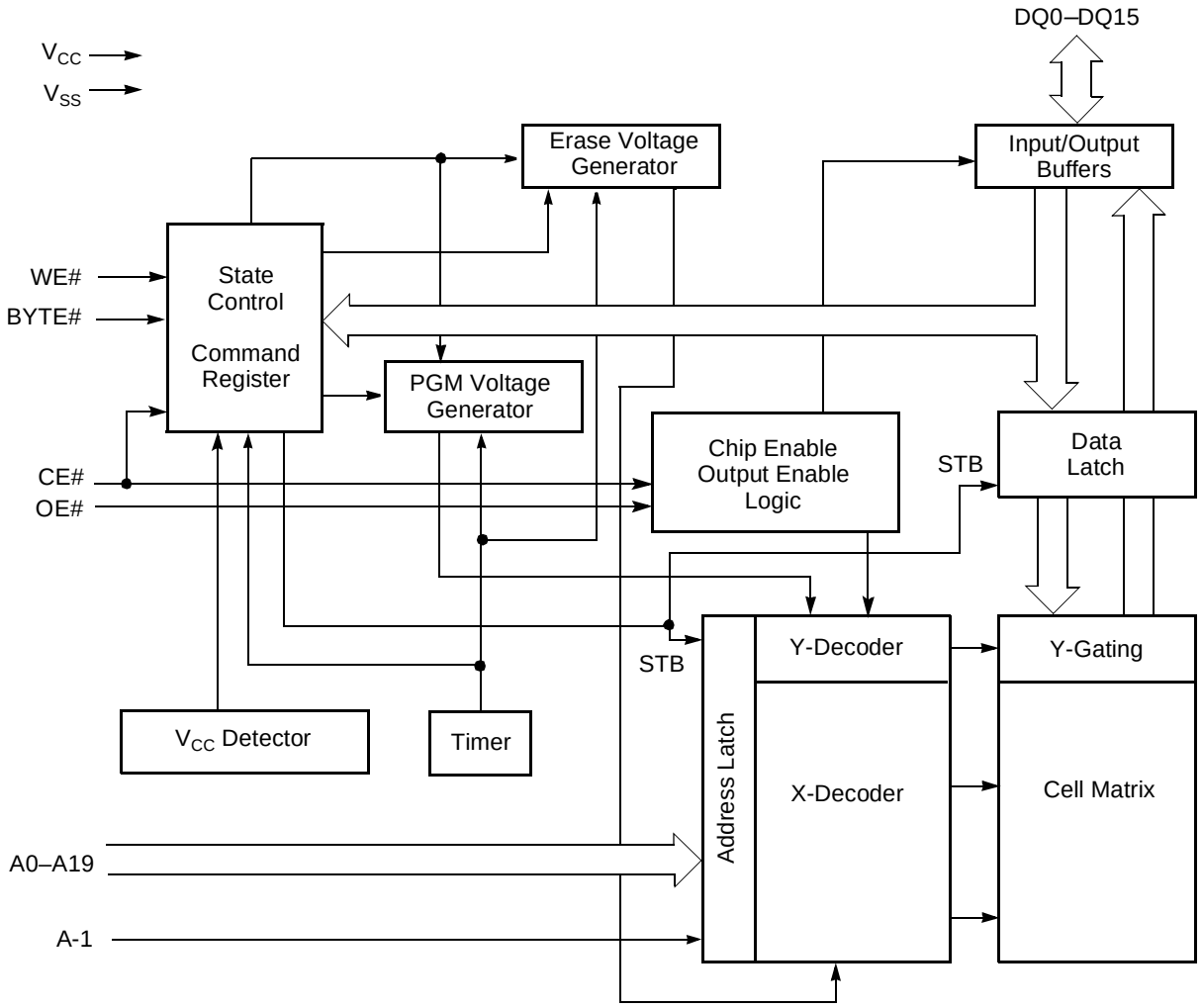

Figure 1. Am29PL160C Block Diagram

Read Operation

The Am29PL160C is capable of fast page mode reads and is compatible with the page mode masked ROM read operation. This mode provides 25 ns data accesses from random locations within a page. The page size of the Am29PL160C device is 8 words or 16 bytes. Address bits A3-A19 select the appropriate page; address bits A0-A2 (in word mode) or A-1 to A2 (in byte mode) determine the specific word/byte within that page. This is an asynchronous operation with the microprocessor supplying the specific word or byte location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) are equivalent to t_{PACC}. When CE# is de-asserted and reasserted for a subsequent access, the access time is t_{ACC}

or t_{CE}. CE# selects the device, and OE# is the output control that should be used to gate data to the output pins when the device is selected. Fast page mode accesses are obtained by keeping A3-A19 constant and changing A0 to A2 to select the specific word, or changing A-1 to A2 to select the specific byte, within that page.

The following tables determine the specific word and byte within the selected page:

Word	A2	A1	A0
Word 0	0	0	0
Word 1	0	0	1
Word 2	0	1	0
Word 3	0	1	1
Word 4	1	0	0
Word 5	1	0	1
Word 6	1	1	0
Word 7	1	1	1

For Byte Mode, A-1 would need to be added into this table as the least significant bit.

The timing diagram in Figure 2 demonstrates this page mode operation. In this mode, the page size is 16 bytes.

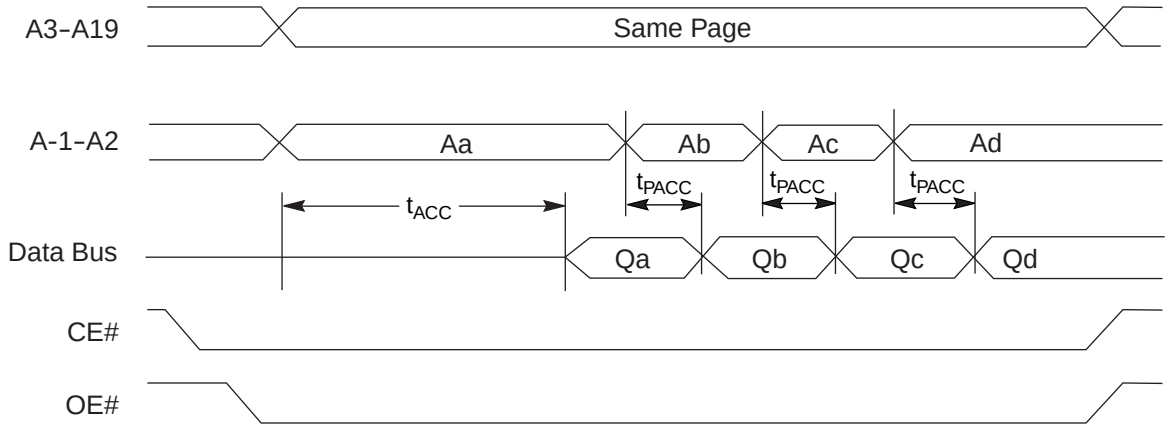

Figure 2. Page Mode Read Operations

Summary

Technology leadership, experience, and creativity of AMD's engineering resources have once again led to the arrival of the next generation of high performance flash memory devices. The Am29PL160C is a low voltage, page mode device that offers page read access times of 25 ns, with initial access times of 65 ns. The high performance, reduced power consumption, and industry-leading guaranteed minimum endurance of 1,000,000 cycles combine to make this device an ideal choice for cost-sensitive, performance-driven applications.

One AMD Place
P.O. Box 3453
Sunnyvale,
California 94088-3453
USA
(408) 732-2400
(800) 538-8450
TWX: 910-339-9280
TELEX: 34-6306

TECHNICAL SUPPORT
USA & CANADA non-PC CPU: (800) 222-9323
USA & CANADA PC CPU: (408) 749-3060
USA & CANADA PC CPU E-mail: hw.support@amd.com
EUROPE & UK: +44-(0)1276 803299
Fax: +44-(0)1276 803298
BBS: +44-(0)1276 803211
FRANCE: 0800 90 8621
GERMANY: 089-450-53199
ITALY: 1678-77224
EUROPE E-mail: euro.tech@amd.com
FAR EAST Fax: (852) 2956-0599
JAPAN: 03-3346-7550
Fax: 03-3346-7848
ARGENTINA: 001-800-200-1111,
after tone 800-859-4478
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