AMD

AMD's 3.3-V NetPHY™-1LP Device with Motorola's MC68360, MPC860, MPC850, MPC855, and MPC8260

Application Note

AMD's 3.3-V NetPHY™-1LP Device with Motorola's MC68360, MPC860, MPC850, MPC855, and MPC8260

Application Note

The following application note describes how to interface AMD's Am79C874 NetPHY-1LP 10/100 Mbps Ethernet physical layer transceiver to the SCCs, FECs, and FCCs on Motorola's integrated communication microprocessors.

Most of the Motorola QUICC™, PowerQUICC™ and PowerQUICC II™ integrated communication microprocessors support 10 Mbps Ethernet and/or Fast Ethernet. All of the Motorola integrated communication microprocessors that support Ethernet or Fast Ethernet require a separate PHY (transceiver). The AMD Am79C874 NetPHY-1LP device is a 3.3-V Ethernet PHY that operates at either 10 Mbps or 100 Mbps. The NetPHY-1LP device connects easily, without any glue logic, to all of the Ethernet or Fast Ethernet ports on these Motorola communication microprocessors.

There are two methods (one for 10 Mbps Ethernet and one for 10/100 Mbps Fast Ethernet) of interfacing the NetPHY-1LP device to the Ethernet or Fast Ethernet ports on the Motorola microprocessors. This application note provides information on both methods of interfacing the Motorola integrated communication microprocessors to the AMD NetPHY-1LP device.

Table 1 summarizes the Ethernet and Fast Ethernet support provided by the different Motorola communication microprocessors and the interface used to connect to the AMD NetPHY-1LP device. Refer to the Motorola QUICC/PowerQUICC/PowerQUICC II data sheets and AMD NetPHY-1LP data sheet (PID#22235) for additional information.

Table 1. Ethernet and Fast Ethernet Support of the Motorola Communication Microprocessors

Motorola Microprocessor	MC68360 QUICC	MPC860 PowerQUICC, MPC850, and MPC855	MPC8260 PowerQUICC II
Support for 10 Mbps	Ethernet-enabled Serial Communication Controllers (SCC)	Ethernet-enabled Serial Communication Controllers (SCC)	Ethernet-enabled Serial Communication Controllers (SCC)
10 Mbps Interface to use with AMD NetPHY-1LP Device	GPSI, 7-wire, SIA interface	GPSI, 7-wire, SIA interface	GPSI, 7-wire, SIA interface
Support for 10/100 Fast Ethernet	None	Fast Ethernet Controllers (FEC) on 860T and 860DT	Fast Communication Controllers (FCC)
10/100 Mbps interface to use with AMD NetPHY-1LP Device	N/A	MII	MII
Support for MDC/MDIO Management Register	No	Yes	Yes

10 Mbps Ethernet

The AMD NetPHY-1LP device can be used as a low-cost 10BASE-T PHY. The Ethernet-enabled SCCs of the QUICC/PowerQUICC/PowerQUICC II and the NetPHY-1LP device support the 7-wire, SIA interface (also called General Purpose Serial Interface (GPSI) mode). This section of the application note describes how to connect the GPSI 7-wire, SIA interface of the NetPHY-1LP PHY with Motorola's Ethernet-enabled SCCs.

Because every SCC has different pin names, the actual SCC pin names in Figure 1 were omitted. Refer to Table 2 for proper corresponding SCC pin names.

Publication# **22356** Rev: **C** Amendment/**0**
Issue Date: **June 2000**

Table 2. NetPHY-1LP Pin Connections to Various SCC pins

Am79C874 Pins	SCC Pins			
	SCC1	SCC2	SCC3	SCC4
10RXCLK	CLKa	CLKa	CLKb	CLKb
10TXCLK	CLKa	CLKa	CLKb	CLKb
10RXD	RXD1	RXD2	RXD3	RXD4
10TXD	TXD1	TXD2	TXD3	TXD4
10TXEN	RTS1	RTS2	RTS3	RTS4
10CRS	CD1	CD2	CD3	CD4
10COL	CTS1	CTS2	CTS3	CTS4

Note: *CLKa = CLK1, CLK2, CLK3 or CLK4*
CLKb = CLK5, CLK6, CLK7 or CLK8

The interface between the SCC and the NetPHY-1LP transceiver has seven pins as shown in Figure 1. Below is a description of these pins and their respective connections:

1. Receive Clock - Receive Clock (10RXCLK) comes from the NetPHY-1LP device and goes into the SCC (RCLK) and may either be the CLK1, CLK2, CLK3, CLK4, CLK5, CLK6, CLK7, or CLK8 pin on the SCC.
2. Transmit Clock - Transmit Clock (10TXCLK) comes from the NetPHY-1LP device and goes into the SCC (TCLK) and may either be the CLK1, CLK2, CLK3, CLK4, CLK5, CLK6, CLK7, or CLK8 pin on the SCC. However, TCLK and RCLK cannot be connected to the same CLK because the Ethernet transceiver supplies a separate clock signal between the transmitter and receiver.
3. Receive Data - 10RXD of the NetPHY-1LP transceiver connects directly to the RXD pin of the SCC.
4. Transmit Data - 10TXD of the NetPHY-1LP transceiver connects directly to the TXD pin of the SCC.
5. Transmit Enable - The SCC's $\overline{\text{RTS}}$ changes to TENA when it is configured to Ethernet mode. TENA connects to the NetPHY-1LP device's 10TXEN pin. This signal allows the SCC to signal the NetPHY-1LP device when there is valid 10 Mbps data on 10TXD.
6. Receive Enable - The SCC's $\overline{\text{CD}}$ changes to RENA when it is configured to Ethernet Mode. RENA connects to the NetPHY-1LP device's 10CRS pin. This signal allows the NetPHY-1LP device to signal the SCC when data has been received.
7. Collision - The SCC's $\overline{\text{CTS}}$ changes to CLSN when it is configured to Ethernet mode. CLSN connects to the NetPHY-1LP device's 10COL pin. This signal indicates the detection of a collision condition.

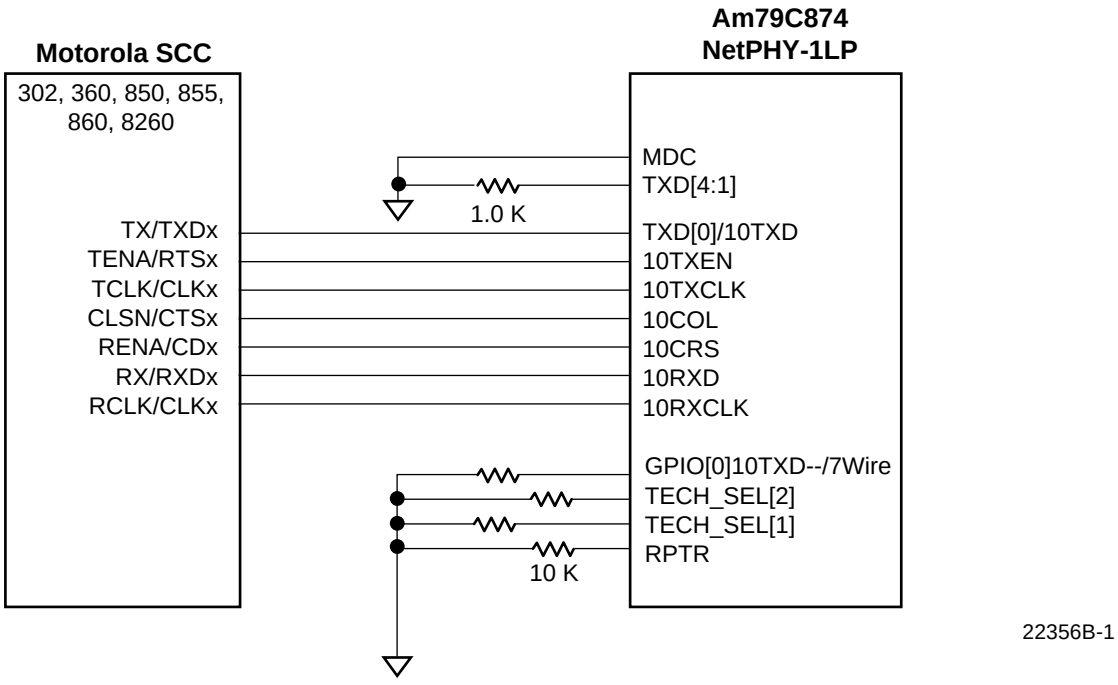

Figure 1. Half-Duplex 10 Mbps Ethernet Interface Between SCC and NetPHY-1LP Devices

The NetPHY-1LP device can be configured to operate in Full or Half-Duplex mode by hardwiring the ANEGA pin and the TECH_SEL[2:0] pins:

Half Duplex	ANEGA=GND, TECH_SEL[2:0]=[GND,GND,NC]
Full Duplex	ANEGA=GND, TECH_SEL[2:0]=[NC,GND,NC]

Note: *NC = No Connection*
GND = 10K pull-down resistor.

On the NetPHY-1LP device, the RPTR pin must be connected to GND. All pins not mentioned must be connected according to the NetPHY-1LP data sheet.

The NetPHY-1LP device can also be connected to the PowerQUICC FEC port using this same GPSI 7-wire SIA interface. This is not the most efficient use of the FEC port because it is capable of both 10 Mbps and 100 Mbps Ethernet operation. Figure 2 shows the 10 Mbps GPSI 7-wire interface between the FEC and the NetPHY-1LP transceiver. NetPHY-1LP PHYAD pins can be configured for any address, except 00h in GPSI mode.

Note: *The NetPHY-1LP side of the interface is unchanged in Figure 1 and Figure 2.*

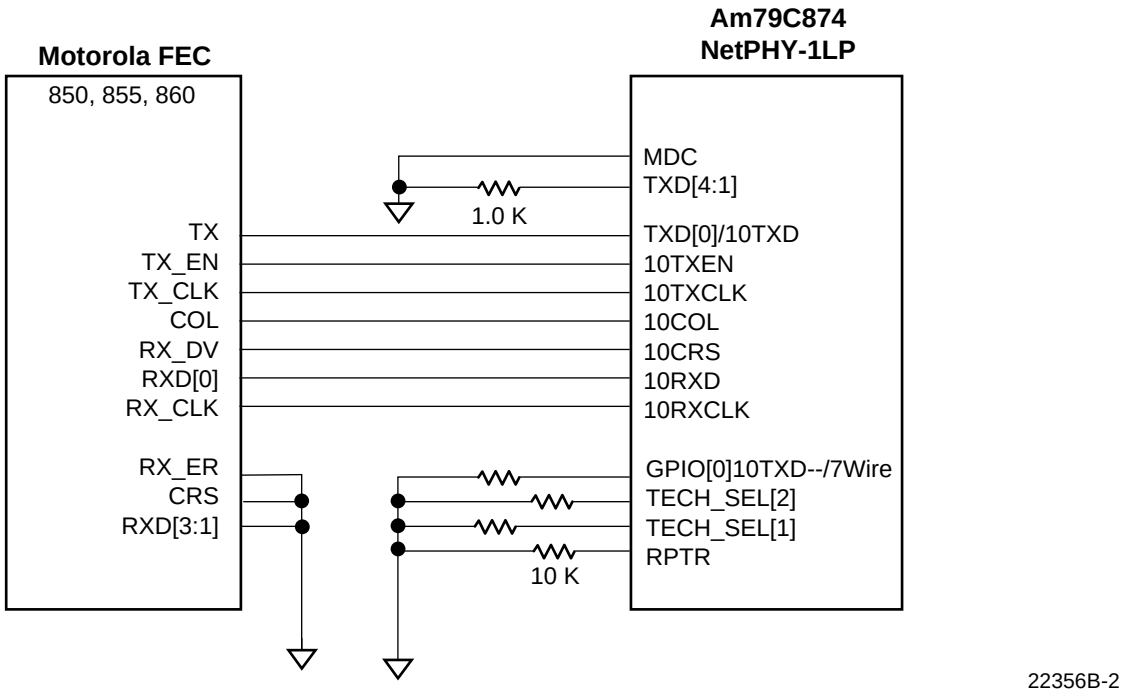

Figure 2. Half-Duplex 10 Mbps Ethernet Interface Between FEC and NetPHY-1LP Devices

10/100 Mbps Ethernet

The AMD NetPHY-1LP device is a high-performance 100BASE-TX/FX PHY. The PowerQUICC's FEC, the PowerQUICC II FCCs, and the NetPHY-1LP device support the IEEE-standard Media Independent Interface (MII). Connecting PowerQUICC/PowerQUICC II to the NetPHY-1LP device using MII is straight forward. Refer to the Motorola MPC860T Fast Ethernet Controller Supplement and the AMD NetPHY-1LP data sheet (PID#22235).

Figure 3 and Figure 4 illustrate the straightforward connection between the NetPHY-1LP device and the FEC or FCC ports. In these figures, the NetPHY-1LP device is configured for all capabilities. This includes auto-negotiation, full or half-duplex, 10 Mbps or 100 Mbps, and the management interface. The MDIO/MDC management interface can gather status information and control the PHY.

Note: *The NetPHY-1LP side of the interface is unchanged in Figure 3 and Figure 4.*

The NetPHY-1LP configuration in all figures is for twisted-pair copper cable operation. Fiber optic operation can be enabled by pulling FX_SEL* (pin 44) low. The NetPHY-1LP configuration in all figures is for using a 1:1 ratio isolation transformer. A power saving 1.25:1 transmit ratio transformer can be enabled by pulling GPIO[1]/TP125 (pin 20) high. The use of the NetPHY-1LP LED pins and the PowerWise™ manage-

ment modes are covered in the NetPHY-1LP data sheet.

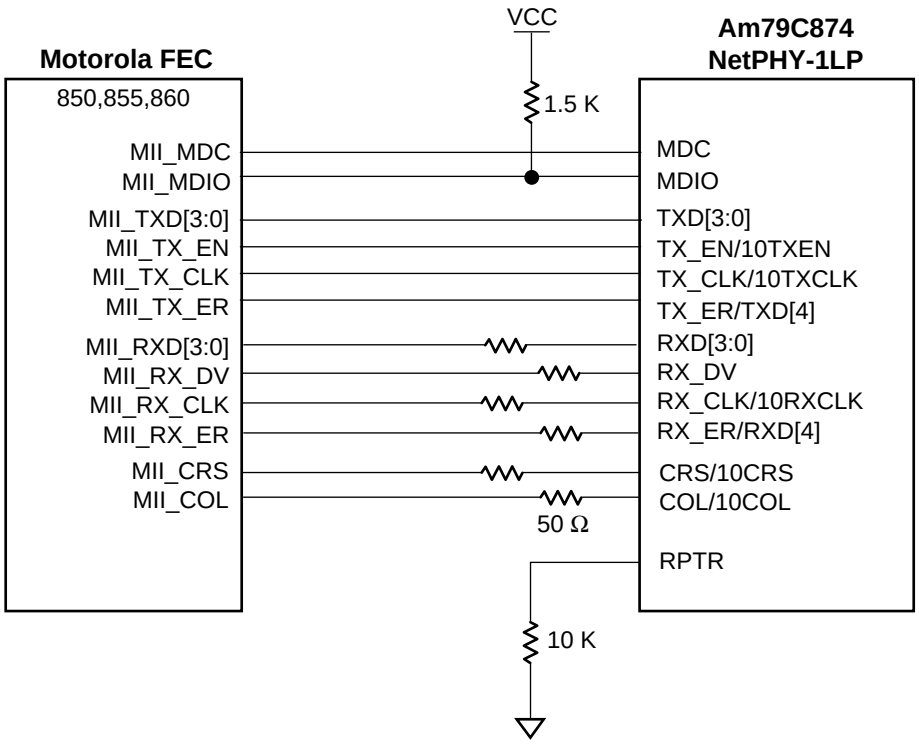

Figure 3. 10/100 Mbps Ethernet Interface Between FEC and NetPHY-1LP Devices

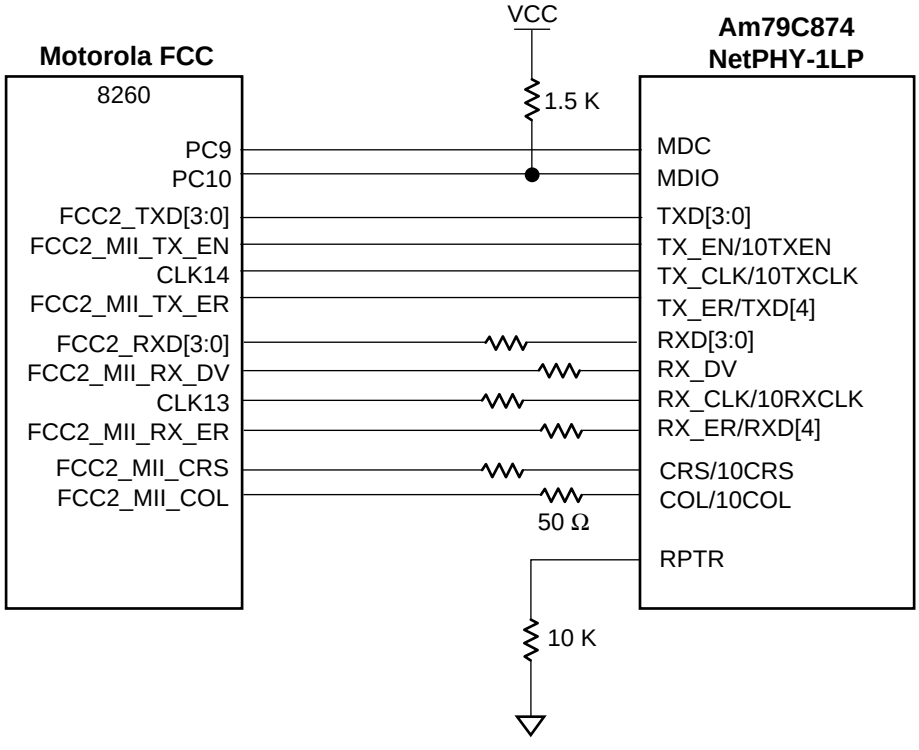

Figure 4. 10/100 Mbps Ethernet Interface Between FCC and NetPHY-1LP Devices

REVISION SUMMARY

Revisions to other versions this document are as follows:

Revision B to C

1. In GPSI mode, PHYAD pins must be set to address other than 00h.