Élan™SC520 Microcontroller Customer Development Platform User's Manual

Order #22450C

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Élan™SC520 Microcontroller Customer Development Platform User's Manual

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About the Élan™SC520 Microcontroller Customer Development Platform

The Élan™SC520 microcontroller customer development platform (CDP) provides a robust evaluation and development platform for the ÉlanSC520 microcontroller. Using the ÉlanSC520 microcontroller, SDRAM, Am79C973 Ethernet controller, and PCI bus, the ÉlanSC520 microcontroller CDP serves as a platform for embedded product development. Within the ÉlanSC520 microcontroller CDP, the embedded PCI bus controller works well with other PCI-ready peripherals (audio, video, etc.).

The ÉlanSC520 microcontroller CDP uses an on-board 10/100 Mbit/s Ethernet based on the Am79C973 PCnet™-*FAST III* device. In addition, the ÉlanSC520 microcontroller CDP uses an ALi Super I/O for additional interface functionality including serial (two), parallel, IrDA, floppy, keyboard, and mouse devices. The ÉlanSC520 microcontroller CDP contains 16-Mbytes of Flash memory that is expandable to an additional 32 Mbytes through a daughter module (with a flexible 8- and 16-bit configuration on the GP-bus or 8-, 16-, or 32-bit on a SDRAM data bus), system configuration jumpers, and PCI and ISA expansion connectors. The ÉlanSC520 microcontroller CDP uses an ATX form factor.

The ÉlanSC520 microcontroller CDP enables you to:

- Develop firmware and application code for the ÉlanSC520-based embedded microcontroller
- Benchmark embedded, network-ready applications on the high performance ÉlanSC520 microcontroller
- Make power measurements
- Experiment with design trade-offs and assemble an ÉlanSC520 microcontroller system using off-the-shelf components.

Features

The ÉlanSC520 microcontroller CDP contains the following features:

- 10/100BaseT Ethernet
- Super I/O peripheral chip containing:
  - Floppy device
  - Two serial devices (one IrDA shared with Serial Port 2)
  - One parallel device
  - Keyboard
  - Mouse
- Three PCI card slots
- Two ISA card slots
- Test Interface Port (TIP) connector
- High-speed UART port
- Low-speed UART port
- Hex LED display
- Logic analyzer connector (AMP MICTOR type)
- SDRAM (two 168-pin DIMM sockets)
- 16-Mbyte on-board Flash memory
- AMDebug™ (JTAG-compliant) test interface tool (connector POD1 or POD2)
- In-circuit emulator (ICE) connector (J10) support using a PROM ICE device
- Synchronous serial interface (SSI)
- Integrated drive electronics (IDE)

Documentation

The *Élan™SC520 Microcontroller Customer Development Platform User's Manual* provides information about the system, features, functions, and interfaces. Additional information can be found in "Suggested Reference Material" on page xiv.

About this Manual

Chapter 1, "Quick Start", describes how to quickly set up and begin using the ÉlanSC520 microcontroller CDP.

Chapter 2, "Features and Functions", describes the features and functions of the ÉlanSC520 microcontroller CDP.

Appendix A, "Jumper and DIP Switch Settings", describes the various jumpers, switches, and settings.

Appendix B, "Resource Assignments", describes the resource assignments for chip select, GPIRQ, GPDMA, PIO, and UART.

A standard index is also included.

Suggested Reference Material

The following AMD documentation may be of interest:

- *Élan™SC520 Microcontroller Register Set Manual*, order #22005
- *Élan™SC520 Microcontroller User's Manual*, order #22004
- *Élan™SC520 Microcontroller Data Sheet*, order #22003
- *Am486® Microprocessor Software User's Manual*, order #18497
- *AMD Test Interface Port Board User's Manual*, order #22505A
- *Am79C973/Am79C975 PCnet™-FAST III Single-Chip10/100 Mbps PCI Ethernet Controller with OnNow Support*, order #21510
- *E86™ Family Products Development Tools CD*, order #21058

For current application notes and technical bulletins, see our World Wide Web page at **www.amd.com**.

The following non-AMD documentation may also be of interest to you:

- *PCI Local Bus Specification*, Production Version, Revision 2.1, June 1, 1995, PCI Special Interest Group, 800-433-5177 (US, 503-693-6232 (International), **www.pcisig.com**.
- *IEEE Std 1148\9.1-1990 Standard Test Access Port and Boundary-Scan Architecture* (order #SH16626-NYF), Institute of Electrical and Electronic Engineers, Inc., 800-678-4333, **www.ieee.org**.
- *PCI System Architecture*, Mindshare, Inc., Third Edition. Reading, MA: Addison-Wesley, 1995, ISBN 0-201-40993-3.
- *ISA System Architecture*, Mindshare, Inc., Third Edition. Reading, MA: Addison-Wesley, 1995, ISBN 0-201-40996-8.
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Third Edition. Wokingham, England: Addison-Wesley, 1995, ISBN 0-201-40399-4.

Documentation Conventions

The *Élan™SC520 Microcontroller Customer Development Platform User's Manual* uses the notational conventions shown in Table 0-1 (unless otherwise noted).

Table 0-1. Notational Conventions

Symbol	Usage
Boldface	Indicates that characters must be entered exactly as shown, except that the alphabetic case is only significant when indicated.
Italic	Indicates a descriptive term to be replaced with a user-specified term.
`Typewriter face`	Indicates computer text input or output in an example or listing.
`EXE`	Indicates a DOS executable file.
`HEX`	Indicates an Intel extended hex file.
`<>`	Encloses a required parameter. To include the information described within the angle brackets, type only the parameters, not the angle brackets themselves.
`[]`	Encloses an optional parameter. To include the information described within the brackets, type only the parameter, not the brackets themselves.
|	Separates alternate choices in a list. Only one of the choices can be entered.

Chapter 1

Quick Start

This chapter provides information to enable you to quickly set up and start using the ÉlanSC520 microcontroller customer development platform (CDP). The following sections describe how to connect, power up, and begin using the board.

The ÉlanSC520 Microcontroller is shipped with a BIOS that has been configured specifically for the chipset used on this platform. The BIOS contains the code that enables the ÉlanSC520 Microcontroller to function as a standard AT-compatible PC, using AT-compatible displays, display adapters, mouse, and keyboards. Details on the BIOS can be found in the online BIOS documentation shipped with your kit.

The ÉlanSC520 Microcontroller can run AT-compatible operating system software. You can start the system with either a bootable floppy disk or an ATA (IDE) hard disk drive that has the pre-installed operating system.

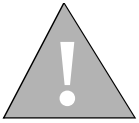
Embedded BIOS software typically supports the configuration of onboard Flash memory as a resident Flash disk (RFD) that can also be set up as a boot device. See the online BIOS manual included with your kit.

For information on how to:

- Set up the ÉlanSC520 microcontroller CDP, refer to “Set-Up Procedure” on page 1-5.
- Boot the ÉlanSC520 microcontroller CDP from a floppy disk, refer to “Starting from a Floppy Disk” on page 1-14.
- Boot the ÉlanSC520 microcontroller CDP from a hard disk drive, refer to “Starting from an IDE Hard Disk Drive” on page 1-15.
- Modify the PromICE interface cable for booting the ÉlanSC520 microcontroller CDP, refer to “Modifying the PromICE Interface Cable for Booting the ÉlanSC520 Microcontroller CDP” on page 1-8. This procedure should be used only with CDP board versions 1.0–1.2.

Additonal information and utilities are available as CodeKit software included with your kit. CodeKit software can also be found at **www.amd.com**.

Setting Up the Élan™SC520 Microcontroller CDP



CAUTION: As with all computer equipment, the ÉlanSC520 microcontroller CDP may be damaged by electrostatic discharge (ESD). Please take proper ESD precautions when handling any board.

WARNING: Read the following before using the Élan™SC520 microcontroller CDP.

Before applying power, the following precautions should be taken to avoid damage or misuse of the board:

- Make sure the power connector JP1 (ATX Power) is plugged into the ÉlanSC520 microcontroller CDP correctly.
  - Refer to Figure 2-2 on page 2-4 for the JP1 (ATX Power) connector location.
- Check the materials that were shipped with your kit for README or errata documentation. Read all the information carefully before continuing.

For current application notes and technical bulletins, refer to the AMD World Wide Web page at **www.amd.com** and follow the link to Embedded Systems.

Set-Up Requirements

The following items are provided with the ÉlanSC520 microcontroller CDP.

- ÉlanSC520 microcontroller (pre-installed)
- CR2032 Lithium battery (pre-installed)
- 64-Mbyte SDRAM DIMM module
- General Software BIOS (pre-installed)
- 34-pin ribbon cable with header (for floppy disk drive)
- 40-pin ribbon cable with header (for IDE drive)
- PCI video card

You must provide the following items:

- PS/2 keyboard
- PS/2 mouse
- Floppy disk drive
- IDE hard disk drive
- ATX power supply (any wattage)
- Color VGA monitor (any size)

To boot from a floppy disk, you must provide at least the following:

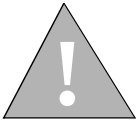
- A PC/AT-compatible 3.5-inch or 5.25-inch floppy disk drive
- A bootable DOS floppy disk

To boot from a hard disk drive, you must provide at least the following:

- An IDE hard disk drive
- PC/AT-compatible operating system (pre-installed on the hard disk drive) (DOS, Microsoft Windows)

For correct configuration, the jumper and DIP switch settings must be set to the default settings. Verify these settings before operating the ÉlanSC520 microcontroller CDP; refer to Appendix A, “Jumper and DIP Switch Settings”.

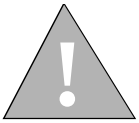
If you install both a floppy disk drive and a hard disk drive, you can boot from either device. Only one boot disk image (floppy disk or hard disk) is required. For example, you can boot from the floppy disk drive, and then install the operating system on a blank hard disk drive.



CAUTION: Use the configuration described here when you first start the ÉlanSC520 microcontroller CDP. Before using other features, read the appropriate sections in Chapter 2, “Features and Functions.”

Set-Up Procedure

NOTE: For block diagram information, refer to Figure 2-1 on page 2-3. For layout and connector locations, refer to Figure 2-2 on page 2-4.



CAUTION: Ensure that all connections and settings are correct before powering up the ÉlanSC520 microcontroller CDP. Incorrect connections or settings can damage the ÉlanSC520 microcontroller CDP.

Perform the following steps to set up the ÉlanSC520 microcontroller CDP:

1. Remove the ÉlanSC520 microcontroller CDP from the shipping carton, and inspect the it to verify that it was not damaged during shipping. The ÉlanSC520 microcontroller CDP contains several jumpers. The following steps assume all jumpers are set to the factory default configuration (settings are listed in "Jumper and DIP Switch Settings" on page A-1).
2. If you are installing a floppy disk drive, perform the following steps:
    a. Inspect the 34-wire, floppy disk drive cable. The red wire along one edge of the ribbon cable indicates wire 1. Most cables have a connector for the board at one end and two or more connectors along the length. There may be two different drive connectors at each location to accommodate different drive types.
    b. Connect one end of the floppy disk drive cable to the 34-pin connector (connector P13) on the ÉlanSC520 microcontroller CDP (with wire 1 oriented towards the LED displays). If there is a twist in one span of the cable, connect the opposite end to the board. Note the pin-1 position.
    c. Connect the other connector on the floppy disk drive cable to the floppy disk drive, just as you would for a standard PC installation. If there is a twist in the cable, the position you use determines whether the drive responds as A or B (typically drive A connects to the end of the cable, beyond the twist). The connector's orientation should be indicated in the drive documentation, or marked near the connector on the drive. Usually wire 1 is oriented towards the drive's power cable connector.
    d. Find one of the 4-wire power connectors from the PC power supply and attach it to the 4-pin connector on the floppy disk drive just as you would for a standard PC installation.

3. If you are installing a hard disk drive, perform the following steps:
    a. Connect the 40-pin hard disk drive cable into the IDE box header (P3). Note the pin-1 position. The red wire along one edge of the ribbon cable indicates wire 1.
    b. Connect one end of the 40-wire IDE cable to the hard disk drive just as you would for a standard PC installation. The connector's orientation should be indicated in the drive documentation, or marked near the connector on the drive. Usually wire 1 is oriented towards the drive's power cable connector.
    c. Connect the other end of the 40-wire IDE cable to the first 40-pin connector (connector P3) on the ÉlanSC520 microcontroller CDP (with wire 1 oriented towards the LED displays).
    d. Find one of the 4-wire power connectors from the PC power supply and attach it to the 4-pin connector on the hard disk drive just as you would for a standard PC installation.
4. Connect the monitor cable from the monitor to the D-connector on the video card just as you would for a standard PC.
5. Connect the ISA VGA or PCI video card into one of the ISA or PCI slots.
6. Connect the SDRAM DIMM module into either J2 or J3.
7. The ÉlanSC520 microcontroller is pre-installed in the ÉlanSC520 microcontroller CDP. If the microcontroller is mounted in a ZIF socket and you need to re-seat or replace the microcontroller, perform the following steps:
    a. Lift the lever-bar of the socket to the vertical position.
    b. Place the ÉlanSC520 microcontroller over the ZIF socket, and then align the golden arrow on the ÉlanSC520 microcontroller with the upper-left corner (pin-A1) of the socket.
    c. Place the ÉlanSC520 microcontroller flat on the ZIF socket, and then lock the lever-bar by pushing it down to the horizontal position.
8. Connect the PS/2 keyboard cable into the J1 lower-socket.

    NOTE: The keyboard and mouse socket positions have changed in board revision 1.4. They were reversed in previous board versions.

9. Connect the PS/2 mouse cable into the J1 upper-socket.
10. Connect the ATX power connector into the JP1 connector.

Configuring the System Setup (BIOS) Setting

Perform the following steps to configure the system setup (BIOS) setting:

1. In the drive assignment order:
    a. Set Drive A: to Floppy Drive 0.
    b. Set Drive C: to IDE 0 (Master 1).
2. In the boot order block:
    a. Set Boot 1st to Drive A:.
    b. Set Boot 2nd to Drive C:.
3. In the IDE drive geometry block, set device IDE0 to “Auto Config, Physical” (typically for drives smaller than 1 Gbyte) or “Auto Config, LBA” (typically for drives 1 Gbyte and larger). If only one IDE device exists, set the other IDE devices to “not installed.”
4. In the floppy disk drive type block, set Floppy 0: to 1.44 Mbyte, 3.5.

Modifying the PromICE Interface Cable for Booting the Élan™SC520 Microcontroller CDP

NOTE: For CDP board versions 1.3 or 1.4, use either of the following jumper settings on jumper JP20, according to your PromICE setup. If your CDP board version is 1.3 or 1.4, skip "Modifying the PromICE Interface Cable Procedure" on page 1-9.

Setting Jumper JP20 According to Your PromICE Setup

Use either of the following jumper settings on jumper JP20 according to your PromICE setup. For the location of jumper JP20, refer to "Élan™SC520 Microcontroller CDP Board Layout" on page 2-4.

- When using Flash memory or a modified PromICE cable, jumper pins 1 and 3 and jumper pins 2 and 4.
- When using PromICE with the original cable (requiring no cable modifications), jumper pins 3 and 5 and jumper pins 4 and 6.

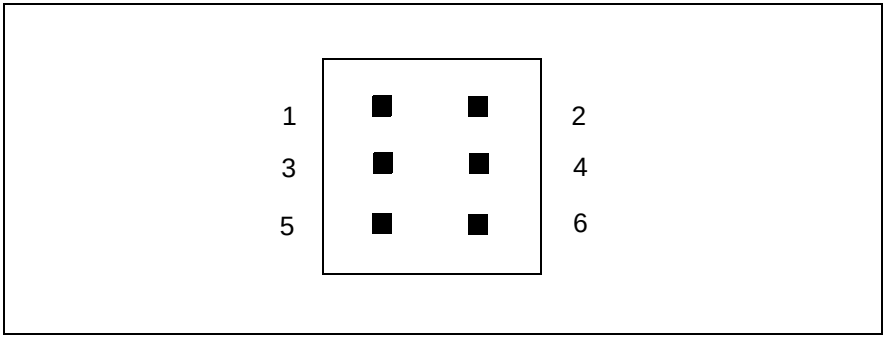


Figure 1-1. Jumper JP20

Modifying the PromICE Interface Cable Procedure

NOTE: This procedure applies only to CDP board versions 1.0–1.2.

The ÉlanSC520 microcontroller CDP enables you to boot either from a ROM/Flash device in a 32-pin DIP socket U17, or from a PromICE (or compatible ROM emulator) that is connected to the 34-pin connector labeled PROM ICE (located adjacent to the diskette 34-pin connector). The boot device is selected by positioning JP18 to pins 1 and 2 for the DIP socket, and to pins 2 and 3 for the PromICE. The PromICE interface for the rev 1.2 ÉlanSC520 microcontroller CDP is designed in strict accordance with pinouts given in the PromICE User's Manual, version 3.4. However, this reference refers to UV-EPROM instead of the more popularly used EEPROM and Flash memory devices, making the ÉlanSC520 microcontroller CDP incompatible.

To fix this condition, perform one of the following tasks:

- Modify a 34-pin floppy disk cable.

  To modify a 34-pin floppy disk cable, perform step 1 on the following pages. Step 1 describes how to remove the extra connectors prior to making the wiring connection changes in step 2. Step 1 is optional, but is recommended.

- Make a standard 34-pin cable by using a cable press to attach a berg connector to both ends of a ribbon cable.

  After making the standard 34-pin ribbon cable, perform step 2 to change the wiring connections.

1. To modify a 34-pin floppy disk cable, perform the following steps:

   The floppy disk cable contains extra connectors that are not required for this application. After cutting off the extra connectors, the modified cable contains the correct connectors that are properly keyed for the PromICE application.

NOTE: If you are using a newer type of floppy disk cable (not containing any card-edge interface connectors), perform step 1.b. instead of step 1.a.

   a. If you are using an older type of floppy disk cable (containing card-edge interface connectors), use a razor knife or scissors to cut the cable as shown in Figure 1-2, and then proceed to step 2 to make the required wiring connection changes.

      After cutting the cable, make sure none of the exposed wires at the edge of the cut cable are touching.

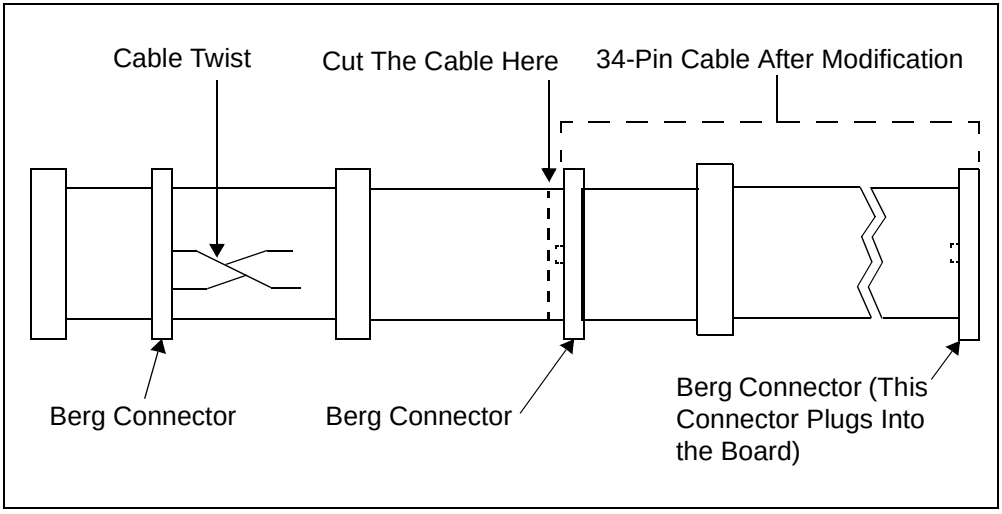


Figure 1-2. Older Type of 34-Pin Floppy Disk Cable

b. If you are using a newer type of floppy disk cable (not containing any card-edge interface connectors), use a razor knife or scissors to cut the cable as shown in Figure 1-3, and then proceed to step 2 to make the required wiring connection changes.

After cutting the cable, make sure none of the exposed wires at the edge of the cut cable are touching.

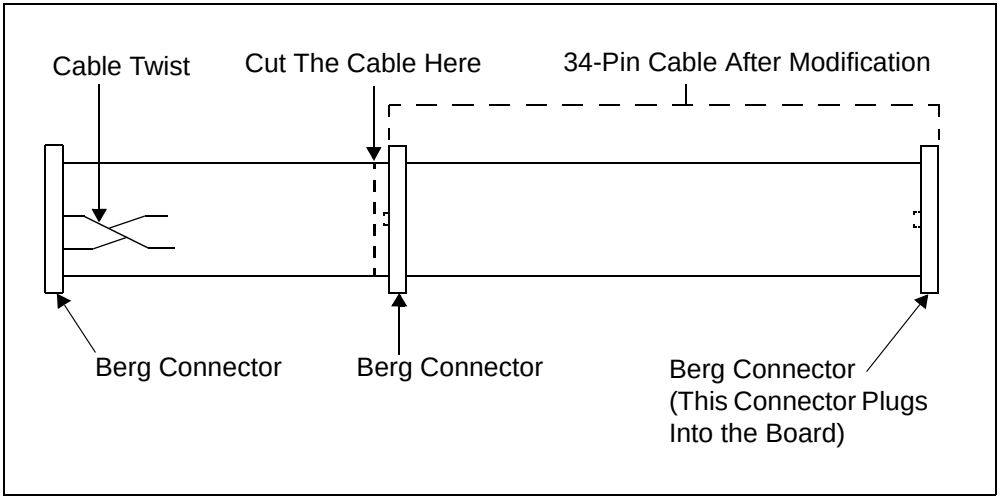


Figure 1-3. Newer Type of 34-Pin Floppy Disk Cable

NOTE: The information provided in Step 2 and Figure 1-4 assumes that you are supporting the emulation of a 256K Flash device, because address lines A18 and A19 are tied high.

2. To change the wiring connections on the 34-pin cable, perform the following steps:

   a. Being careful not to cut into the insulation of the wires, use a razor knife to separate wires 2, 3, 4 and 5 from each other and from the other cable wires, as shown in Figure 1-4.

   b. Cut wires 2, 3, 4, and 5, as shown in Figure 1-4.

c. Remove about a half-inch of insulation from the ends of the following wires:

   Wires 2, 3, 4, and 5 on the side of the cable that connects to the PromICE

   Wire 4, on the side of the cable that connects to the ÉlanSC520 microcontroller CDP.

NOTE: Do not remove the insulation from wires 2, 3, and 5 located on the side of the cable that connects to the ÉlanSC520 microcontroller CDP.

d. Connect exposed wires 2, 3, and 4 by twisting the wire-ends together.

e. This connection provides a pull-up for A18 and A19 to VCC because they are not used in addresses 256K–1 and below.

f. Connect exposed wire 4 to exposed wire 5 by twisting the wire-ends together.

g. This connection fixes the compatibility issue originating in the PromICE user's manual.

h. To ensure that the exposed connected wires do not touch other wires, use electrical tape to cover the exposed wires.

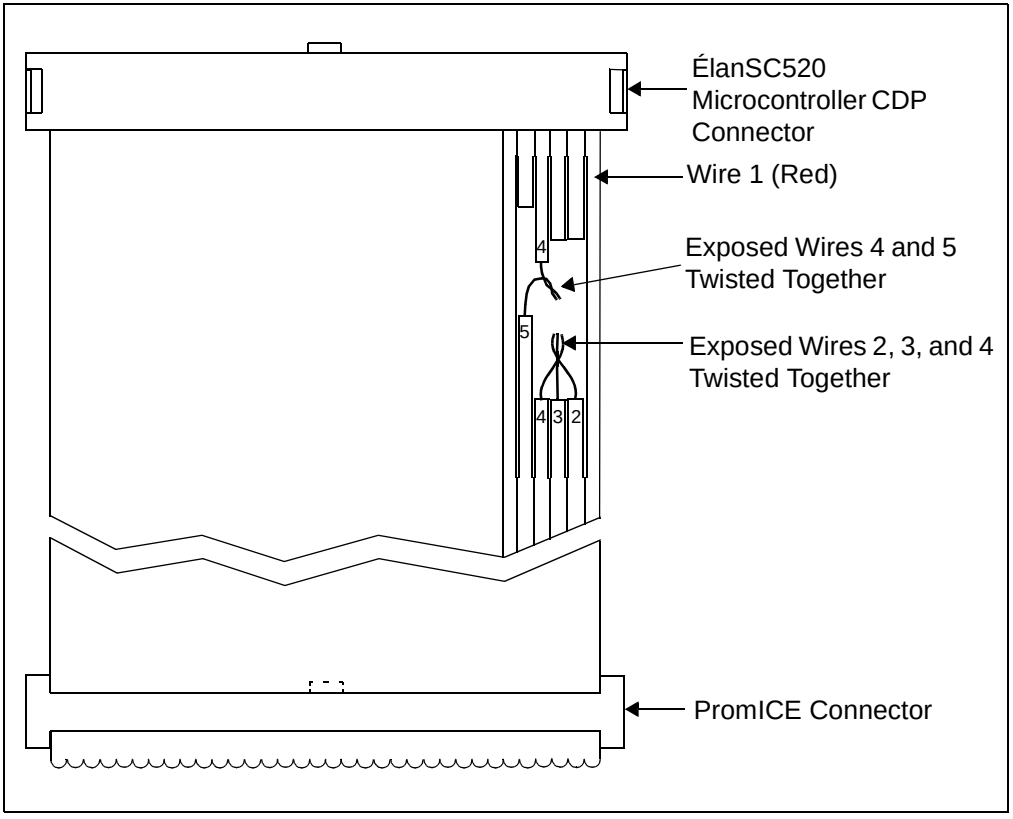
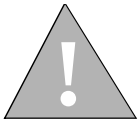


Figure 1-4. Wiring Connection Changes on 34-Pin Ribbon Cable

Starting from a Floppy Disk

Use the following steps to start the ÉlanSC520 microcontroller CDP from a bootable floppy disk:

1. Make sure you have installed the ÉlanSC520 microcontroller CDP correctly as described in “Set-Up Procedure” on page 1-5.



CAUTION: Failure to verify the power supply connections can result in total destruction of the ÉlanSC520 microcontroller CDP.

2. Plug the VGA monitor into an electrical outlet and turn it on.
3. Insert a bootable DOS floppy disk (not included) in the floppy disk drive.
4. Apply power to the ÉlanSC520 microcontroller CDP by connecting the PC power supply to an electrical outlet. If the power supply is equipped with a switch, turn it on. Then turn on the power switch on the CDP.

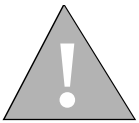
   The power supply fan should start running, and the port 80h and 680h LEDs should start to display power-on self-test (POST) status codes. Then the speaker should beep and the monitor should start displaying startup information.
5. The first time you start the system, the BIOS might display a message reporting a CMOS error or some other BIOS configuration problem. Follow the instructions shown on the screen to enter the Setup utility. Once you are in the Setup utility, you can set the system’s date, time, startup drive, and other options.

   For more information on the included BIOS, including power-on status codes, see the online BIOS manual included with your kit.
6. Save and exit the setup utility.
7. The system should now boot from the DOS floppy disk just like a standard PC.

Starting from an IDE Hard Disk Drive

Use the following steps to start up the ÉlanSC520 microcontroller CDP from an IDE hard disk drive on which you have pre-installed an operating system (while it was connected to another PC):

1. Make sure you have installed the ÉlanSC520 microcontroller CDP correctly as described in “Set-Up Procedure” on page 1-5.



CAUTION: Failure to verify the power supply connections can result in total destruction of the ÉlanSC520 microcontroller CDP.

2. Plug the VGA monitor into an electrical outlet and turn it on.
3. If a floppy disk drive is installed, make sure it is empty.
4. Apply power to the ÉlanSC520 microcontroller CDP by connecting the PC power supply to an electrical outlet. If the power supply is equipped with a switch, turn it on. Then turn on the power switch on the CDP.

   The power supply fan and hard disk should start running, and the port 80h and port 680h LEDs should start to display power-on self-test (POST) status codes. Then the speaker should beep and the monitor should start displaying startup information.
5. The first time you start the system, the BIOS might display a message reporting a CMOS error or some other BIOS configuration problem. Follow the instructions shown on the screen to enter the Setup utility. Once you are in the Setup utility, you can set the system’s date, time, startup drive, and other options.

   For more information on the included BIOS, including power-on status codes, see the online BIOS manual included with your kit.
6. Save and exit the setup utility.
7. The system should now boot using the operating system on the hard disk drive.

Chapter 2

Features and Functions

The ÉlanSC520 microcontroller customer development platform (CDP) is designed for validating features and functionality, qualifying specifications on the ÉlanSC520 microcontroller, and for developing customer applications.

For more information about the components of the ÉlanSC520 microcontroller CDP, refer to the following sections:

- In-circuit emulator (ICE) connector support using PROM ICE, page 2-17
- Synchronous serial interface (SSI), page 2-17
- Integrated Drive Electronics (IDE), page 2-17
- Daughter modules: 32-Mbyte Flash memory module and TIP module, page 2-18

Block Diagram and Component Locations

The following figures show the features and layout of the ÉlanSC520 microcontroller customer development platform:

- Figure 2-1 on page 2-3 shows a block diagram and a summary of the functions of the features.
- Figure 2-2 on page 2-4 shows the board layout and the locations of the components.
- Figure 2-3 on page 2-5 shows the connectors on the ÉlanSC520 microcontroller CDP.

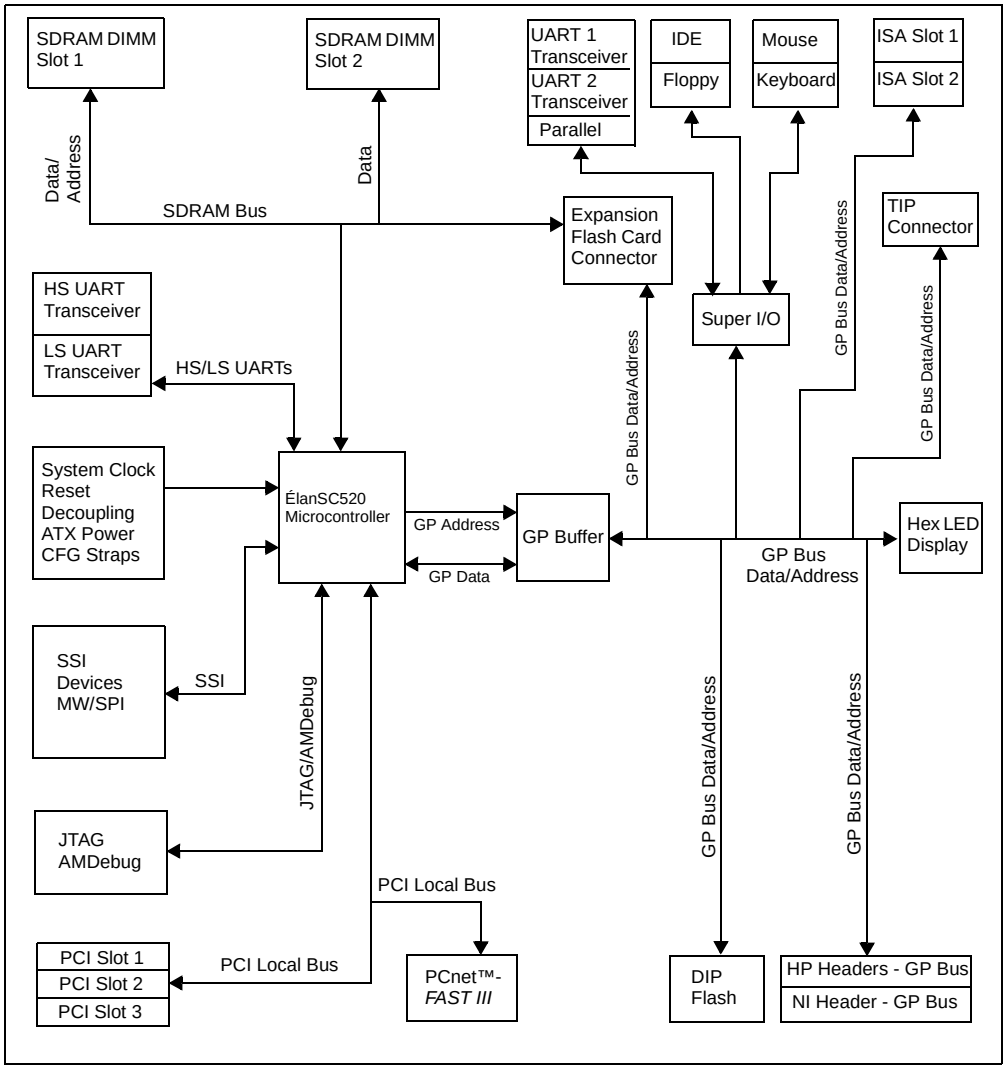


Figure 2-1. Élan™SC520 Microcontroller CDP Block Diagram

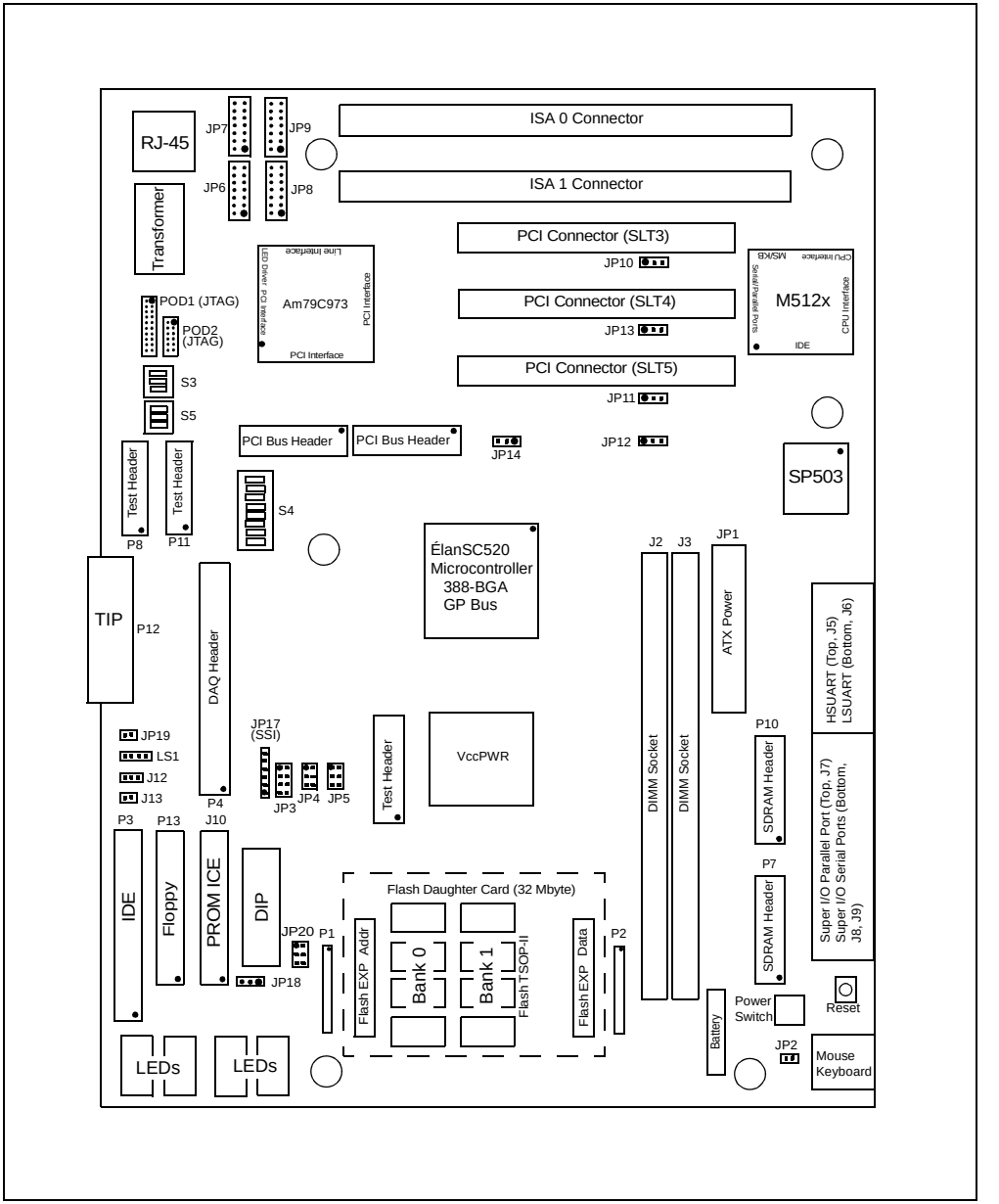
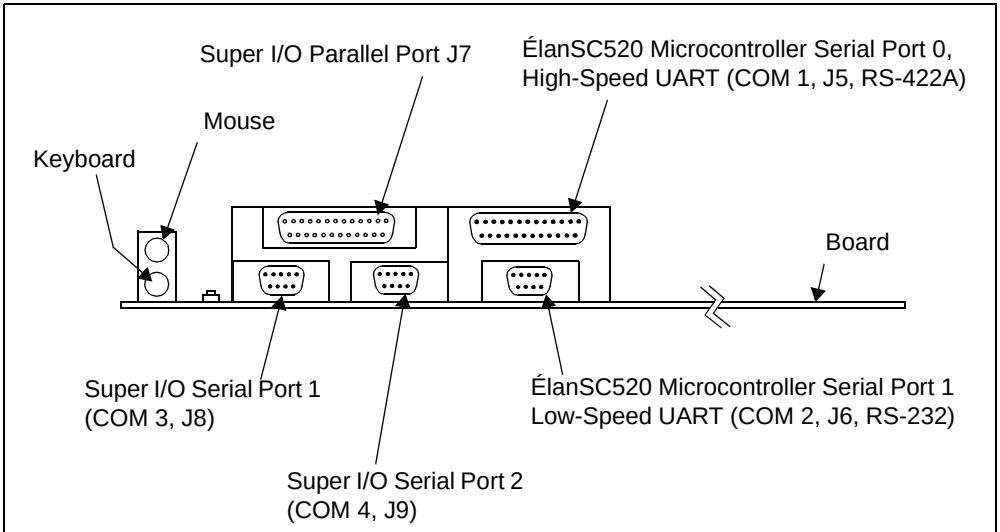


Figure 2-2. Élan™SC520 Microcontroller CDP Board Layout



NOTE: The mouse and keyboard connector positions are reversed (keyboard connector on top) in CDP board versions 1.3 and earlier.

Figure 2-3. Connectors on the Élan™SC520 Microcontroller CDP

ATX-style headers are provided near the IDE connector for the following chassis connections: reset switch JP19, speaker LS1, power status LED J12, and HD (IDE) status LED J13.

Descriptions

This chapter describes the features and functions of the ÉlanSC520 microcontroller CDP. For additional information about the ÉlanSC520 microcontroller CDP, refer to the following sections:

- Appendix A, “Jumper and DIP Switch Settings” for information about jumper and switch settings.
- Appendix B, “Resource Assignments” for information about chip select, GPIRQ, GPDMA, PIO on CDP, and UART assignments.

For component layout and locations, refer to Figure 2-2 on page 2-4.

Élan™SC520 Microcontroller

The Élan™SC520 microcontroller is a full-featured microcontroller developed for the general embedded market. Designed for medium- to high-performance applications in the telecommunications, data communications, and information appliance markets, the ÉlanSC520 microcontroller is particularly well suited for applications requiring high throughput combined with low latency and low cost.

The ÉlanSC520 microcontroller utilizes a high-performance, industry-standard, 33-MHz, 32-bit PCI bus for high-bandwidth I/O peripherals. The microcontroller also contains a simple 8- and 16-bit general-purpose (GP) bus for a glueless connection to low-bandwidth peripherals. The GP bus supports most legacy ISA peripherals.

The ÉlanSC520 microcontroller utilizes the industry-standard x86 architecture instruction set that enables compatibility across a variety of performance levels from the low-end 16-bit Am186 processors to the high-end AMD-K6E™ family processors. Software written for the x86 architecture family is compatible with the ÉlanSC520 microcontroller.

With the AMDebug technology, the ÉlanSC520 microcontroller provides a full-featured, high-performance in-circuit emulation capability that enables you to test and debug your software earlier in the design cycle.

In addition to these features, the ÉlanSC520 microcontroller provides a high-performance SDRAM controller, ROM/Flash controller, flexible address-mapping hardware, general-purpose bus interface, clock generation, integrated peripherals, JTAG boundary scan test interface, and various system test and debug features.

For more information about the ÉlanSC520 microcontroller, refer to the *Élan™SC520 Microcontroller Data Sheet*, *Élan™SC520 Microcontroller User's Manual*, and the *Élan™SC520 Microcontroller Register Set Manual*, which are included in your kit.

10/100BaseT Ethernet Controller

The ÉlanSC520 microcontroller CDP contains the Am79C973 PCnet™-*FAST III* Ethernet controller chip. The high-performance 10/100BaseT Ethernet port enables the ÉlanSC520 microcontroller CDP to connect to a high-bandwidth LAN. External magnetics for a built-in transceiver (PHY) are utilized for a full-duplex implementation with an RJ45 10/100BaseT connector.

The Am79C973 device logically resides on the PCI bus and is wired for full bus-mastering capability. The PCI address bit 27 is used for the $\overline{\text{IDSEL}}$ pin of the Am79C973 device. The Am79C973 registers can be configured by either the PCI configuration space mechanism, or by downloading the configuration information from a dedicated serial EEPROM (part U30). A 4K serial EEPROM is used so that other board-level configuration information can be stored with the Am79C973 device configuration parameters. CodeKit software is provided to read and write the serial EEPROM so it can be used for a wide variety of applications. Figure 2-4 shows a block diagram of the 10/100BaseT Ethernet.

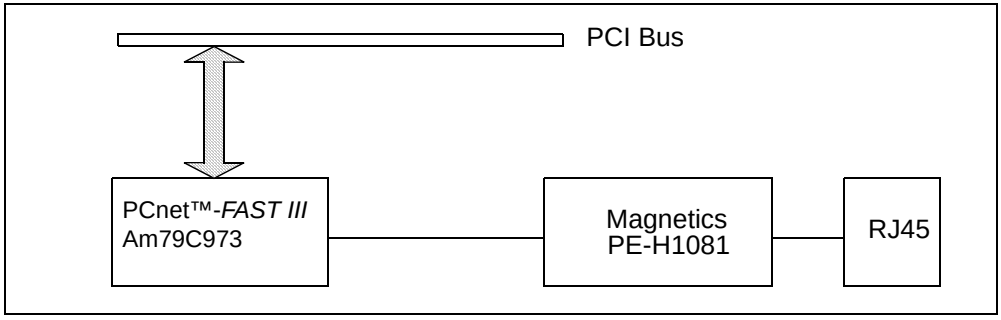


Figure 2-4. On-Board 10/100 Mbit/s Ethernet Controller Block Diagram

Super I/O

The ALi Super I/O Chip (Acer Laboratories, Inc., P/N M512x) provides two 16550 compatible UARTs (serial ports) that operate at baud rates up to 1.15 Mbit/s, one parallel port, a floppy disk interface, IrDA interface (shared with COM4), and a keyboard/mouse controller.

NOTE: The two serial ports (COM3 and COM4) of the Super I/O are not the same as the two serial ports (COM1 and COM2) of the ÉlanSC520 microcontroller.

The two serial ports facilitate software development and other communications. External transceivers are needed for the serial ports and IrDA interface. LEDs indicate TX and RX activity on both serial ports. Both serial ports are routed to industry-standard DB9 and RS-232 connectors on the ÉlanSC520 microcontroller CDP and are named as COM3 and COM4.

NOTE: The BIOS included with CDP version 1.4 maps the Super I/O UARTs to COM3 and COM4. Earlier BIOS versions, used on boards with microcontroller revisions A0 and A1, disabled the microcontroller's UARTs and mapped the Super I/O UARTs to COM1 and COM2 instead.

The EPP-supported parallel port is routed to an industry-standard DB25 connector. The keyboard and mouse use PS/2 connectors. Table 2-1 shows the DMA channels and the IRQs for the Super I/O devices. Figure 2-5 on page 2-9 shows the block diagram of the Super I/O configuration.

Table 2-1. DMA Channels and IRQs Reserved for Super I/O

Devices	DMA Channels Reserved for Super I/O	IRQs Reserved for Super I/O
FDD	DRQ0/$\overline{\text{DACK0}}$	IRQ6
EPP (Parallel Port)	DRQ0/$\overline{\text{DACK0}}$	IRQ7
SIO1	—	IRQ4
SIO2	—	IRQ3
KB (Keyboard)	—	IRQ1
Mouse	—	IRQ12

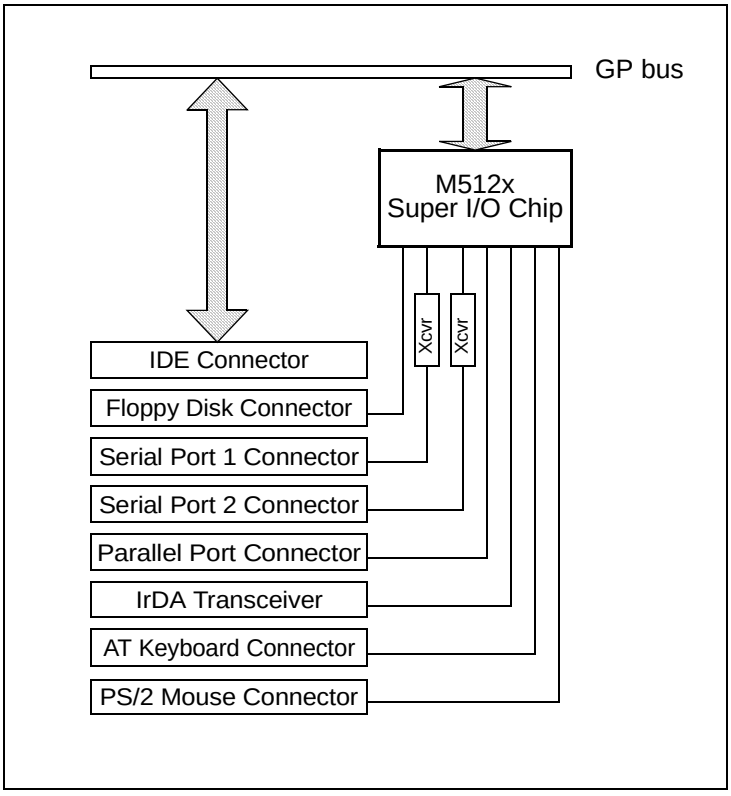


Figure 2-5. Super I/O Block Diagram

PCI Card Slots

Three industry-standard PCI card slots are provided to enable you to plug in most PCI-V2.2-compliant peripheral cards to speed up their design process and to reduce development time for your product. The ÉlanSC520 microcontroller CDP supports up to five PCI masters. The PCI card slots are 5V-capable (only).

ISA Card Slots (General-Purpose Bus Slots)

Two industry-standard ISA card slots enable you to plug in a variety of off-the-shelf, low-cost ISA peripheral cards to achieve design simplicity and reduced development time.

Test Interface Port (TIP) Connector

The 60-pin, test interface port (TIP) connector enables you to use the optional module to develop software and debug hardware. The TIP board contains a rich set of peripherals used for debugging, diagnostics, evaluation, and reference design. The TIP board is available through your AMD sales contact.

Logic Analyzer Connector

The logic analyzer connector enables you to use a logic analyzer to debug the application design. All signals from the ÉlanSC520 microcontroller are connected to the logic analyzer connectors, except for crystals, CLKPCIOUT (PCI clocks), and CLKMEMOUT (SDRAM clocks).

AMD supports the Hewlett Packard (HP) and Tektronix logic analyzer connector without shrouds and the HP connector with shrouds. Both types of connectors attach to a specific Mictor connector on the ÉlanSC520 microcontroller CDP, depending on what feature is being tested.

High-Speed UART

The High-Speed UART (port 0, COM1) is embedded in the ÉlanSC520 microcontroller. The High-Speed UART port enables you to communicate at a speed of up to 1.152 Mbit/s through balanced RS-422A-compliant serial ports with other serial communication equipment, for a longer distance and faster speed. You can make the High-Speed UART port pin-compatible with the RS-232 by setting the external pin strap. For connector location, refer to Figure 2-2 on page 2-4 and Figure 2-3 on page 2-5.

NOTE: The BIOS included with CDP version 1.4 maps the microcontroller's UARTs to COM1 and COM2. Earlier BIOS versions, used on boards with microcontroller revisions A0 and A1, disabled the microcontroller's UARTs and mapped the Super I/O UARTs to COM1 and COM2 instead.

Low-Speed UART

The low-speed UART (port 1, COM2) is embedded in the ÉlanSC520 microcontroller. The low-speed UART port enables you to communicate at a lower speed of up to 460 Kbit/s through a single-ended RS-232-compliant serial port. The low-speed UART is capable of high-speed, like the High-Speed UART port, but is restricted through a low-speed transceiver that limits this High-Speed UART channel to a lower speed for the purpose of communicating with specific serial communication equipment.

NOTE: The BIOS included with CDP version 1.4 maps the microcontroller's UARTs to COM1 and COM2. Earlier BIOS versions, used with microcontroller revisions A0 and A1, disabled the microcontroller's UARTs and mapped the Super I/O UARTs to COM1 and COM2 instead.

Hexadecimal LED Display

The hexadecimal LED display is a single-byte (two digits) hexadecimal LED address at 80h and 680h. The hexadecimal LED display (error code display) provides indications for CPU status as well as debugging status, which improves the debugging process.

Memory

The memory on the ÉlanSC520 microcontroller CDP consists of SDRAM and Flash memory.

SDRAM

The ÉlanSC520 microcontroller CDP can have a maximum of four rows on two DIMMs that connect into two industry-standard, 168-pin DIMM sockets. The DIMMs are 64-bit wide main memory, using 16/64-Mbit x 8 SDRAM chips. Note that the SDRAM DIMMs used are 64-bits wide only because they are configured as two rows each. Error Correction Code (ECC) is not supported on the full SDRAM DIMMs; the ECC supports only half of the DIMM capacity. Figure 2-6 on page 2-13 shows the SDRAM configuration diagram.

The two DIMM sockets are wired to enable you to install a combination of single- or double-sided DIMMs. This configuration yields a total of four rows of SDRAM memory, using the two DIMM sockets. You can adjust the timing of the SDRAM interface by using the registers in the ÉlanSC520 microcontroller.

Table 2-2 shows the SDRAM signals and the descriptions.

Table 2-2. SDRAM Signals

SDRAM Signal	Description
CS0–CS3	Chip select signal for each row on DIMM
MA0–MA12	Memory address signals
MD0–MD31	Memory data signals
BA0–BA1	Memory bank select signal for each memory chip
DQM0–DQM3	Data byte masks

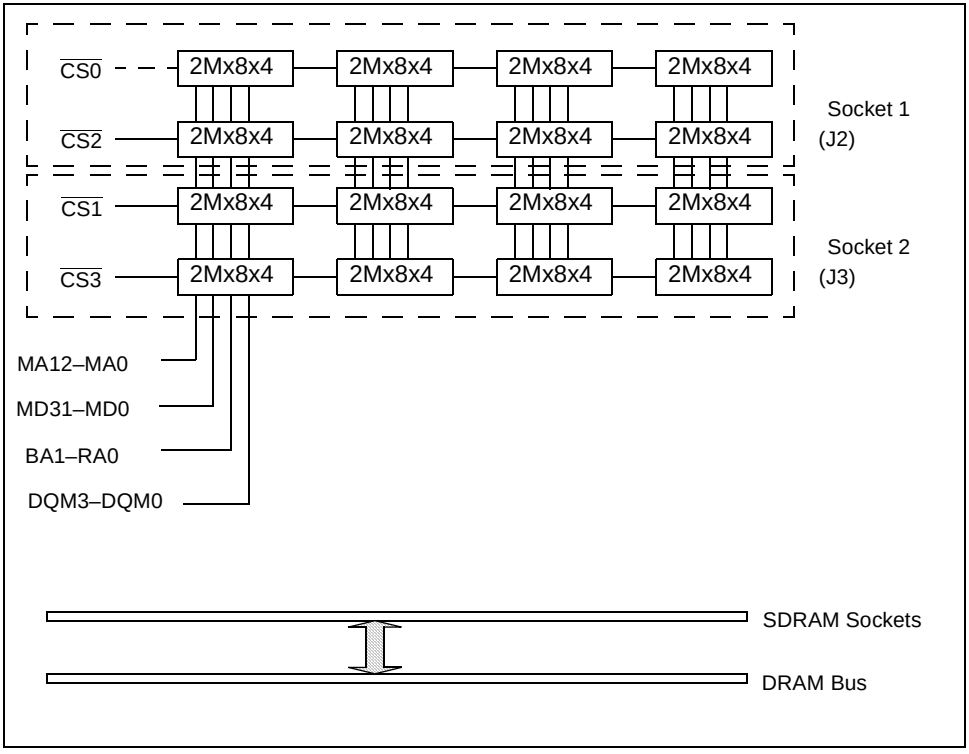


Figure 2-6. SDRAM Configuration Diagram

Flash Memory

The on-board Flash memory uses the AMD Am29LV017B and consists of following configuration:

- Two 8-Mbyte banks in a 32-bit data width consisting of eight 2-Mbit x 8 devices
- The Flash memory is used for the BIOS and/or Execute-In-Place memory that interfaces to the ÉlanSC520 microcontroller only through the SDRAM data bus MD31–MD0 or the residential Flash disk (RFD).
- An additional two banks of Flash/ROM is optionally available on a 32-Mbyte daughter module that can be configured to interface to either the 32-bit SDRAM MD bus (with 8/16/32-bit data width (x32 is only available when data bus is selected on SDRAM MD31–MD0 and selected by $\overline{\text{BOOTCS}}$, $\overline{\text{ROMCS1}}$, or $\overline{\text{ROMCS2}}$)) or with the 16-bit GP bus (with 8- or 16-bit selectable).

$\overline{\text{BOOTCS}}$ can be assigned to each Flash bank. $\overline{\text{ROMCS1}}$ and $\overline{\text{ROMCS2}}$ can be assigned to the 16-Mbytes on-board Flash bank and/or the 32-Mbyte Flash daughter card. Flash ROMs are configured as 32-bit wide on both the on-board and daughter modules. If the Flash memory is set as 8-bit or 16-bit data width, the higher bytes are not accessible on the ÉlanSC520 microcontroller CDP. The ÉlanSC520 microcontroller CDP demonstrates the ability of only sizing the data width for ROM access. The user can configure it in any bus size to access the entire ROM space by rearranging the address bus for $\overline{\text{BOOTCS}}$, $\overline{\text{ROMCS1}}$, and $\overline{\text{ROMCS2}}$.

The Flash ROM x8 DIP is connected on the GP bus and can be selected only by $\overline{\text{BOOTCS}}$. The Flash ROM x32 onboard memory is connected only on SDRAM MD31–MD0, and it can be selected by $\overline{\text{BOOTCS}}$, $\overline{\text{ROMCS1}}$, and $\overline{\text{ROMCS2}}$.

The Flash ROM daughter module contains configuration jumpers. Users can configure the module as x8, x16, x32 data width on the GP bus (GPD15–GPD0) or the SDRAM Bus (MD31–MD0).

Figure 2-7 on page 2-15 shows the Flash memory configuration supported by the ÉlanSC520 microcontroller CDP.

Figure 2-8 on page 2-16 shows a Flash memory configuration block diagram.

Table 2-3 on page 2-16 shows the signals, inputs, and outputs for each type of memory.

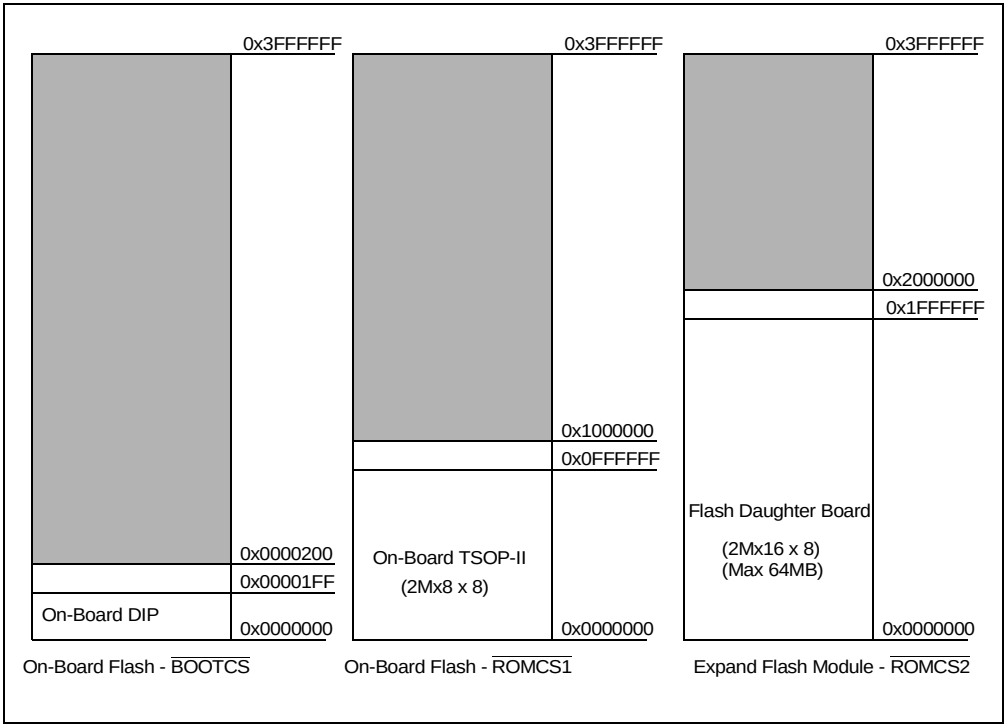


Figure 2-7. Flash Memory Configuration for Élan™SC520 Microcontroller CDP

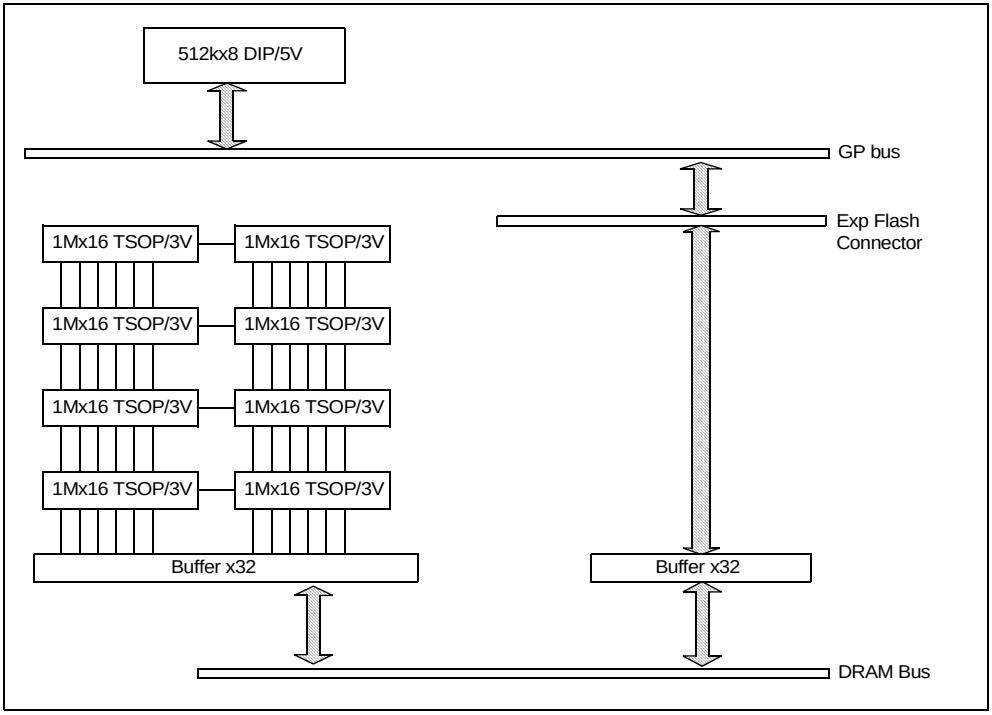


Figure 2-8. Flash Memory Configuration Block Diagram

Table 2-3. Chip Select ($\overline{CS}$) Decoder Address Space

	Signal Name	Number of Outputs	Inputs Associated With
SDRAM	SCS3–SCS0	3–0	—
Flash/ROM	$\overline{BOOTCS}$	1	GPA25–GPA0, $\overline{BOOTCS}$, CFG2–CFG0
	$\overline{ROMCS1}$	1	GPA25–GPA0, $\overline{ROMCS1}$, CFG2–CFG0
	$\overline{ROMCS2}$	1	GPA25–GPA0, $\overline{ROMCS2}$, CFG2–CFG0

AMDebug™ Tool

This in-system test feature is a standard JTAG-compliant test interface. The JTAG utilizes two types of 2-mm connectors—one 20-pin full version (POD1) and one 12-pin simple version (POD2). Both connectors are used for the AMDebug tool.

In-Circuit Emulator (ICE) Connector

The in-circuit emulator (ICE) connector (J10) is used to speed up the design development of application software. The ICE connector is a 34-pin, 1/10-inch box header and is supported by PROM ICE.

Synchronous Serial Interface

The microcontroller's synchronous serial interface (SSI) is populated with a 6-pin, 1/10-inch center SIP connector (JP17) that can communicate with an external device.

In addition, two on-board EEPROM devices are populated on the SSI: one synchronous peripheral interface (SPI), and one MICROWIRE™ peripheral. These EEPROM devices contain no relevant data when the CDP is shipped. They are provided to demonstrate the use of the SSI port with these device types. They can be freely written to or read using the SSI CodeKit software included with your kit, or downloaded from **www.amd.com**.

Integrated Drive Electronics (IDE)

One IDE channel supports two IDE devices: one master and one slave. Usually, the bootable device is set on the master and all other devices reside on the slave. The IDE uses the GP-bus.

Header J13 is provided near the IDE connector to allow connection of an external drive status LED.

Optional Daughter Modules

The ÉlanSC520 microcontroller CDP can interface with two optional daughter modules: the 32-Mbyte Flash memory module and the test interface port (TIP) module. The 32-Mbyte Flash memory module provides additional memory for developing and testing applications. The TIP provides an additional resource for testing and debugging applications, diagnostics, and hardware. The TIP module is available through your AMD sales contact.

Appendix A

Jumper and DIP Switch Settings

Each section in this appendix provides information about settings and operating state descriptions for the respective components. For locations of the various jumpers and DIP switches, refer to Figure 2-2 on page 2-4.

Jumper Settings

The following information provides the jumper settings and pin locations for the various jumpers.

Jumper JP2

The following settings indicate the possible configurations for jumper JP2. Figure A-1 shows the jumper pins and the default setting for jumper JP2.

- To set to On or connect to chassis power supply, jumper pins 1 and 2.
- When using the on-board power supply, pins 1 and 2 are not jumpered.

NOTE: Jumper JP2 is not meant to be used as an external power switch connector. If it is used to connect to an external switch, an on/off toggle switch must be used (not the momentary-contact type typically used in an ATX chassis).

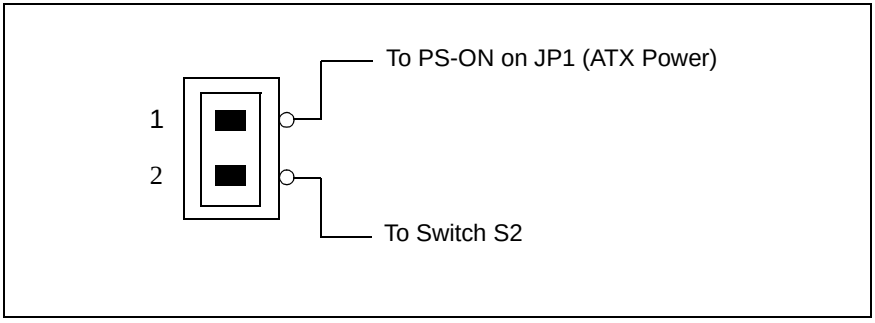


Figure A-1. Jumper JP2 Default Setting

Jumper JP3

The following settings indicate the possible configurations for jumper JP3. Figure A-2 shows the jumper pins and the default setting for jumper JP3.

NOTE: When a row of jumper pins (either pins 1 and 2, pins 3 and 4, or pins 5 and 6) are jumpered on JP3, jumper pins on the same row of JP4 and JP5 cannot be jumpered. For example, if pins 1 and 2 of JP3 are jumpered, then pins 1 and 2 of JP4 and JP5 cannot be jumpered. Only one pair (row) of jumper pins can be jumpered on JP3.

- To boot from the on-board Flash bank 0, jumper pins 1 and 2.
- To boot from the on-board Flash bank 1, jumper pins 3 and 4.
- To boot from the expansion Flash board, jumper pins 5 and 6.
- To boot from the DIP Flash memory, jumper pins 7 and 8 (shown in Figure A-2).

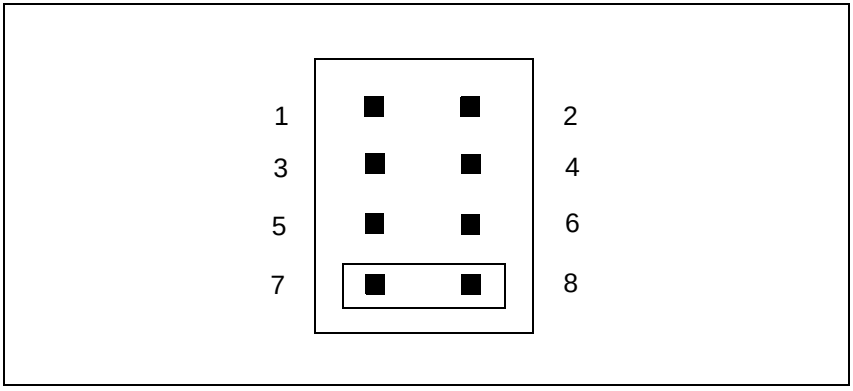


Figure A-2. Jumper JP3 Default Setting

Jumper JP4

The following settings indicate the possible configurations for jumper JP4. Figure A-3 shows the jumper pins and the default setting for jumper JP4.

NOTE: When a row of jumper pins (either pins 1 and 2, pins 3 and 4, or pins 5 and 6) are jumpered on JP4, jumper pins on the same row of JP3 and JP5 cannot be jumpered. For example, if pins 1 and 2 of JP4 are jumpered, then pins 1 and 2 of JP3 and JP5 cannot be jumpered.

- To select $\overline{\text{ROMCS1}}$ for accessing the on-board Flash bank 0, jumper pins 1 and 2 (shown in Figure A-3).
- To select $\overline{\text{ROMCS1}}$ for accessing the on-board Flash bank 1, jumper pins 3 and 4.
- To select $\overline{\text{ROMCS1}}$ for accessing the expansion Flash board, jumper pins 5 and 6.

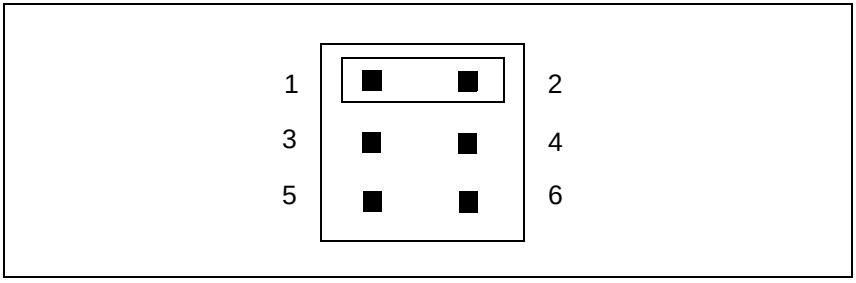


Figure A-3. Jumper JP4 Default Setting

Jumper JP5

The following settings indicate the possible configurations for jumper JP5. Figure A-4 shows the jumper pins and the default setting for jumper JP5.

NOTE: When a row of jumper pins (either pins 1 and 2, pins 3 and 4, or pins 5 and 6) are jumpered on JP5, jumper pins on the same row of JP3 and JP4 cannot be jumpered. For example, if pins 1 and 2 of JP5 are jumpered, then pins 1 and 2 of JP3 and JP4 cannot be jumpered.

- To select $\overline{\text{ROMCS2}}$ for accessing the on-board Flash bank 0, jumper pins 1 and 2.
- To select $\overline{\text{ROMCS2}}$ for accessing the on-board Flash bank 1, jumper pins 3 and 4 (shown in Figure A-4).
- To select $\overline{\text{ROMCS2}}$ for accessing the expansion Flash board, jumper pins 5 and 6.

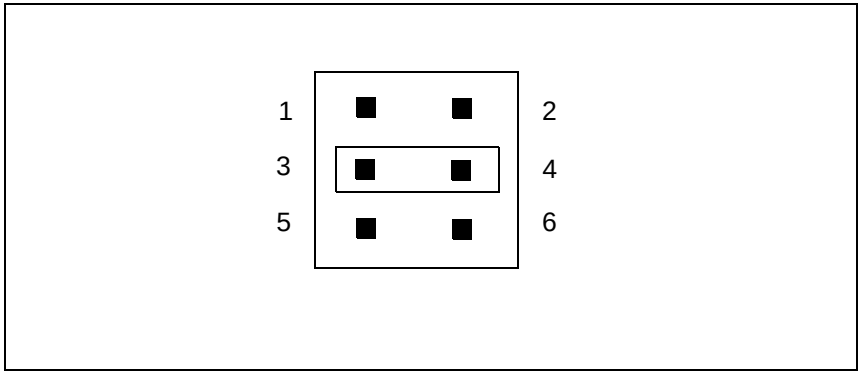


Figure A-4. Jumper JP5 Default Setting

ISA DMA Selection, Jumpers JP6–JP9

The ÉlanSC520 Microcontroller supports two DMA channels via its GPDRQ0, $\overline{\text{GPDACK0}}$, GPDRQ1, and $\overline{\text{GPDACK1}}$ signals. The ISA-compatible signaling on the ISA interface provides paths for seven DMA channels (0–3 and 5–7), which are shared by attached devices. Jumpers JP6, JP7, JP8, and JP9 allow you to route any one ISA-bus DMA channel to either of the microcontroller's two DMA channels. Figure A-5 shows the pin numbering for these jumpers.

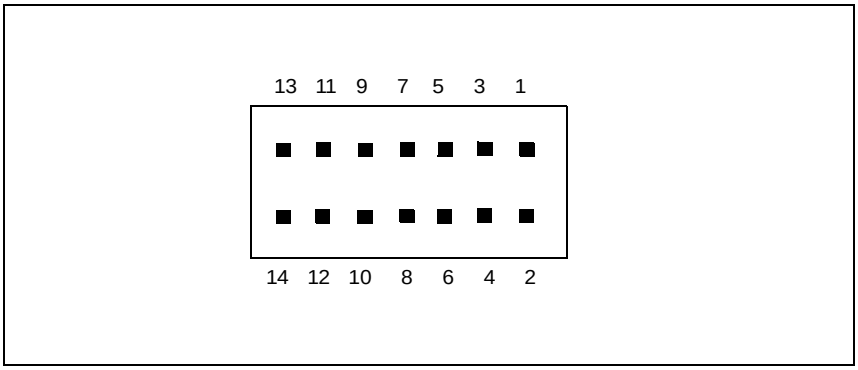


Figure A-5. Jumper JP6, JP7, JP8, and JP9 Pin Numbering

Jumper JP6

Jumper JP6 is used to route one ISA-compatible DRQn channel from the PC/104-Plus connector to the microcontroller's GPDRQ0 input. The following settings indicate the possible configurations for jumper JP6.

- To route ISA DRQ0 to microcontroller GPDRQ0, jumper pins 1 and 2.
- To route ISA DRQ1 to microcontroller GPDRQ0, jumper pins 3 and 4.
- To route ISA DRQ2 to microcontroller GPDRQ0, jumper pins 5 and 6.
- To route ISA DRQ3 to microcontroller GPDRQ0, jumper pins 7 and 8.
- To route ISA DRQ5 to microcontroller GPDRQ0, jumper pins 9 and 10.
- To route ISA DRQ6 to microcontroller GPDRQ0, jumper pins 11 and 12.
- To route ISA DRQ7 to microcontroller GPDRQ0, jumper pins 13 and 14.

Jumper JP7 must be used to route the corresponding $\overline{\text{DACKx}}$ signal (i.e., the selected channel number must match, for example DRQ0 and $\overline{\text{DACK0}}$). Also, the channel number selected must be different from the channel selected by JP8 and JP9 (if any). Figure A-6 shows the default signal routing for jumper JP6, with ISA DRQ5 routed to GPDRQ0.

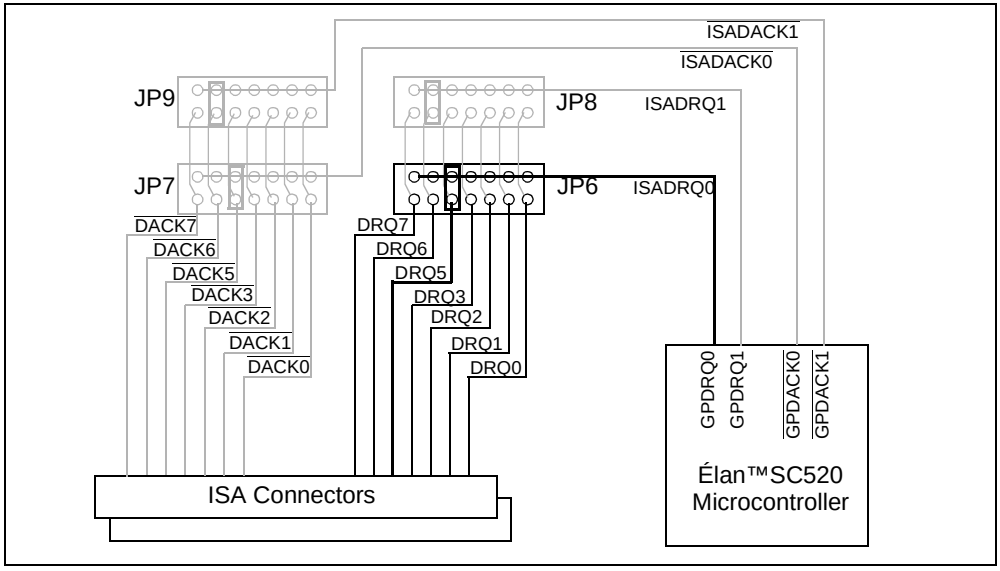


Figure A-6. Jumper JP6 Default Routing

Jumper JP7

Jumper JP7 is used to route one ISA-compatible $\overline{\text{DACKn}}$ channel from the PC/104-Plus connector to the microcontroller's $\overline{\text{GPDACK0}}$ input. The following settings indicate the possible configurations for jumper JP7.

- To route ISA $\overline{\text{DACK0}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 1 and 2.
- To route ISA $\overline{\text{DACK1}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 3 and 4.
- To route ISA $\overline{\text{DACK2}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 5 and 6.
- To route ISA $\overline{\text{DACK3}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 7 and 8.
- To route ISA $\overline{\text{DACK5}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 9 and 10.
- To route ISA $\overline{\text{DACK6}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 11 and 12.
- To route ISA $\overline{\text{DACK7}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 13 and 14.

Jumper JP6 must be used to route the corresponding DRQx signal (i.e., the selected channel number must match, for example DRQ0 and $\overline{\text{DACK0}}$). Also, the channel number selected must be different from the channel selected by JP8 and JP9 (if any). Figure A-7 shows the default signal routing for jumper JP7, with ISA $\overline{\text{DACK5}}$ routed to $\overline{\text{GPDACK0}}$.

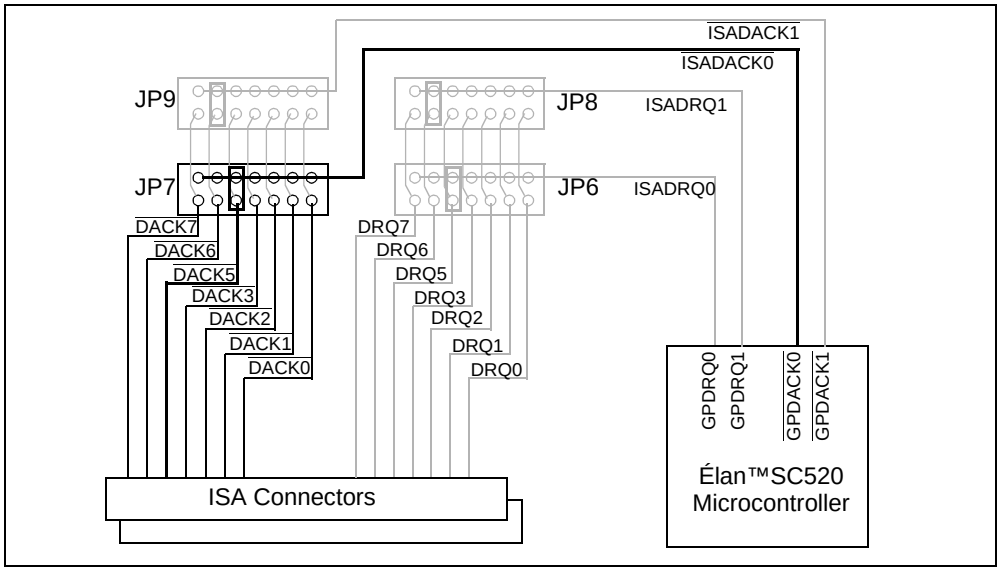


Figure A-7. Jumper JP7 Default Routing

Jumper JP8

Jumper JP8 is used to route one ISA-compatible DRQn channel from the PC/104-Plus connector to the microcontroller's GPDRQ1 input. The following settings indicate the possible configurations for jumper JP8.

- To route ISA DRQ0 to microcontroller GPDRQ1, jumper pins 1 and 2.
- To route ISA DRQ1 to microcontroller GPDRQ1, jumper pins 3 and 4.
- To route ISA DRQ2 to microcontroller GPDRQ1, jumper pins 5 and 6.
- To route ISA DRQ3 to microcontroller GPDRQ1, jumper pins 7 and 8.
- To route ISA DRQ5 to microcontroller GPDRQ1, jumper pins 9 and 10.
- To route ISA DRQ6 to microcontroller GPDRQ1, jumper pins 11 and 12.
- To route ISA DRQ7 to microcontroller GPDRQ1, jumper pins 13 and 14.

Jumper JP9 must be used to route the corresponding $\overline{\text{DACKx}}$ signal (i.e., the selected channel number must match, for example DRQ0 and $\overline{\text{DACK0}}$). Also, the channel number selected must be different from the channel selected by JP6 and JP7 (if any). Figure A-8 shows the default signal routing for jumper JP8, with ISA DRQ6 routed to GPDRQ1.

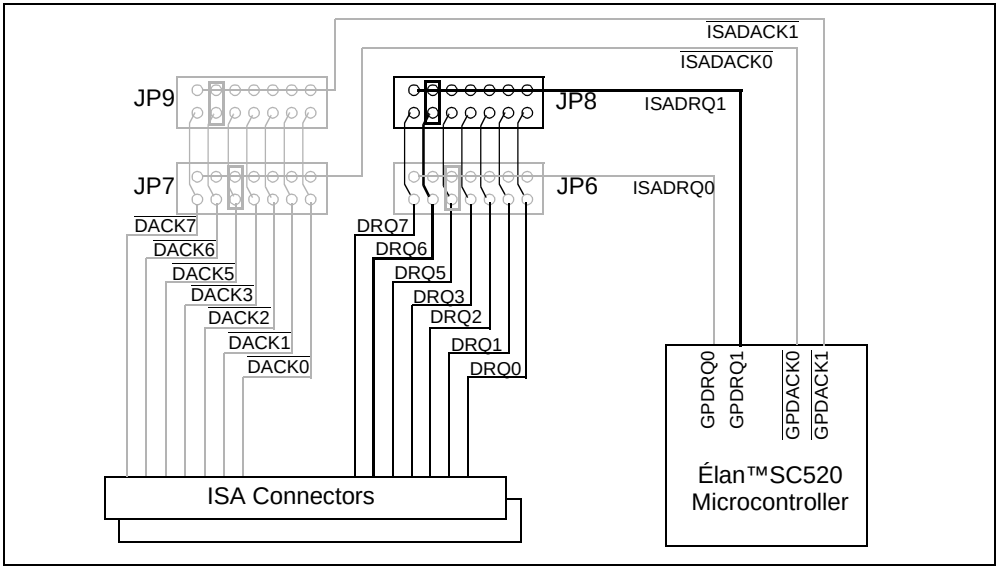


Figure A-8. Jumper JP8 Default Routing

Jumper JP9

Jumper JP9 is used to route one ISA-compatible $\overline{\text{DACKn}}$ channel from the PC/104-Plus connector to the microcontroller's $\overline{\text{GPDACK1}}$ input. The following settings indicate the possible configurations for jumper JP9.

- To route ISA $\overline{\text{DACK0}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 1 and 2.
- To route ISA $\overline{\text{DACK1}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 3 and 4.
- To route ISA $\overline{\text{DACK2}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 5 and 6.
- To route ISA $\overline{\text{DACK3}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 7 and 8.
- To route ISA $\overline{\text{DACK5}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 9 and 10.
- To route ISA $\overline{\text{DACK6}}$ to microcontroller $\overline{\text{GPDACK1}}$, jumper pins 11 and 12.
- To route ISA $\overline{\text{DACK7}}$ to microcontroller $\overline{\text{GPDACK0}}$, jumper pins 13 and 14.

Jumper JP8 must be used to route the corresponding DRQx signal (i.e., the selected channel number must match, for example DRQ0 and $\overline{\text{DACK0}}$). Also, the channel number selected must be different from the channel selected by JP6 and JP7 (if any). Figure A-9 shows the default signal routing for jumper JP9, with ISA $\overline{\text{DACK6}}$ routed to $\overline{\text{GPDACK1}}$.

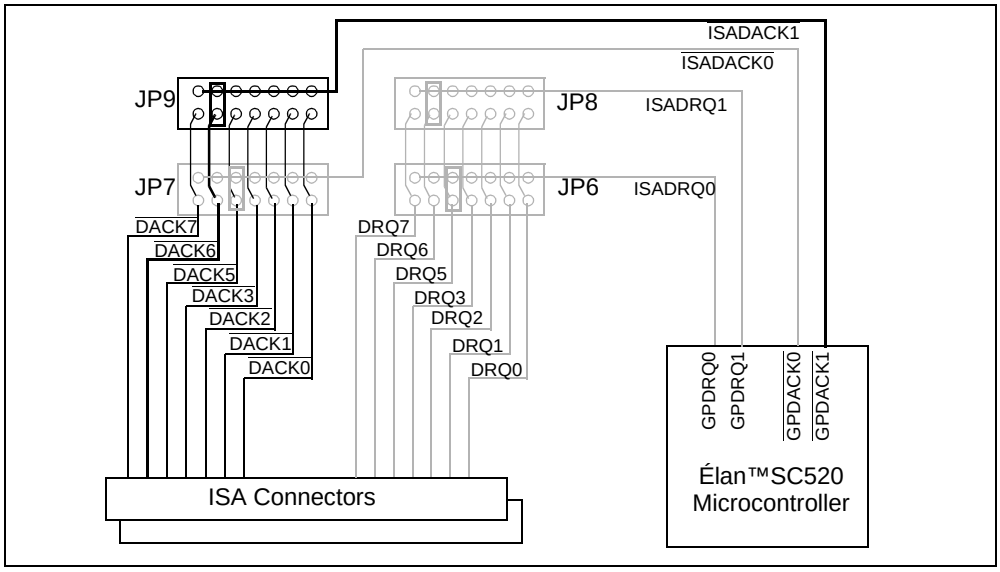


Figure A-9. Jumper JP9 Default Routing

Jumpers JP10, JP11, JP12, JP13, and JP14

Jumpers JP10, JP11, JP12, JP13, and JP14 are used for $\overline{\text{REQn}}$/$\overline{\text{GNTn}}$ tests and are used for AMD internal use only.

Jumper JP18

Select the boot device either from DIP memory or from PROM ICE when JP3 is set on pin 7 and 8. The following settings indicate the possible configurations for jumper JP18. Figure A-10 shows the jumper pins and the default setting for jumper JP18.

- To boot from DIP memory, jumper pins 1 and 2 (shown in Figure A-10).
- To boot from PROM ICE, jumper pins 2 and 3.

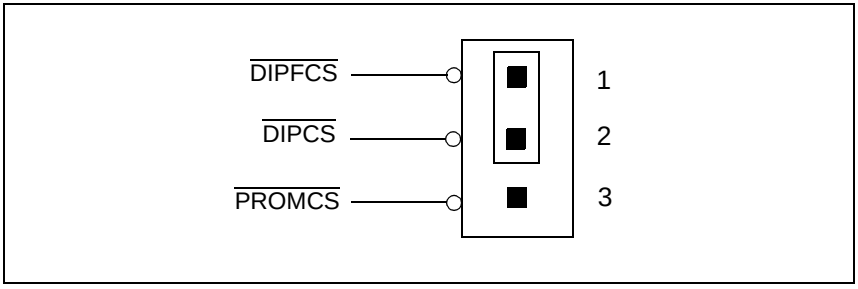


Figure A-10. Jumper JP18 Default Setting

Jumper JP20

Use either of the following jumper settings on jumper JP20 according to your PromICE setup.

- When using Flash memory or a modified PromICE cable, jumper pins 1 and 3 and jumper pins 2 and 4.
- When using PromICE with the original cable (requiring no cable modifications), jumper pins 3 and 5 and jumper pins 4 and 6.

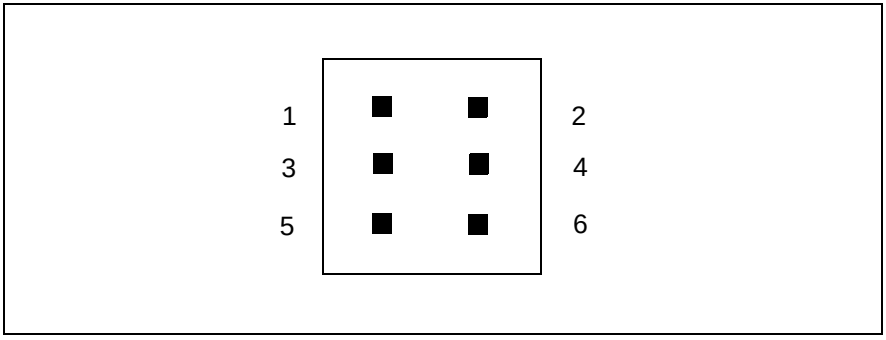


Figure A-11. Jumper JP20

DIP Switch Settings

This section provides the switch settings for the three DIP switches.

DIP Switch S3

DIP switch S3 is a single, three-circuit, slide-actuated, single-pole single-throw (SPST) DIP switch for the system boot pinstrap. The default switch setting is shown in Figure A-12. A description of the DIP switch settings and functions are shown in Table A-1. For the layout location, refer to Figure 2-2 on page 2-4.

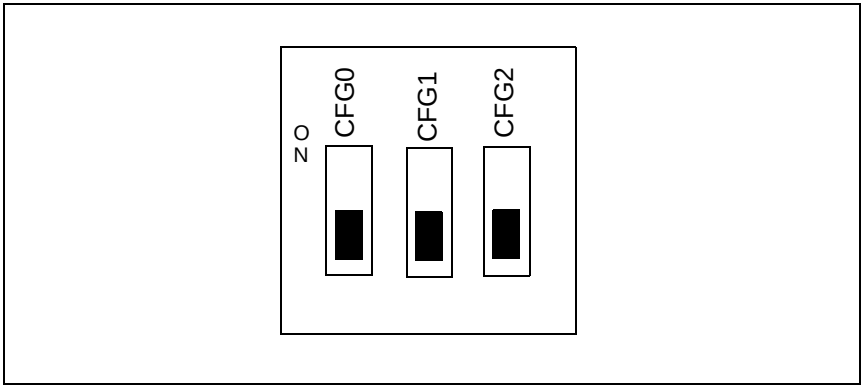


Figure A-12. DIP Switch S3 Default Setting

Table A-1. DIP Switch S3 Settings

CFG0	CFG1	CFG2	Function
OFF	OFF	X	$\overline{\text{BOOTCS}}$ data width = 8 bit
ON	OFF	X	$\overline{\text{BOOTCS}}$ data width = 16 bit
OFF	ON	X	$\overline{\text{BOOTCS}}$ data width = 32 bit
X	X	OFF	$\overline{\text{BOOTCS}}$ data bus = GP data bus
X	X	ON	$\overline{\text{BOOTCS}}$ data bus = SDRAM data bus

DIP Switch S4

DIP switch S4 is a slide-actuated DIP switch for the system boot pinstrap. The default switch setting is shown in Figure A-13. The DIP switch settings (positions 2 - 8) vary according to the user-defined applications. You must define the switch settings according to the applications being used.

For the layout location on the ÉlanSC520 microcontroller CDP, refer to Figure 2-2 on page 2-4. Table A-2 shows the switch settings on switch S4.

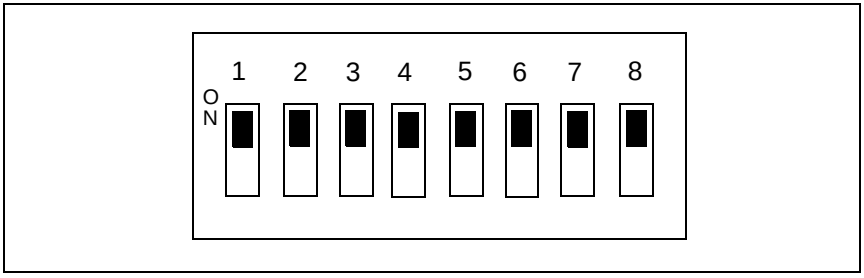


Figure A-13. DIP Switch S4 Default Setting

Table A-2. DIP Switch S4 Settings

Switch	Setting	Description
1	On Off	Normal Safe; resets CMOS settings on BIOS
2	X	Don't care
3	X	Don't care
4	On Off	BIOS splash displayed at startup Memory/PCI info displayed at startup
5	X	Don't care
6	X	Don't care
7	X	Don't care
8	X	Don't care

DIP Switch S5

DIP switch S5 is a single three-circuit, slide-actuated DIP switch for the system boot pinstrap. The default switch setting is shown in Figure A-14. A description of the DIP switch settings and functions are shown in Table A-3. For the layout location, refer to Figure 2-2 on page 2-4.

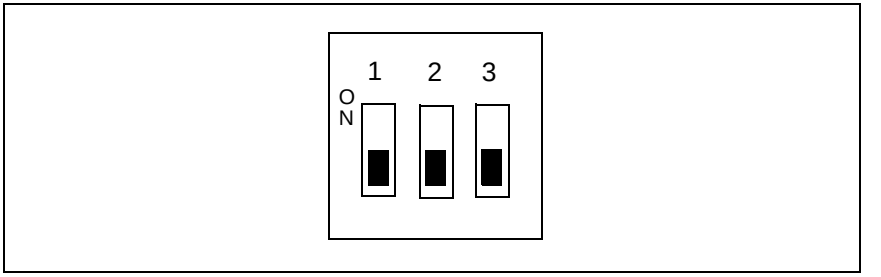


Figure A-14. DIP Switch S5 Default Setting

Table A-3. DIP Switch S5 Settings

Switch 1 - DEBUG_ENTER	
Setting	**Function**
OFF	Normal operation
ON	AMDebug tool enabled
Switch 2 - INST_TRCE	
Setting	**Function**
OFF	Normal operation
ON	Trace controller enabled to output trace records
Switch 3 - DEBUG_DIS	
Setting	**Function**
OFF	Normal operation
ON	AMDebug tool is disabled and cannot be enabled by software

Appendix B

Resource Assignments

This section provides information about the resource assignments for the chip selects, GPIRQ, GPDMA, PIO, and UART.

The following information applies to the following five resource assignment tables in this appendix:

- All PIOs are configured for alternate pin functions except PIO27, which is default to input and works as ISA IOCHCHK.
- CBAR aliases MMCR at DF00:0.
- Echo Mode is default to Off.
- $\overline{\text{GPCS3}}$-$\overline{\text{GPCS7}}$ are chip selects, the default setting of PITGATE2, TMRIN1, TMRIN0, TMROUT1, and TMROUT0.
- CLKTEST pin is default to output 1.8432 MHz.
- $\overline{\text{BOOTCS}}$, $\overline{\text{ROMCS1}}$, and $\overline{\text{ROMCS2}}$ are default to non-page mode (seven wait states).

Chip Select Resource Assignments

Table B-1 provides the resource assignments for the devices listed.

Table B-1. Chip Select Resource Assignments

Chip Select	Settings
$\overline{\text{BOOTCS}}$	**For JP3 and JP18, select either:**
	First 2M X 32 SDRAM bus bank
	Second 2M X 32 SDRAM bus bank
	Flash memory expansion connector
	512K X 8 DIP EPROM/Flash memory
	Flash memory expansion connector
$\overline{\text{ROMCS1}}$	**For JP4, select either:**
	First 2M X 32 SDRAM bus bank
	Second 2M X 32 SDRAM bus bank
	Flash memory expansion connector
$\overline{\text{ROMCS2}}$	**For JP5, select either:**
	First 2M X 32 SDRAM bus bank
	Second 2M X 32 SDRAM bus bank
	Flash memory expansion connector
$\overline{\text{GPCS3}}$	64K X 16 SRAM on GPBUS (word access)
$\overline{\text{GPCS4}}$	Unused - for use as TMRIN1 set to input
$\overline{\text{GPCS5}}$	Unused - for use as TMRIN0 set to input
$\overline{\text{GPCS6}}$	IDE hard drive CS0
$\overline{\text{GPCS7}}$	IDE hard drive CS1

GPIRQ Resource Assignments

Table B-2 provides the resource assignments for the devices listed.

Table B-2. GPIRQ Resource Assignments

	ISA SLT1	ISA SLT2	Super I/O	TIP	IDE Hard Drive
GPIRQ0	IRQ11	IRQ11	IRQ11	—	—
GPIRQ1	—	—	IRQ1 (Keyboard)	—	—
GPIRQ2	IRQ12	IRQ12	IRQ12 (Mouse)	—	—
GPIRQ3	IRQ3	IRQ3	IRQ3 (COM4[1])	—	—
GPIRQ4	IRQ4	IRQ4	IRQ4 (COM3[1])	—	—
GPIRQ5	IRQ5	IRQ5	IRQ5 (Lpt2) (Not in use)	—	—
GPIRQ6	IRQ6	IRQ6	IRQ6 (FDC)	—	—
GPIRQ7	IRQ7	IRQ7	IRQ7 (Lpt1)	SERIRQ0 R109	—
GPIRQ8	—	—	IRQ8 (RTC) (Not in use)	SERIRQ1 R107	—
GPIRQ9	IRQ9	IRQ9	IRQ9	PARIRQ R106	—
GPIRQ10	IRQ10	IRQ10	IRQ10	ENETIRQ R105	IRQ14

NOTE:

1. The BIOS included with CDP version 1.4 maps the Super I/O UARTs to COM3 and COM4. Earlier BIOS versions, used on boards with microcontroller revisions A0 and A1, disabled the microcontroller's UARTs and mapped the Super I/O UARTs to COM1 and COM2 instead.

GPDMA Resource Assignments

Table B-3 provides the resource assignments for the devices listed.

Table B-3. GPDMA Resource Assignments

	ISA SLT1	ISA SLT2	Super I/O	IDE Hard Drive
$\overline{\text{GPDRQ0}}$ $\overline{\text{GPDACK0}}$	DRQ/DACK, 0, 1, 2, 3, 5, 6, 7, JP6, JP7	DRQ/DACK, 0, 1, 2, 3, 5, 6, 7, JP6, JP7	—	—
$\overline{\text{GPDRQ1}}$ $\overline{\text{GPDACK1}}$	DRQ/DACK, 0, 1, 2, 3, 5, 6, 7, JP8, JP9	DRQ/DACK, 0, 1, 2, 3, 5, 6, 7, JP8, JP9	—	—
$\overline{\text{GPDRQ2}}$ $\overline{\text{GPDACK2}}$	—	—	DRQ0/ DACK0	—
$\overline{\text{GPDRQ3}}$ $\overline{\text{GPDACK3}}$	—	—	—	DMAREQ/ DMA_ACK R17, R18

PIO Resource Assignments

Table B-4 provides the resource assignments for the devices listed.

Table B-4. PIO Resource Assignments

PIN	CDP	PROBE[1]	CDP Use	PIO Input	PIO Output
PIO0	GPALE	P8 D14	Drives ISA ALE via buffer U20	NA	NA
PIO1	$\overline{\text{GPBHE}}$	P8 D12	Drives ISA $\overline{\text{BHE}}$ via buffer U20	NA	NA
PIO2	GPRDY	P8 D15	Driven by ISA IOCHRDY, IDE hard drive IOCHRDY, Super I/O IOCHRDY, and TIP IOCHRDY. Wired OR with 1K pullup to 5V.	NA	NA
PIO3	GPAEN	P8 P11	Drives ISA, Super I/O, AND tip and via buffer U20. GPAEN used by PALs U4 and U6 for GP bus decode.	NA	NA
PIO4	GPTC	P3 D10	Drives ISA and Super I/O TC via Buffer U20	NA	NA
PIO5	GPDRQ3	P4-16	IDE hard drive DMAREQ via R17	NA	NA
PIO6	GPDRQ2	P4-11	Super I/O DRQ0 for SIO	NA	NA
PIO7	GPDRQ1	P4-14	ISA DRQ0, 1, 2, 3, 5, 6, 7; selected by JP8	NA	NA
PIO8	GPDRQ0	P4-11	ISA DRQ0, 1, 2, 3, 5, 6, 7; selected by JP6	NA	NA
PIO9	$\overline{\text{GPDACK3}}$	P4-20	IDE hard drive $\overline{\text{DMA\_ACK}}$ via R18	NA	NA
PIO10	$\overline{\text{GPDACK2}}$	P4-17	Super I/O $\overline{\text{DACK0}}$ for SIO	NA	NA
PIO11	$\overline{\text{GPDACK1}}$	P4-18	ISA $\overline{\text{DACK0}}$, 1, 2, 3, 5, 6, 7; selected by JP9	NA	NA
PIO12	$\overline{\text{GPDACK0}}$	P4-15	ISA $\overline{\text{DACK0}}$, 1, 2, 3, 5, 6, 7; selected by JP7	NA	NA
PIO13	GPIRQ10	P4-12	Driven by ISA IRQ10, Super I/O IRQ10, IDE hard drive IRQ, and TIP ENETIRQ via R015; has pullup 4K7 to 5V.	NA	NA
PIO14	GPIRQ9	P4-9	Driven by ISA IRQ9, Super I/O IRQ9, and TIP PARIRQ via R106; has pullup 4K7 to 5V.	NA	NA
PIO15	GPIRQ8	P4-10	Driven by Super I/O IRQ8 and TIP SERIRQ1 via R107; has pullup 4K7 to 5V.	NA	NA

Table B-4. PIO Resource Assignments (Continued)

PIN	CDP	PROBE[1]	CDP Use	PIO Input	PIO Output
PIO16	GPIRQ7	P4-7	Driven by ISA IRQ7, Super I/O IRQ7 and TIP SERIRQ0 via R109; has pullup 4K7 to 5V.	NA	NA
PIO17	GPIRQ6	P4-8	Driven by ISA IRQ6, Super I/O IRQ6 and TIP MAINIRQ via R108; has pullup 4K7 to 5V.	NA	NA
PIO18	GPIRQ5	P4-5	Driven by ISA IRQ5 and Super I/O IRQ5; has pullup 4K7 to 5V.	NA	NA
PIO19	GPIRQ4	P4-6	Driven by ISA IRQ4 and Super I/O IRQ4; has pullup 4K7 to 5V.	NA	NA
PIO20	GPIRQ3	P4-3	Driven by ISA IRQ3 and Super I/O IRQ3; has pullup 4K7 to 5V.	NA	NA
PIO21	GPIRQ2	P4-4	Driven by ISA IRQ12 and Super I/O IRQ12; has pullup 4K7 to 5V.	NA	NA
PIO22	GPIRQ1	P4-1	Driven by Super I/O IRQ1; has pullup 4K7 to 5V.	NA	NA
PIO23	GPIRQ0	P4-2	Driven by ISA IRQ11 and Super I/O IRQ11; has pullup 4K7 to 5V.	NA	NA
PIO24	$\overline{\text{GPDBUFOE}}$	P8 D9	Enables GP data bus buffer and 512 Kbyte SRAM RD strobe	NA	NA
PIO25	$\overline{\text{GPIOCS16}}$	P11 D15	Driven by ISA $\overline{\text{IOCS16}}$ and IDE hard drive $\overline{\text{IO16}}$; used by PAL U4 for GP bus decode; has pullup 1K to 5V.	NA	NA
PIO26	$\overline{\text{GPMEMCS16}}$	P11 D14	Driven by ISA $\overline{\text{MEMCS16}}$; has pullup 1K to 5V.	NA	NA
PIO27	PIO27 Input	P4-22	Driven by ISA $\overline{\text{IOCHCK}}$; has pullup 4K7 to 5V.	Input	NA
PIO28	$\overline{\text{CTS2}}$	P4-40	Driven by COM2 transceiver U34 (CTS)	NA	NA
PIO29	$\overline{\text{DSR2}}$	P4-46	Driven by COM2 transceiver U34 (DSR)	NA	NA
PIO30	$\overline{\text{DCD2}}$	P4-38	Driven by COM2 transceiver U34 (DCD)	NA	NA
PIO31	$\overline{\text{RIN2}}$	P4-48	Driven by COM2 transceiver U34 (RI)	NA	NA

Note:
1. The Probe column indicates the probe point on the CDP as the pin name (Px Dxx) or the number (Px-xx).

UART Resource Assignments

Table B-5 provides the resource assignments for the devices listed.

Table B-5. UART Resource Assignments

Device	Setting
UART1	COM1 DTE on DB25M R70 and R173, or R71 and R172 selects RS422 or RS232 1.15 Mbit/s maximum speed
UART2	COM2 DTE RS232 on DB9M 120 Kbit/s maximum speed
SSI	Three devices selected by Super I/O signals: CIO14: expansion connector JP17 CIO15: MICROWIRE EEPROM CIO16: SPI EEPROM

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