National Semiconductor

2470A Servo Demodulator

General Description

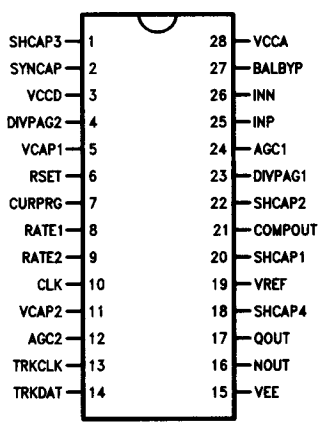
The new 2470A servo demodulator decodes the quadrature di-bit pattern from the dedicated servo surface providing position and data information.

Features

- Quadrature positions signals
- Phase locked to servo pattern with embedded lock indication
- Track data and track clock for data encoding
- AGC amplifier with 36 dB range
- Servo fields to 400 kHz
- Compatible with the 24H80 servo preamp and 2460 servo control chip
- Standard 5V and 12V supplies
- New phase detector eliminates jitter due to dropped sync's
- New lock detector uses sync pulse location to determine sync. Dropped pulses are not out of sync conditions.
- New ±20% VCO with extended frequency capability (>30 MHz)
- New totem pole TTL outputs
- New sync detector eliminates one shot multivibrator setting
- New sample and hold circuits eliminate output droop and glitching of the quadrature circuits
- New reference centers the quadrature outputs in the 12V supply
- New sync window controller prevents erroneous pulses from reaching the phase detector for a second level of jitter prevention

Connection Diagrams

28-Pin Molded DIP



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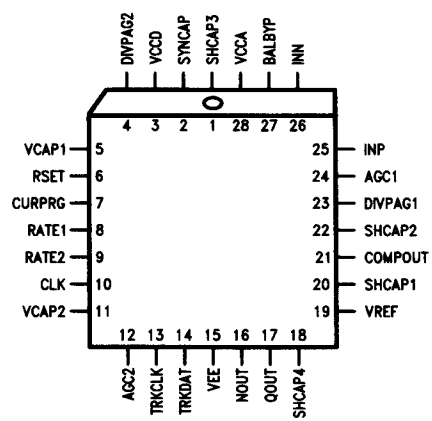
Top View
† **Order Number 2470PC**
‡ **See NS Package Number N28B**

28 PLCC



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Top View
† **Order Number 2470QC**
‡ **See NS Package Number V28A**

† For most current order information, contact your local sales office.
‡ For most current package information, contact product marketing.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +175°C
Operating Temperature	0°C to +70°C
Lead Temperature (Ceramic DIP (10 sec.))	300°C
Internal Power Dissipation	2.5W
Supply Voltage V_{CCD}	6V
Supply Voltage V_{CCA}	15V

2470A Electrical Specification T_A = 25°C, V_{CCD} = 5V, V_{VCCA} = 12V

Parameter	Conditions	Min	Typ	Max	Units
AGC AMPLIFIER					
Max Voltage Gain	Input Freq. = 1 MHz		46		dB
AGC Range	Input Freq. = 1 MHz		40		dB
Frequency Response			10		MHz
Input Voltage Range		30		300	mV
Output Voltage			3.5		V_{PP}
QUADRATURE OUTPUTS					
Output Voltage	R_L = 20k		3.0		V_{PP}
Output Impedance			100		Ω
Output Offset Voltage			20		mV
Common Mode Voltage			6		V
VOLTAGE REFERENCE					
Output Voltage			6		V
Output Current			5		mA
SYNC DETECTOR					
SYNCAP = 15.2E−6/(Frame Rate) in Farads					
Frame Rate Span		−50%	...	+100%	
Phase Detector & Charge Pump					
Gain P_D & CHGPMP, K_{PD}			ICH/6.28		Amps/Rad
CURPRG Pin Voltage to ICH			6.95E−4		Amps/V
V_{CO}					
Center Frequency = 0.20833/(RSET × VCAP) in Hz					
K(V_{CO}) = 0.3 × Center Frequency in Hz/V					
Tuning Range		−20%		+20%	
Max Frequency	C_{EXT} = 7 pF, rset = 350		40		MHz
Logic					
	0.8V to 3.6V				
Risetime	10%–90%		9		ns
Falltime	10%–90%		4		ns

DIVIDER TABLE

DIVPAG1	DIVPAG2	RATIO
0	0	32
1	0	64
0	1	96
1	1	128

Power Supply Ratings				
V_{CCD} (5V)			75	mA
V_{CCA} (12V)			35	mA

Features of the 2470A Servo Demodulator

1) The sync detecting operation is based on the servo disk's own timing and eliminates the need to precisely set a resistor-capacitor time constant for the di-bit detecting one shot timer. The new circuit uses a single low precision capacitor.
2) The phase detector has a linear phase vs. output detection scheme as an improvement over the one shot scheme. The circuit performs no detection for dropped sync pulses and when in lock as defined by the lock detector, it will only detect in a predefined window. These features eliminate jitter caused by dropped pulses and/or bad servo areas on the disk. Also eliminated are the phase detector external components.

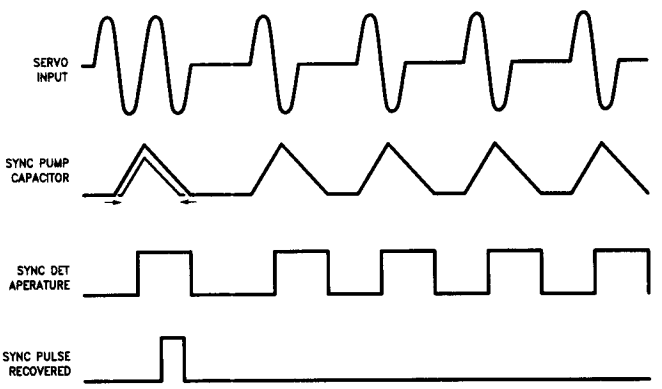
   Out of lock conditions require acquisition aids to achieve lock. Should a sync pulse show outside the sync window (2 of 32 counts in a servo field), aperature control circuits realign the sync pulse with the sync window by resetting the decoder and enlarge the next window to find a sync pulse with the VCO's ±20% tuning range. The limited range on the VCO prevents 2X locks. The aperature control prevents the dropped pulse ignoring phase detector from achieving non-integral false locks. The window realignment and enlargement is disabled during lock to prevent erroneous sync pulses from upsetting the decoder.
3) The new lock detector ignores dropped pulses in testing for in and out of lock conditions. Should a sync pulse appear the detector records whether or not it appeared in the normal sync window. The lock detector uses four consecutive sync pulses either all out or all in the sync window to determine lock status. The lock detector enables and disables the aperature control for the phase detector and the sync data detector.
4) The 2470A has a VCO with improved performance. It has > 30 MHz operation and a restricted tuning range of ±20%. Tuning circuits will reduce jitter due to parasitic couplings into the VCO.
5) New sample hold circuits for the N and Q decoders eliminate the droop in the N and Q outputs. The sample holds are opened immediately after the peak detection is complete. This eliminates droop induced offsets and glitching.
6) TTL totem pole outputs eliminates the need for resistive pullup for the output. Switching times of 10 ns are achieved.
7) The analog reference is 6V. Centering in the 12V supply lines is easier. The 6V reference maintains compatibility with the 2460 servo controller and the 24H80 preamp.

List of Lead Functions

Lead	Name	Function
INPUT SIGNALS		
23 4	DIVPAG1 DIVPAG2	Programs the prescaler for the VCO Divide ratios are 32, 64, 96 and 128
7	CURPRG	Voltage sets PLL charge pump bias current
15	V_{EE}	Ground 0V
3	V_{CCD}	+5V supply
28	V_{CCA}	+12V supply
25 26	INP INN	Composite inputs to the AGC amplifier
OUTPUTS		
13	TRKCLK	Clock output for data during lock, TTL
14	TRKDAT	Data from dropped sync pulses TTL
10	CLK	VCO output TTL
21	COMPOUT	Output of AGC amplifier @8.2V CM
19	V_{REF}	6V reference for N and Q outputs
16	N_{OUT}	Normal position signal @6V CM
17	Q_{OUT}	Quadrature position signal @6V CM

List of Lead Functions (Continued)

Lead	Name	Function
EXTERNAL COMPONENTS		
2	SYNCAP	Timing capacitor for the sync detector
5–11	V_{CAP} 1 & 2	VCO timing capacitor
8–9	Rate 1 & 2	PLL loop filter
27	BALBYP	DC offset restore filter capacitor.
24	AGC1	AGC system loop filter
12	AGC2	Bypass capacitor for AGC system
6	R_{SET}	Sets the VCO bias currents I < 2 mA
20, 22, 1, 18	SHCAP 1 . . . 4	Four sample hold capacitors



The sync pulse gate is triggered by the sync det aperature and is locked open until the sync goes to zero. The locking mechanism prevents clipping the negative edge of the sync.

FIGURE 1. Sync Detector Diagram

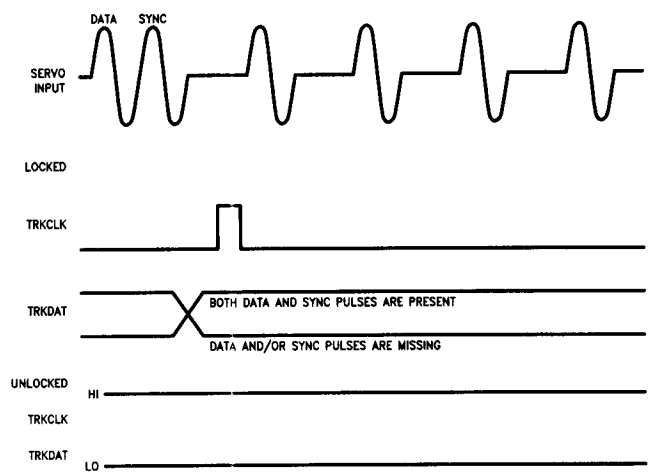


FIGURE 2. Track Data Output Information

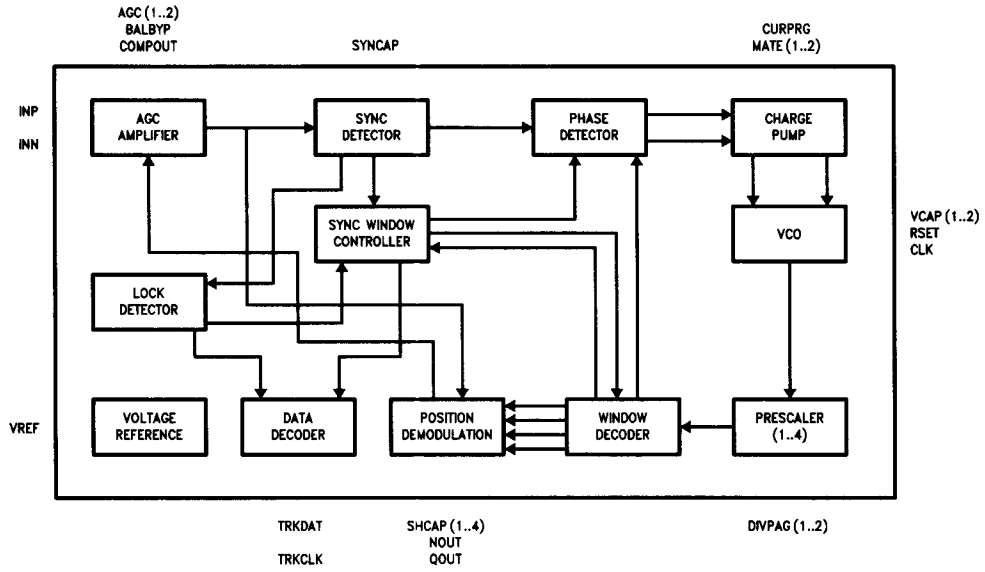


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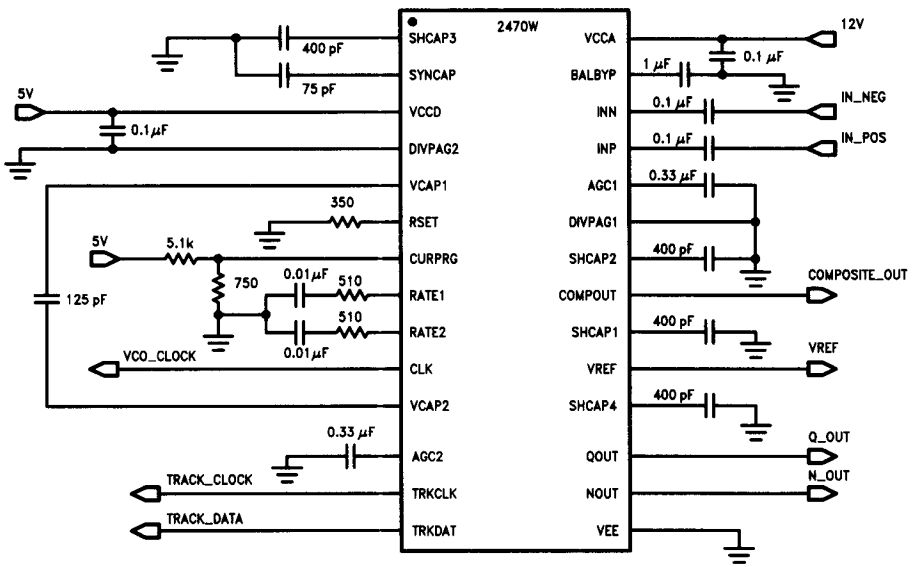
FIGURE 3. 2470A Block Diagram

This test circuit runs at about a 136 kHz frame rate



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DIVPAG1 and DIVPAG2 are TTL divider controls.
e.g. 10, 01, 11 are divided by 1,2,3,4 respectively.
SYNCAP (Min) = 7.6 µ/F (Field Rate)
SYNCAP = (1.5 . . . 2) = SYNCAP (Min)

TRKCLK and TRKDAT are high and low respectively when unlocked.
$I(R_{SET}) < 2$ mA ‖
ICH = 695 µA/V = V(CURPRG)
Sample hold caps (4) are a balance of smoothing vs speed.

$K(P_D + CHGPMP) = ICH/(2 = PI)$
F(CENTER) = 5/(24 × RC)
F′ ≈ (9/10) × F(CENTER)

FIGURE 4. 2470A Test Circuit