MICROCHIP

24LC41A

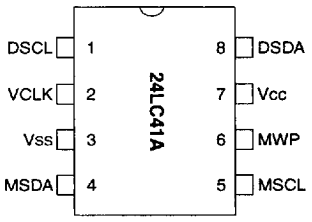
1K/4K 2.5V Dual Mode, Dual Port I^2C^{TM} Serial EEPROM

FEATURES

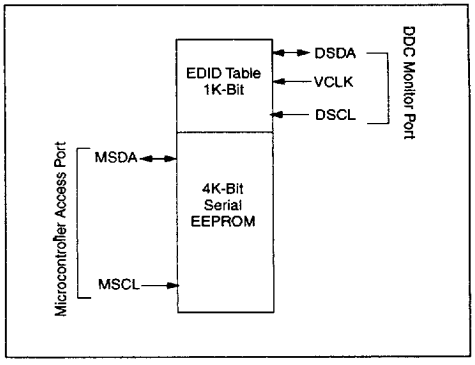
- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification, including recovery to DDC1
- Improved noise immunity
- Separate high speed 2-wire bus for microcontroller access to 4K-bit Serial EEPROM
- Low power CMOS technology
- 2 mA active current typical
- 20 µA standby current typical at 5.5V
- Dual 2-wire serial interface bus, I^2C™ compatible
- Hardware write-protect for Microcontroller Access Port
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes (DDC port) or 16 bytes (4K Port)
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- 1,000,000 erase/write cycles guaranteed
- Data retention > 40 years
- 8-pin PDIP package
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

PACKAGE TYPE

PDIP



BLOCK DIAGRAM



DESCRIPTION

The Microchip Technology Inc. 24LC41A is a dual-port 128 x 8 and 512 x 8-bit Electrically Erasable PROM (EEPROM). This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Three modes of operation have been implemented:

- Transmit-Only Mode for the DDC Monitor Port
- Bi-directional Mode for the DDC Monitor Port
- Bi-directional, industry-standard 2-wire bus for the 4K Microcontroller Access Port

Upon power-up, the DDC Monitor Port will be in the Transmit-Only Mode, repeatedly sending a serial bit stream of the entire memory array contents, clocked by the VCLK pin. A valid high to low transition on the DSCL pin will cause the device to enter the transition mode, an look for a valid control byte on the I^2C bus. If it detects a valid control byte from the master, it will switch to Bi-directional Mode, with byte selectable read/write capability of the memory array using DSCL. If no control byte is received, the device will revert to the Transmit-Only Mode after it received 128 consecutive VCLK pulses while the DSCL pin is idle. The 4K-bit microcontroller port is completely independent of the DDC port, therefore, it can be accessed continuously by a microcontroller without interrupting DDC transmission activity. The 24LC41A is available in a standard 8-pin PDIP package in both commercial and industrial temperature ranges.

DDC is a trademark of Video Electronics Standards Association.
I^2C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC} 7.0V
All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ... +300°C
ESD protection on all pins ..... ≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
DSCL	Serial Clock for DDC Bi-directional Mode (DDC2)
DSDA	Serial Address and Data I/O (DDC Bus)
VCLK	Serial Clock for DDC transmit-only mode (DDC1)
MSCL	Serial clock for 4K-bit MCU port
MSDA	Serial Address and Data I/O for 4K-bit MCU port
MWP	Hardware write-protect for Microcontroller Access Port
V_{SS}	Ground
V_{CC}	+2.5V to +5.5V power supply

TABLE 1-2: DC CHARACTERISTICS

	V_{CC} = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
DSCL, DSDA, MSCL & MSDA pins: High level input voltage Low level input voltage	 V_{IH} V_{IL}	 .7 V_{CC} —	 — .3 V_{CC}	 V V	
Input levels on VCLK pin: High level input voltage Low level input voltage	 V_{IH} V_{IL}	 2.0 —	 .8 .2 V_{CC}	 V V	 $V_{CC} \geq 2.7V$ (Note) $V_{CC} < 2.7V$ (Note)
Hysteresis of Schmitt trigger inputs	V_{HYS}	.05 V_{CC}	—	V	Note 1
Low level output voltage	V_{OL1}	—	.4	V	I_{OL} = 3 mA, V_{CC} = 2.5V (Note)
Low level output voltage	V_{OL2}	—	.6	V	I_{OL} = 6 mA, V_{CC} = 2.5V
Input leakage current	I_{LI}	-10	10	µA	V_{IN} = .1V to V_{CC}
Output leakage current	I_{LO}	-10	10	µA	V_{OUT} = .1V to V_{CC}
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	10	pF	V_{CC} = 5.0V (Note), Tamb = 25°C, F_{CLK} = 1 MHz
Operating current	I_{CC} Write I_{CC} Read	— —	3 1	mA mA	V_{CC} = 5.5V, DSCL or MSCL = 400 kHz
Standby current	I_{CCS}	— —	60 200	µA µA	V_{CC} = 3.0V, DSDA or MSDA = DSCL or MSCL = V_{CC} V_{CC} = 5.5V, DSDA or MSDA = DSCL or MSCL = V_{CC}

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS (DDC MONITOR AND MICROCONTROLLER ACCESS PORTS)

DDC Monitor Port (Bi-directional Mode) and Microcontroller Access Port							
Parameter	**Symbol**	**Standard Mode**		**Vcc = 4.5 - 5.5V Fast Mode**		**Units**	**Remarks**
		Min	**Max**	**Min**	**Max**		
Clock frequency (DSCL and MSCL)	FCLK	—	100	—	400	kHz	
Clock high time (DSCL and MSCL)	THIGH	4000	—	600	—	ns	
Clock low time (DSCL and MSCL)	TLOW	4700	—	1300	—	ns	
DSCL, DSDA, MSCL & MSDA rise time	TR	—	1000	—	300	ns	(Note 1)
DSCL, DSDA, MSCL & MSDA fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + .1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (DSCL, DSDA, MSCL & MSDA pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	10M	—	10M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)
DDC Monitor Port Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	4000	—	600	—	ns	
Mode transition time	TVHZ	—	500	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of DSCL or MSCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

2.0 FUNCTIONAL DESCRIPTION

2.1 DDC Monitor Port

The DDC Monitor Port operates in two modes, the Transmit-Only Mode and the Bi-directional Mode. There is a separate 2-wire protocol to support each mode, each having a separate clock input and sharing a common data line (DSDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the DSDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the DSCL input. When a valid transition on DSCL is recognized, the device will switch into the Bi-directional Mode and look for its control byte to be sent by the master. If it detects its control byte, it will stay in the Bi-directional Mode. Otherwise, it will revert to the Transmit-Only Mode after it sees 128 VCLK pulses.

2.1.1 TRANSMIT-ONLY MODE

The device will power up in the Transmit-Only Mode at address 00H. This mode supports a unidirectional 2-wire protocol for transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (see Section 2.1.2). In this mode, data is transmitted on the DSDA pin in 8-bit bytes, each followed by a ninth, null bit (see Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted by most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The Bi-directional Mode Clock (DSCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.1.2 INITIALIZATION PROCEDURE

After Vcc has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the DSDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power up at an indeterminate byte address (see Figure 2-2).

FIGURE 2-1: TRANSMIT-ONLY MODE

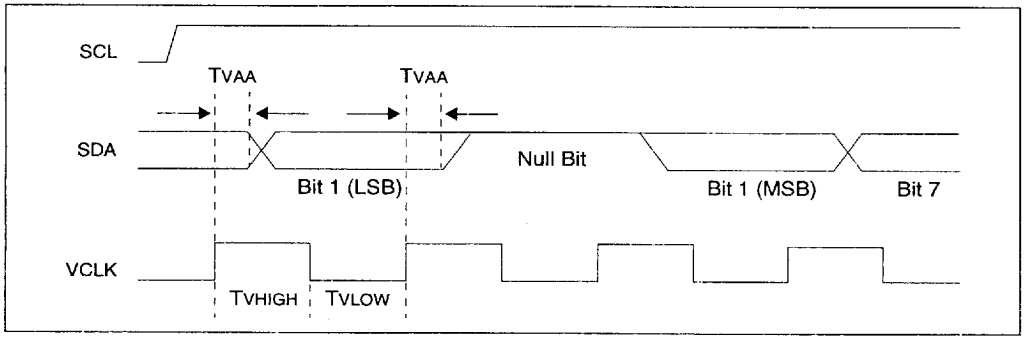
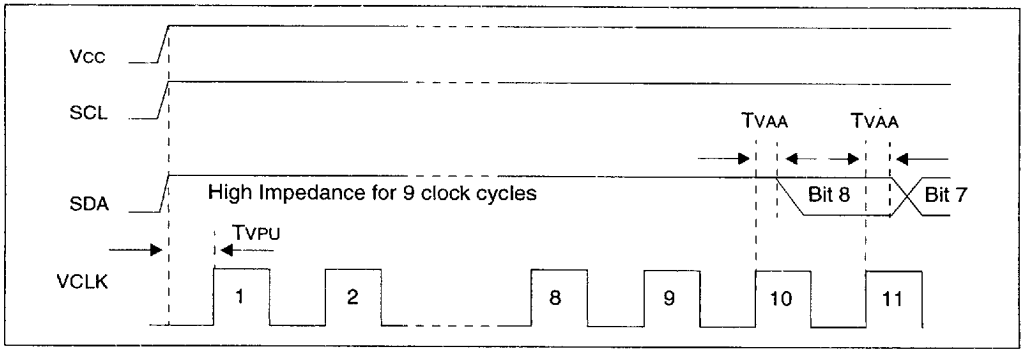


FIGURE 2-2: DEVICE INITIALIZATION



2.1.3 BI-DIRECTIONAL MODE

Before the 24LC41A can be switched into the Bi-directional Mode (Figure 2-4), it must enter the transition mode, which is done by applying a valid high to low transition on the Bi-directional Mode Clock (DSCL). As soon it enters the transition mode, it looks for a control byte 1010 000X on the I^2C™ bus, and starts to count pulses on VCLK. Any high to low transition on the DSCL line will reset the count. If it sees a pulse count of 128 on VCLK while the DSCL line is idle, it will revert back to the Transmit-Only Mode, and transmit its contents starting with the most significant bit in address 00h. However, if it detects the control byte on the I^2C bus, (Figure 2-3) it will switch to the in the Bi-directional Mode. Once the device has made the transition to the Bi-directional mode, the only way to switch the device back to the Transmit-Only Mode is to remove power from the device. The mode transition process is shown in detail in Figure 2-4.

Once the device has switched into the Bi-directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two-wire Bi-directional data transmission protocol (I^2C). In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bi-directional Mode Clock (DSCL), controls access to the bus and generates the START and STOP conditions, while the monitor port acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. In the Bi-directional mode, the monitor port only responds to commands for device 1010 000X.

2.2 Microcontroller Access Port

The Microcontroller Access Port supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (MSCL), controls the bus access, and generates the START and STOP conditions, while the Microcontroller Access Port works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

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FIGURE 2-3: SUCCESSFUL MODE TRANSITION TO BI-DIRECTIONAL MODE

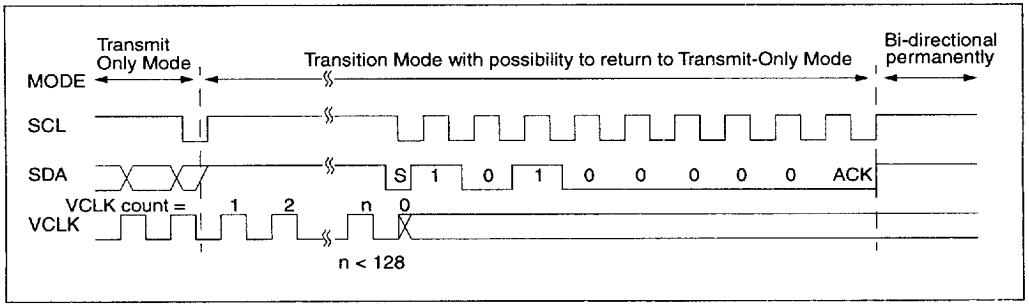


FIGURE 2-4: MODE TRANSITION WITH RECOVERY TO TRANSMIT-ONLY MODE

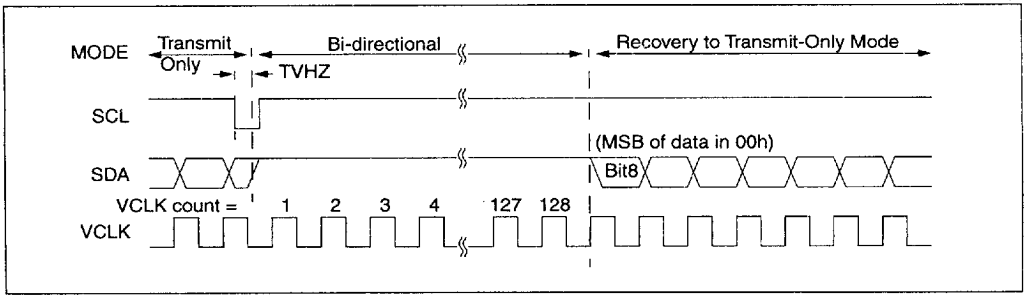
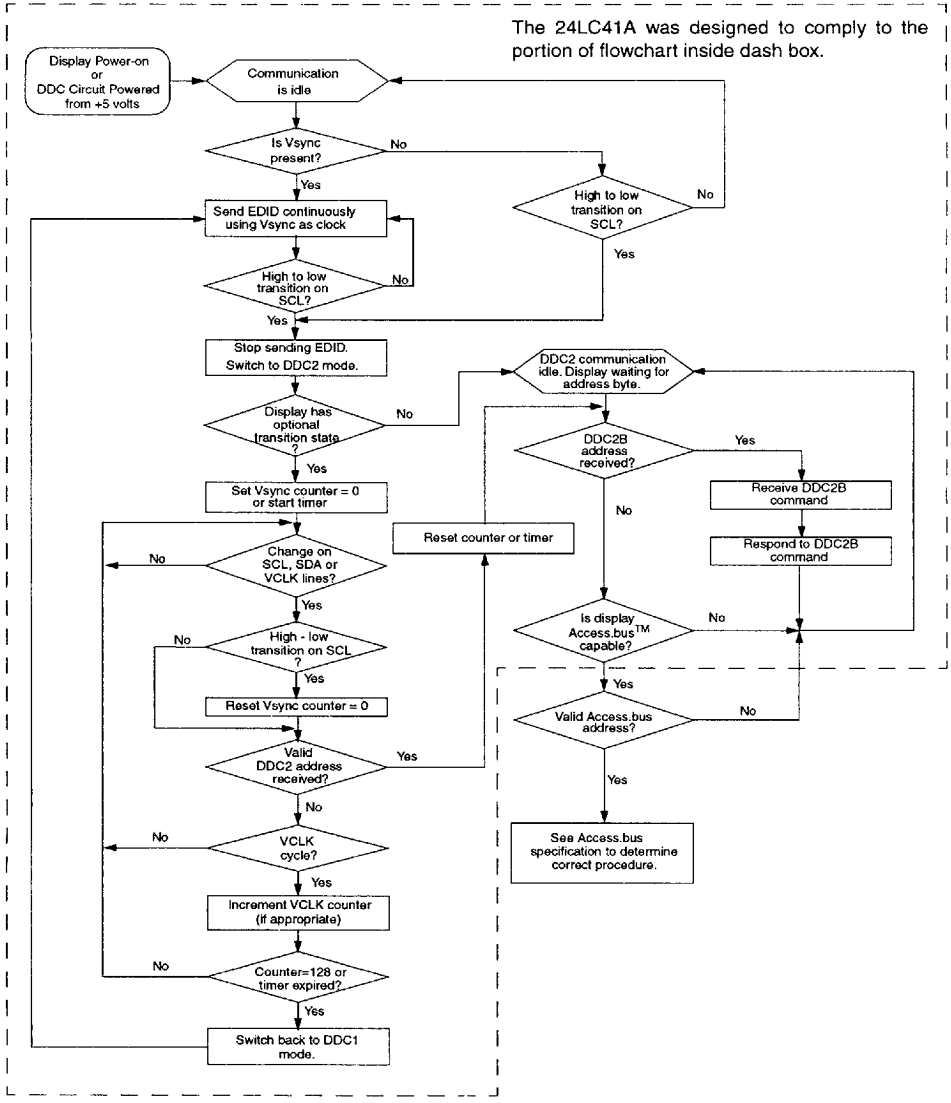


FIGURE 2-5: DISPLAY OPERATION PER DDC STANDARD PROPOSED BY VESA



Note 1: The base flowchart is copyright © 1993, 1994, 1995 Video Electronic Standard Association (VESA) from VESA's Display Data Channel (DDC) Standard Proposal ver. 2p rev. 0, used by permission of VESA.

2: The dash box and text "The 24LC41A and ... inside dash box." are added by Microchip Technology, Inc.

3: Vsync signal is normally used to derive a signal for VCLK pin on the 24LC41A.

3.0 BI-DIRECTIONAL BUS CHARACTERISTICS

Characteristics for the Bi-directional bus are identical for both the DDC Monitor Port (in Bi-directional Mode) and the Microcontroller Access Port The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the DSDA or MSDA line while the clock (DSCL or MSCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit

Note: The microcontroller access port and the DDC Monitor Port (in Bi-directional Mode) will not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the DSDA or MSDA line during the acknowledge clock pulse in such a way that the DSDA or MSDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

3.6 Device Addressing

A control byte is the first byte received following the start condition from the master device. The first part of the control byte consists of a 4-bit control code. This control code is set as 1010 for both read and write operations and is the same for both the DDC Monitor Port and Microcontroller Access Port. The next three bits of the control byte are block select bits (B1, B2, and B0). All three of these bits are zero for the DDC Monitor Port. The B2 and B1 bits are don't care bits for the Microcontroller Access Port, and the B0 bit is used by the Microcontroller Access Port to select which of the two 256 word blocks of memory are to be accessed (see Figure 3-4). The B0 bit is effectively the most significant bit of the word address. The last bit of the control byte defines the operation to be performed. When set to one, a read operation is selected; when set to zero, a write operation is selected. Following the start condition, the device monitors the DSDA or MSDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the device will select a read or a write operation. The DDC Monitor Port and Microcontroller Access Port can be accessed simultaneously because they are completely independent of one another.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	B1B2B0	1
Write	1010	B1B2B0	0

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

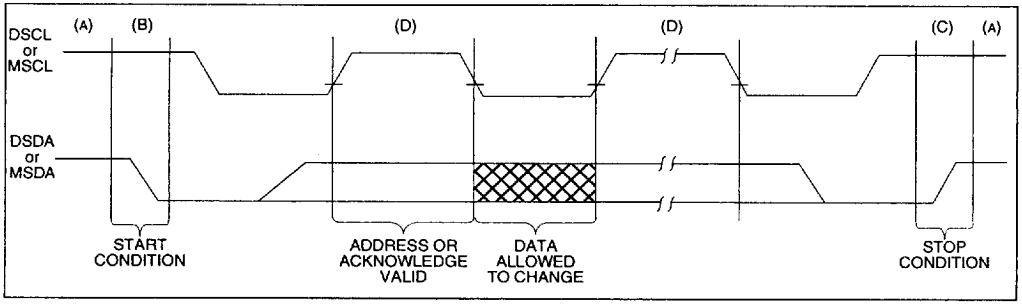


FIGURE 3-2: BUS TIMING START/STOP

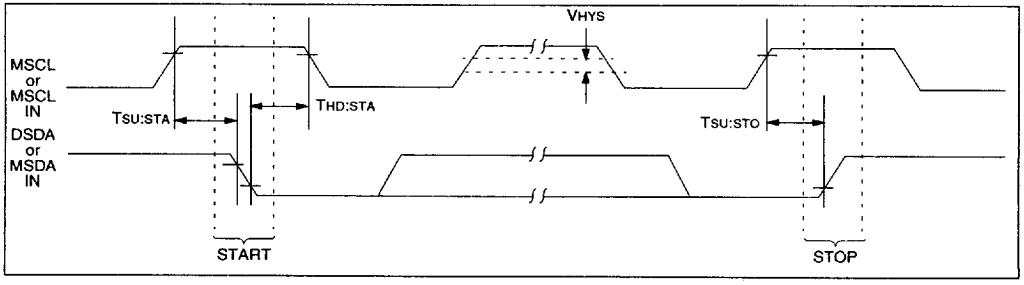


FIGURE 3-3: BUS TIMING DATA

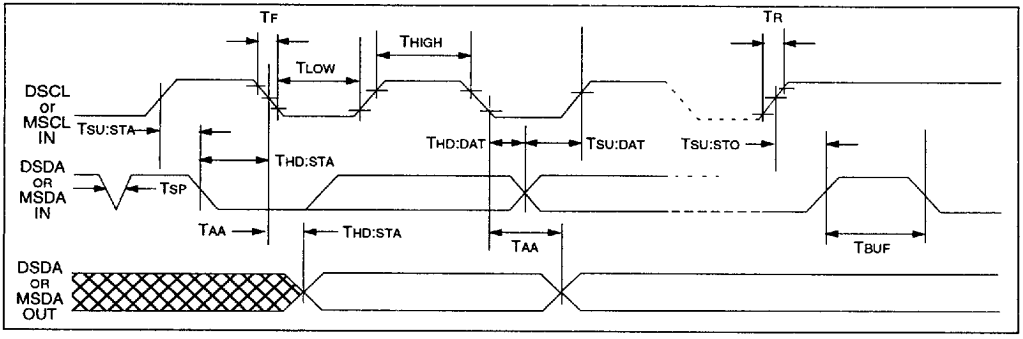
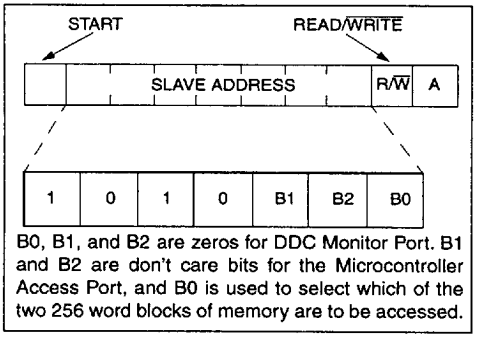


FIGURE 3-4: CONTROL BYTE ALLOCATION



B0, B1, and B2 are zeros for DDC Monitor Port. B1 and B2 are don't care bits for the Microcontroller Access Port, and B0 is used to select which of the two 256 word blocks of memory are to be accessed.

4.0 WRITE OPERATION

Write operations are identical for the DDC Monitor Port (when in Bi-directional Mode) and the Microcontroller Access Port, with the exception of the VCLK and MWP pins noted in the next sections. Data can be written using either a byte write or page write command. Write commands for the DDC Monitor Port and the Microcontroller Access Port are completely independent of one another.

4.1 Byte Write

Following the start signal from the master, the slave address (4-bits), the chip select bits (3-bits) and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the port. After receiving another acknowledge signal from the port, the master device will transmit the data word to be written into the addressed memory location. The port acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time, the port will not generate acknowledge signals (see Figure 4-1).

For the DDC Monitor Port it is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming. The MWP pin must be held high for the duration of the write protection.

4.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the port in the same way as in a byte write. But, instead of generating a stop condition, the master transmits up to eight data bytes to the DDC Monitor Port or 16 bytes to the Microcontroller Access Port, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order 5-bits of the word address remains constant. If the master should transmit more than eight words to the DDC Monitor Port or 16 words to the Microcontroller Access Port prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 4-2).

For the DDC Monitor Port, it is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming. For the DDC Monitor Port, the MWP pin must be held high for the duration of the write cycle.

FIGURE 4-1: BYTE WRITE

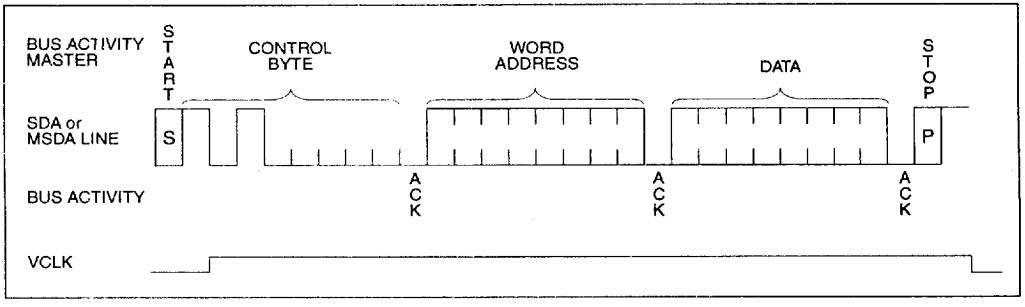


FIGURE 4-2: PAGE WRITE

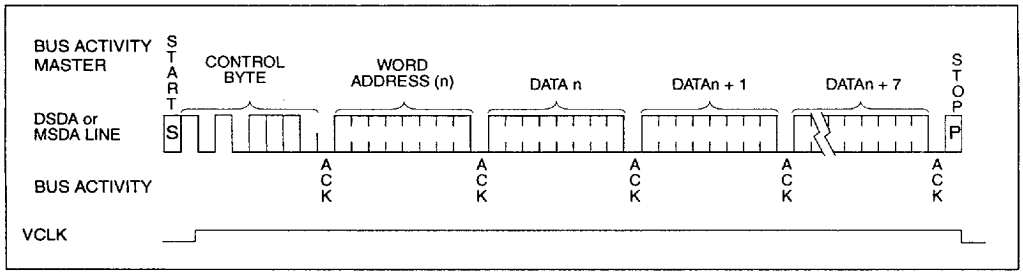
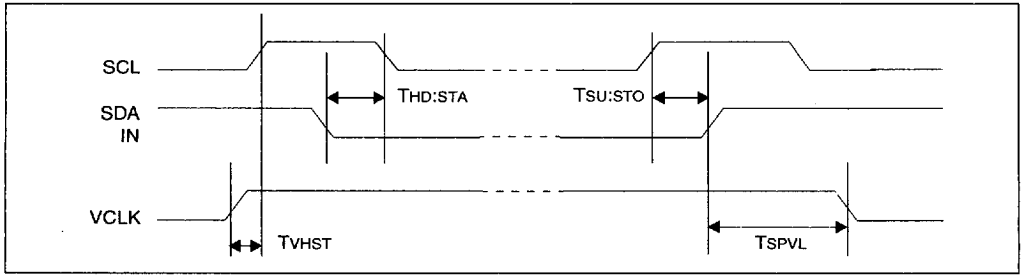


FIGURE 4-3: VCLK WRITE ENABLE TIMING

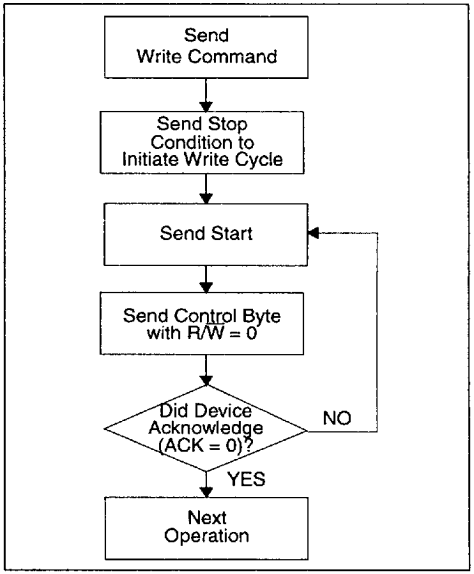


5.0 ACKNOWLEDGE POLLING

Acknowledge polling can be done for both the DDC Monitor Port (when in Bi-directional Mode) and the Microcontroller Access Port.

Since the port will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize but throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W}$=0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

6.1 DDC Monitor Port

When using the DDC Monitor Port in the Bi-directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to Vss would allow the monitor port to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read. These operations are identical for both the DDC Monitor Port (in Bi-directional Mode) and the Microcontroller Access Port and are completely independent of one another.

7.1 Current Address Read

The port contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the port issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (see Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the port as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a one. The port then issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the port discontinues transmission (see Figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the port transmits the first data byte, and the master issues an acknowledge as opposed to a stop condition in a random read. This directs the port to transmit the next sequentially addressed 8-bit word (see Figure 7-3).

To provide sequential reads, the port contains an internal address pointer, which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

Both the DDC Monitor Port and Microcontroller Access Port employ a Vcc threshold detector circuit which disables the internal erase/write logic, if the Vcc is below 1.5 volts at nominal conditions.

The VCLK, DSCL, MSCL, DSDA, and MSDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 7-1: CURRENT ADDRESS READ

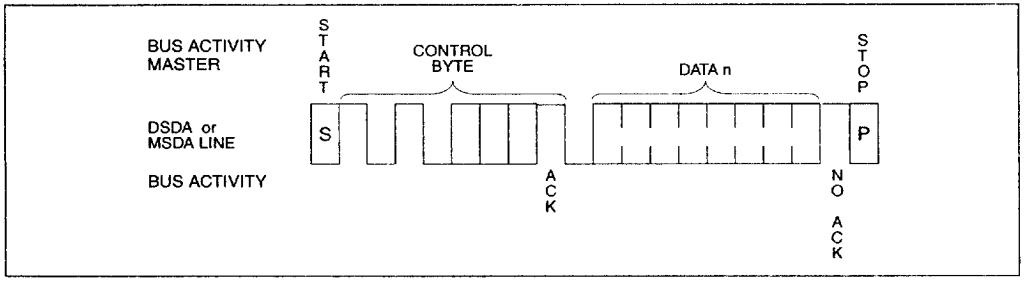


FIGURE 7-2: RANDOM READ

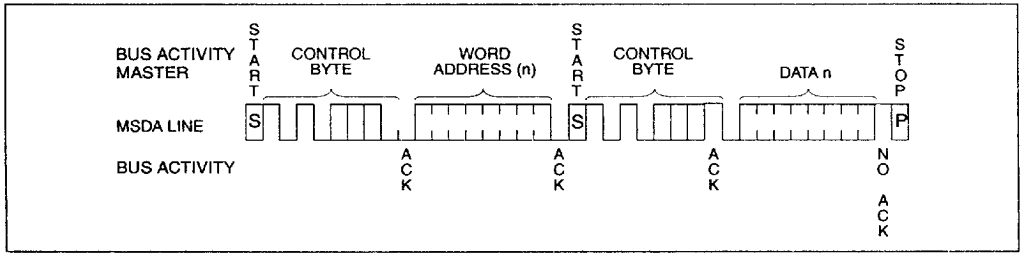
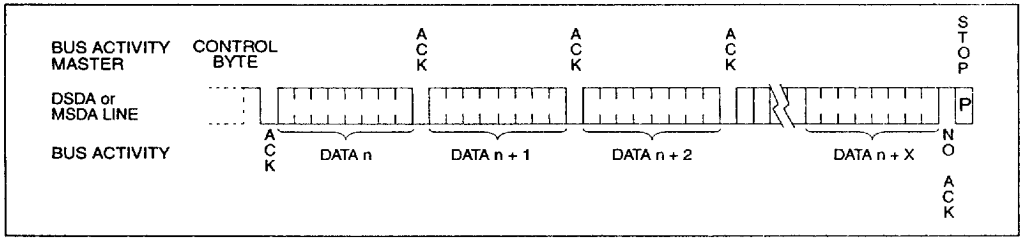


FIGURE 7-3: SEQUENTIAL READ



8.0 PIN DESCRIPTIONS

8.1 DSDA

This pin is used to transfer addresses and data into and out of the DDC Monitor Port, when the device is in the Bi-directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the DSDA pin. This pin is an open drain terminal, therefore the DSDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer in the Bi-directional Mode, DSDA is allowed to change only during DSCL or MSDA low. Changes during DSCL high are reserved for indicating the START and STOP conditions.

8.2 DSCL

This pin is the clock input for the DDC Monitor Port while in the Bi-directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit-Only Mode to the Bi-directional Mode. It must remain high for the chip to continue operation in the Transmit-Only Mode.

8.3 VCLK

This pin is the clock input for the DDC Monitor Port while in the Transmit-Only Mode. In the Transmit-Only Mode, each bit is clocked out on the rising edge of this signal. In the Bi-directional Mode, a high logic level is required on this pin to enable write capability.

8.4 MWP

This pin is used to write protect the 4K memory array for the Microcontroller Access Port.

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

8.5 MSCL

This pin is the clock input for the Microcontroller Access Port, and is used to synchronize data transfer to and from the device.

8.6 MSDA

This pin is used to transfer addresses and data into and out of the Microcontroller Access Port. This pin is an open drain terminal, therefore the MSDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

MSDA is allowed to change only during MSCL low. Changes during MSCL high are reserved for indicating the START and STOP conditions.

24LC41A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.