Migration from Am29LV640DU to MirrorBit Am29LV640MU

Application Note

July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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Migration from Am29LV640DU to MirrorBit™ Am29LV640MU

Application Note

INTRODUCTION

Note: This application note assumes that users are familiar with Flash Technology and HW/SW System Design.

AMD's MirrorBit™ technology offers customers a low-cost Flash Memory solution. MirrorBit technology enables a Flash memory product to hold twice as much data as standard Flash, without compromising device endurance, performance, or reliability.

AMD's MirrorBit Am29LV640MU device is pin-compatible with AMD's Am29LV640DU product. The products are very similar, enabling easy migration. Along with improvements added to the Am29LV640MU, there are a few minor changes between the two products. This application note will focus on these changes and new performance-enhancing features.

Migrate to MirrorBit

Am29LV640MU products are offered in the same 0.8mm pitch FBGA package and with the same pin out as AMD's Am29LV640DU product. As an extension to the previous product offering, the Am29LV640DU is also available in the 1.0 mm pitch Fortified BGA package to support migration to the 64 Mbit MirrorBit device, the Am29LV640MU. Existing systems using Am29LV640DU can migrate to MirrorBit Am29LV640MU without board redesign. For more information on alternate MirrorBit Packages, refer to the "MirrorBit Packages" application note, publication number 25694.

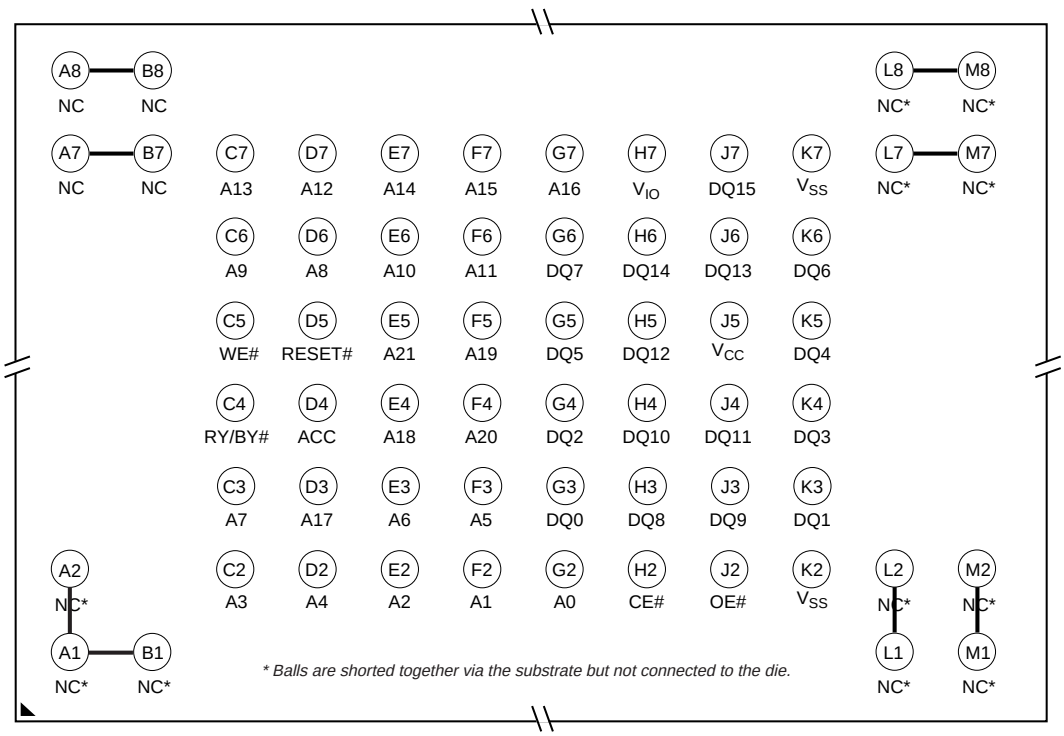

Figure 1. Fine-Pitch BGA Package (63-ball) Connection Diagram

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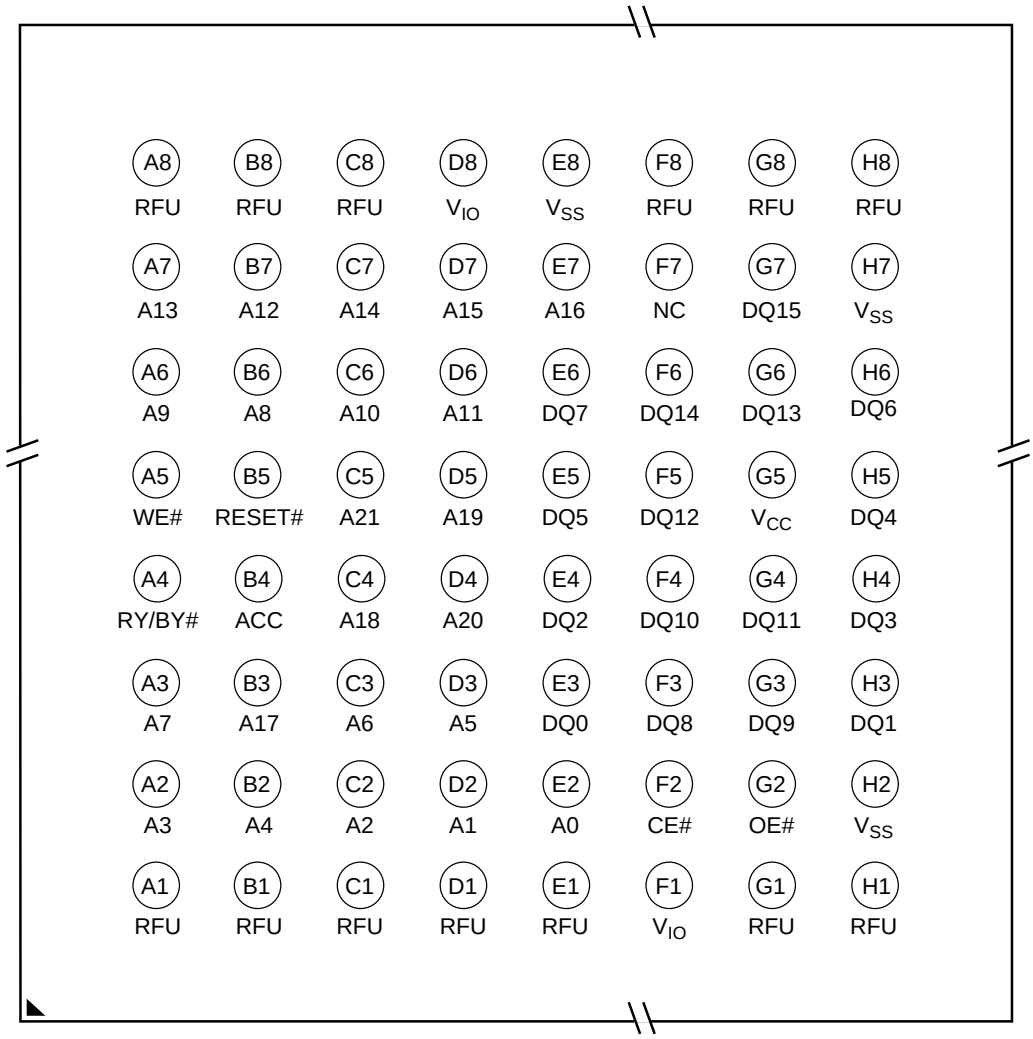

Figure 2. Fortified BGA (1.0 mm Pitch) Connection Diagram

Device ID Change on AMD MirrorBit Devices

Device Identification (ID) in AMD Flash devices is available either via a software command sequence or through a high voltage hardware method. Device ID is a unique set of readable data values, which distinguishes between different vendors and device type. The main difference between Am29LV640DU and MirrorBit Am29LV640MU is the Am29LV640DU uses a single-byte device code whereas Am29LV640MU uses a three-byte device code.

Tables 1 and 2 show the difference between single-byte device code and three-byte device code using the high-voltage hardware method.

Table 1. Device ID for Am29LV640DU, High Voltage Method

Description	CE#	OE#	WE#	A21–A15	A14–A10	A9	A8–A7	A6	A5–A2	A1	A0	DQ15–DQ0
Manufacturer ID: AMD	L	L	H	X	X	VID	X	L	X	L	L	0001h
Device ID: Am29LV640D	L	L	H	X	X	VID	X	L	X	L	H	22D7h

Note: *V_{ID} = 8.5 – 12.5 V.*

Table 2. Device ID for Am29LV640MU, High Voltage Method

Description	CE#	OE#	WE#	A21–A10	A9	A8	A7	A6	A5–A4	A3	A2	A1	A0	DQ15–DQ0
Manufacturer ID: AMD	L	L	H	X	V_{ID}	X	X	L	X	X	X	L	L	0001h
Device ID Read 1	L	L	H	X	V_{ID}	X	X	L	X	L	L	L	H	227Eh
Device ID Read 2	L	L	H	X	V_{ID}	X	L	L	L	H	H	H	L	2213h
Device ID Read 3	L	L	H	X	V_{ID}	X	L	L	L	H	H	H	H	2201h

Note: *V_{ID} = 8.5 – 12.5 V.*

The Device ID read command sequence is extended from four to six cycles for MirrorBit devices. In the device code only the lower byte of the data bus is meaningful. All three bytes of the device code must be read to determine the device type. The first byte of the code (7E) only indicates that there are two more Device ID bytes to be read. For more detailed information on Three-Byte Device Code refer to Migration from Single-Byte to Three-Byte Device IDs" application note, publication number 25538.

Tables 3 and 4 illustrate different bus cycles between Am29LV640DU and Am29LV640MU.

Table 3. Device ID Command Sequence for Am29LV640DU

Command Sequence	Bus Cycles							
	First		Second		Third		Fourth	
	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Manufacturer ID	555	AA	2AA	55	555	90	X00	0001
Device ID	555	AA	2AA	55	555	90	X01	22D7

Table 4. Device ID Command Sequence for Am29LV640MU

Command Sequence	Bus Cycles											
	First		Second		Third		Fourth		Fifth		Sixth	
	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Manufacturer ID	555	AA	2AA	55	555	90	X00	0001				
Device ID	555	AA	2AA	55	555	90	X01	227E	X0E	2213	X0F	2201

Difference in Power Consumption

MirrorBit Am29LV640MU devices have higher power consumption during active read. Active read current is higher due to the new page mode access feature. Erase/Program current is higher because the device will program up to 8 bits at a time instead of the traditional 4 bits. These new features mean that reading, programming, and erase occur in less time. The active power is higher but over a shorter period of time. Table 5 compares power consumption between Am29LV640DU and Am29LV640MU.

Table 5. Power Consumption

Specification		LV640MU	LV640DU
Current Consumption			
Initial Read		30 mA	9 mA
Intra-Page Read		10 mA	N/A
Program		50 mA	26 mA
Erase		50 mA	26 mA
Standby		1 µA	0.4 µA
Accelerated Program	ACC pin	10 mA	5 mA
	V_{CC} pin	30 mA	15 mA
Power Consumption			
Random Read		90 mW	27 mW
Intra-Page Read		30 mW	N/A
Program		150 mW	78 mW
Erase		150 mW	78 mW
64 KByte Sector Erase		3 µW	1.2 µW
Accelerated Program (ACC pin)		210 mW	87 mW
Energy Consumption (based on operational timing below)			
4-Word Read	Page	10.35 nJ	N/A
	Random	32.4 nJ	9.72 nJ
16-Word Program	Buffer	14.16 µJ	N/A
	Random	307.2 µJ	13.73 µJ
64 KByte Sector Erase		60 mJ	124.8 mJ
16-Word Accelerated Program (ACC pin)		23.52 µJ	9.744 µJ
Operation Timing			
Initial Read		90 ns	90 ns
Intra-Page Read		25 ns	N/A
1-Word Program		5.9 µs	11 µs
Sector Erase		0.4 s	1.6 s
1-Word Accelerated Program		7 µs	7 µs

New Page Read Buffer and Write Buffer Features

Page Read Buffer and Page Write Buffer are two new performance-enhancing features in MirrorBit devices.

The Page Read Buffer feature increases read performance significantly. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words. Pages are located on 4 word boundaries. The first access within a page requires the full random access time for the device, 90 to 120ns depending on the speed grade. Subsequent accesses that remain within the same page address range, while Chip Select (CE#) remains asserted, have a reduced page access time of 25 to 40 ns. The page read buffer is automatically used by standard read accesses. No special commands or signals are needed. The system only needs to keep CE# active throughout page mode accesses and be aware of the reduced access time for accesses remaining within a page. The system can reduce the number of wait states for within page accesses and take advantage of the increased read performance.

The addition of a Page Write Buffer doubles the programming throughput compared to current Am29LV640DU devices. The Page Write Buffer is a set of registers used to hold several words that are to be programmed as a group. The Page Write Buffer allows the system to write to a maximum of 16 words in one programming operation. The Write Buffer programming command sequence is initiated by first writing two unlock cycles. Below is the flowchart for Write Buffer Programming. See "MirrorBit™ Flash Memory Write Buffer Programming and Page Mode Read" application note, publication 25539, for more detailed information.

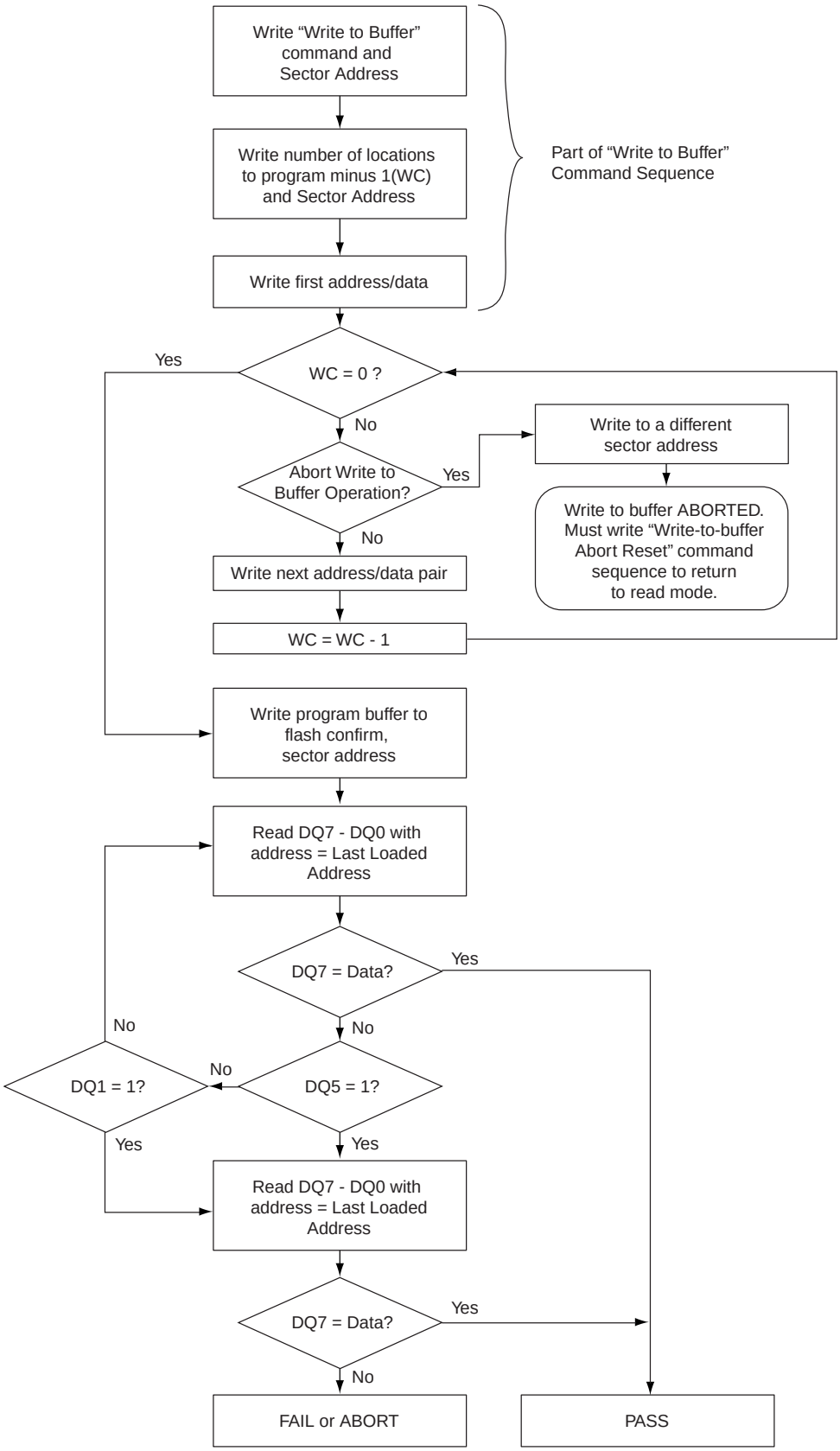

Figure 3. Write Buffer Programming Flowchart

CONCLUSION

MirrorBit technology is a major landmark in Flash memory. MirrorBit devices provide a Flash memory solution at a lower cost, without compromising device performance, endurance, or reliability. Am29LV640MU devices in 0.8 mm FBGA are pin-compatible with AMD's current Am29LV640DU product family of devices in the same package ranging from 8 Mb to 64 Mb. Therefore it is easy to migrate from Am29LV640MU to Am29LV640DU. The addition of the Page Read Buffer and Page Write Buffer increases read performance and reduces the programming time bottleneck that is inherent to very high density Flash memory devices.

MirrorBit products are a superior and cost-competitive solution for designers requiring higher non-volatile memory densities.

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