# VersatileIO: DQ $V_{IO}$ and Enhanced $V_{IO}$

Application Note

July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

## Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

## Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

## For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **27174** Revision **A** Amendment **0** Issue Date **October 23, 2002**

# Versatile I/O: DQ–$V_{I/O}$ and Enhanced–$V_{I/O}$

***Application Note***

This document describes the two types of Versatile I/O provided by AMD Flash memory: DQ-$V_{I/O}$ and Enhanced-$V_{I/O}$. Also described are the benefits of designing with AMD's Versatile I/O Flash memory in terms of reducing system complexity, and the limitations of each type of Versatile I/O interface.

## What is Versatile I/O ($V_{I/O}$)

Versatile I/O ($V_{I/O}$) is used on AMD Flash memory to provide support for I/O signaling that is outside the "normal" operating range of a device. Versatile I/O allows a 3.0V AMD Flash to be compatible with 2.5V or 1.8V devices without the need of expensive voltage translation buffers, as shown in Figure 1. Also, Versatile I/O enables this without affecting the overall performance of the Flash device.

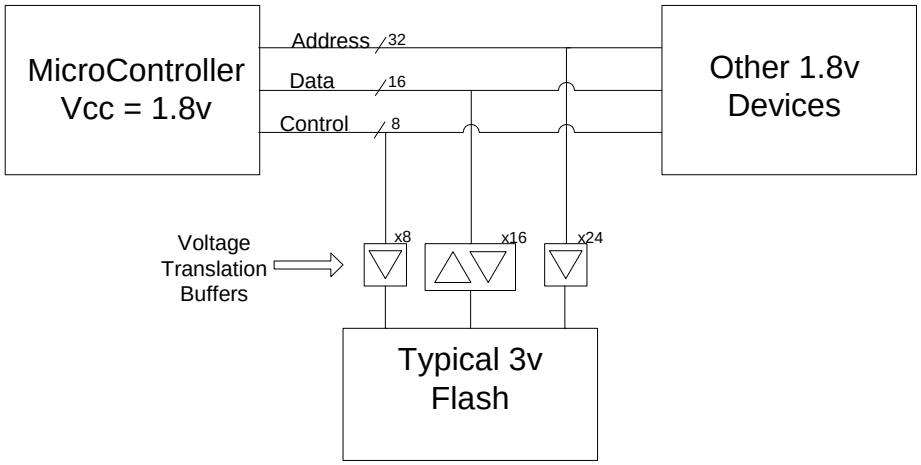


**Figure 1. I/O Signaling to Typical 3V Flash**

Versatile I/O devices can provide this internal voltage conversion because unlike traditional Flash memory, where a single power supply ($V_{CC}$) is used to power both the memory array and I/O pins, $V_{CC}$ only powers the memory array while the $V_{I/O}$ pin(s) power the I/O pins. This allows a Versatile I/O Flash device to directly interface with a wide variety of FPGAs, ASICs, microprocessors, microcontrollers, and other digital devices regardless of the device operating voltage. For example if a board is using a 3.0V AMD Flash, and a 1.8V microcontroller. A typical Flash would have problems since the typical minimum legal high for a 3.0V device is 2.1V (3.0V * 0.7 = 2.1V), this is higher than the source voltage of the 1.8V microcontroller. With AMD's Versatile I/O Flash memory the $V_{I/O}$ pin(s) would be connected to the 1.8V source used by the microcontroller, making the voltage levels for the inputs and outputs JEDEC 1.8V compliant.

## System Performance

The performance of the system shown in Figure 1 is also greatly affected because of the need for translation buffers. The buffers consume up to 100 mA of current each and data skew will occur any time a signal passes through the buffers. This data skew is due to variations in the propagation delay between parts and also between the individual pins on a buffer. However, the skew between individual pins is typically much smaller than between individual buffer chips.

The propagation delays through voltage translation buffers are highly variable, on the order of 2 ns to 7 ns, and discrepant on bi-directional buffers. In Figure 1,

Publication# **27174** Rev: **A** Amendment/**0**
Issue Date: **October 23, 2002**

there could be as much as a 5 ns delay between a control or clock signal and the data and address signals. This delay may also occur between the upper and lower address and/or data lines. To put this in perspective, if the Flash used in Figure 1 is a 66 MHz Flash, it could not be safely used at speeds above 50 MHz due to the uncertainty in the translation buffers' propagation delay.

## DQ–Versatile I/O (DQ–$V_{I/O}$)

AMD's DQ based Versatile I/O (DQ–$V_{I/O}$) follows an old standard for compatibility with Intel Flash devices and other legacy devices. This standard calls for the data pins (DQx) and chip enable (CE#) to be compatible with the Versatile I/O voltage while all other pins (Address, OE#, RY/BY#, etc) still require signaling at $V_{CC}$ voltage levels.

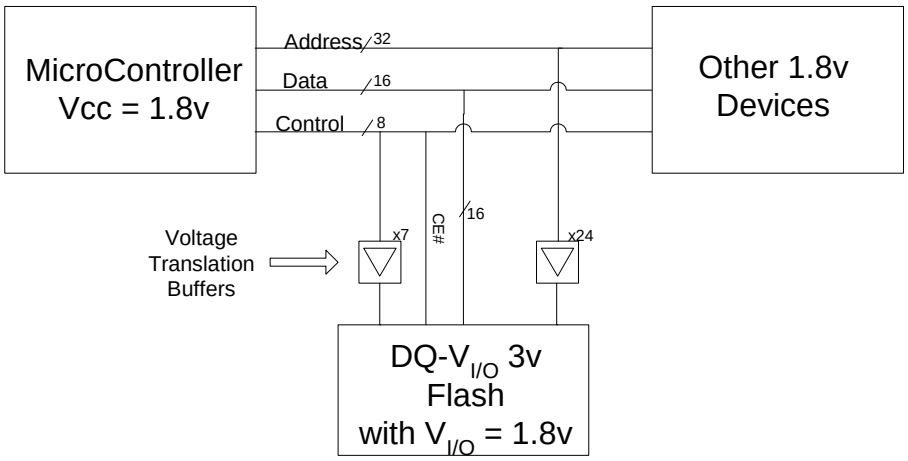


**Figure 2. I/O Signaling to DQ–$V_{IO}$ 3V Flash with $V_{IO}$ = 1.8V**

Therefore, as shown in Figure 2, only the data lines and chip select signals from the microcontroller and Flash can be connected together directly. The address lines, OE#, WE#, RESET#, RY/BY#, BYTE#, etc. would have to pass through voltage translation buffers in order for the Flash to receive legal high values and to prevent the microcontroller from being damaged by 3.0V signals from the Flash.

AMD's DQ–Versatile I/O may at first seem to be of limited use since only one 16-bit voltage translator is saved but this small change can greatly increase system performance. AMD's DQ–$V_{I/O}$ parts were designed on the assumption that most high-speed microprocessors will assert the address and control lines before asserting the data lines. By removing the need for voltage translation buffers on the data lines and assuming the address and control lines are asserted half a clock cycle before the data lines, the clock rate can be increased from 50 MHz to 66 MHz.

## Enhanced–Versatile I/O (Enhanced–$V_{I/O}$)

AMD's Enhanced–Versatile I/O is similar to the DQ–$V_{I/O}$, but with the added benefit of having all input and output pins being compatible with the Versatile I/O voltage and only the internal core memory and logic operating at the $V_{CC}$ voltage.

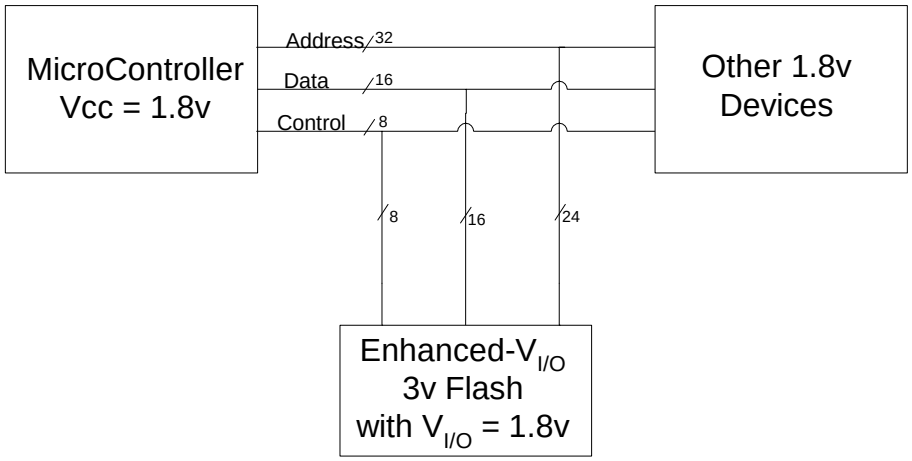


**Figure 3. I/O Signaling to Enhanced–$V_{IO}$ 3V Flash with $V_{IO}$ = 1.8V**

As shown in Figure 3, all the signals on the microcontroller and Flash can be directly connected together without the need of voltage translation buffers.

Without the need for translation buffers, data skew is no longer a significant problem even if the microcontroller does not assert the address and control lines before the data lines. The chip count and power consumption the circuit in Figure 3 has been reduced, from that of Figure 1, and the board space required and layout complexity have been significantly reduced.

## Voltage Range Limitations

Even though Versatile I/O expands the voltage range of AMD's Flash memories, the range is limited to (unless otherwise stated in the datasheet) the JEDEC standard voltage range given by the voltage on the $V_{I/O}$ pin(s). For example, if a 3.0V Versatile I/O Flash is used and 1.8V is being applied to the $V_{I/O}$ pin(s), applying 3.0V signals to the Flash device's I/O will damage the memory. In order to use 3.0V signals, the voltage applied to the $V_{I/O}$ pin(s) must be supplied at 3.0V. This limitation does not prevent the user from using multiple voltage levels when communicating with the Flash memory, it simply requires that the $V_{I/O}$ pin(s) be set to the appropriate voltage.

## Conclusion

AMD's Versatile I/O allows the designer to reduce cost, chip count, complexity and debug time on designs by eliminating the need for voltage translation buffers and the effects the buffers will have on signal integrity. In addition, designs can be upgraded from 3.0V systems to 2.5V or even 1.8V systems without the need to requalify a new Flash device.