T-46-13-29

Microchip

27HC1616

256K (16K x 16) High Speed CMOS UV Erasable PROM

FEATURES

- High speed performance
  —45ns Maximum access time
- CMOS Technology for low power consumption
  —90mA Active current
  —100µA Standby current (low power option)
- OTP (one time programming) available
- WordWide architecture offers space saving over Bytewide memories
- Two programming algorithms allow improved programming times
  —Fast programming
  —Express
- Organized 16K x 16: JEDEC standard pinouts
  —40-Pin dual in line package
  —44-Pin chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C
  —Military**: -55° C to 125° C

DESCRIPTION

The Microchip Technology Inc. 27HC1616 is a CMOS 256K bit (ultraviolet light) Erasable (electrically) Programmable Read Only Memory. The device is organized as 16K words of 16 bits each. Advanced CMOS technology allows bipolar speed with a significant reduction in power. A low power option (L) allows further standby power reduction to 100µA. The 27HC1616 is configured in the JEDEC WordWide pinout which allows a two for one package savings over Bytewide memories along with a significant PC board savings. This very high speed single chip solution is ideal for 16/32 bit digital signal processors (DSP) or other sophisticated microprocessors. A complete family of packages is offered to provide the utmost flexibility. One Time Programming (OTP) is available for low cost (plastic) applications.

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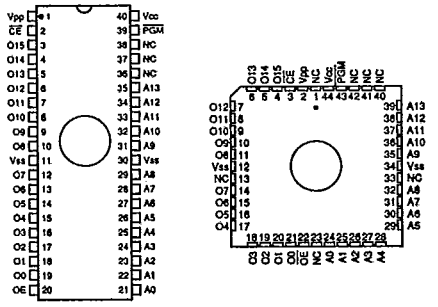
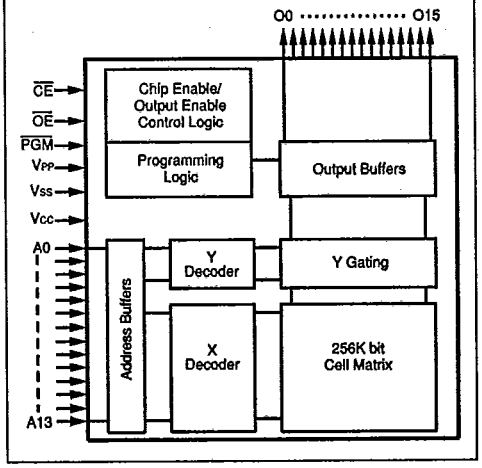
PIN CONFIGURATION

PIN CONFIGURATION

Top View



BLOCK DIAGRAM



** See 27HC1616 Military Data sheet DS60038

PIN FUNCTION TABLE	
Name	**Function**
A0 - A13	Address Inputs
CE	Chip Enable
OE	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O15	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC +1.0V
Temperature under bias .....-65°C to 125° C
Storage temperature .....-65°C to 150° C
ESD protection on all pins 2KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = -0.1 to VCC + 1.0V
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 2mA IOL = 8mA
Output Leakage	all		ILO	-10	10	µA	VOUT = -0.1 to VCC + 1.0V
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	all	TTL input	ICC1		90	mA	VCC = 5.5V; VPP = VCC f = 2MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S,SX		ICC(S)1		50	mA	
Power Supply Current, Standby	L, LX L, LX	TTL input CMOS input	ICC(S)2		3 100	mA µA	$\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: S = Standard Power; L = Low Power; X = Industrial Temp Range;
Notes: (1) AC Power component above 2MHz: 2mA/MHz.
(2) VCC must be applied simultaneously or before VPP and be removed simultaneously or after VPP.

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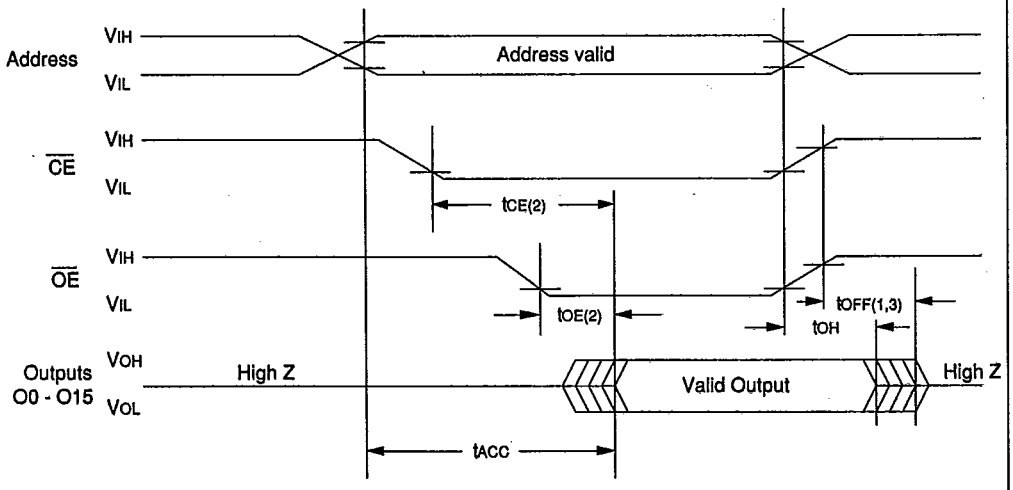
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0 V and V_{IL} = 0.0 V; V_{OH} = V_{OL} = 1.5 V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Sym	27HC1616-45		27HC1616-55		27HC1616-70		Units	Conditions
			Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}		45		55		70	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	L S	t_{CE1} t_{CE2}		45 30		55 35		70 45	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	t_{OE}		25		30		35	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	20	0	20	0	25	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	all	t_{OH}	0		0		0		ns	

* Parts: S = Standard Power; L = Low Power

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

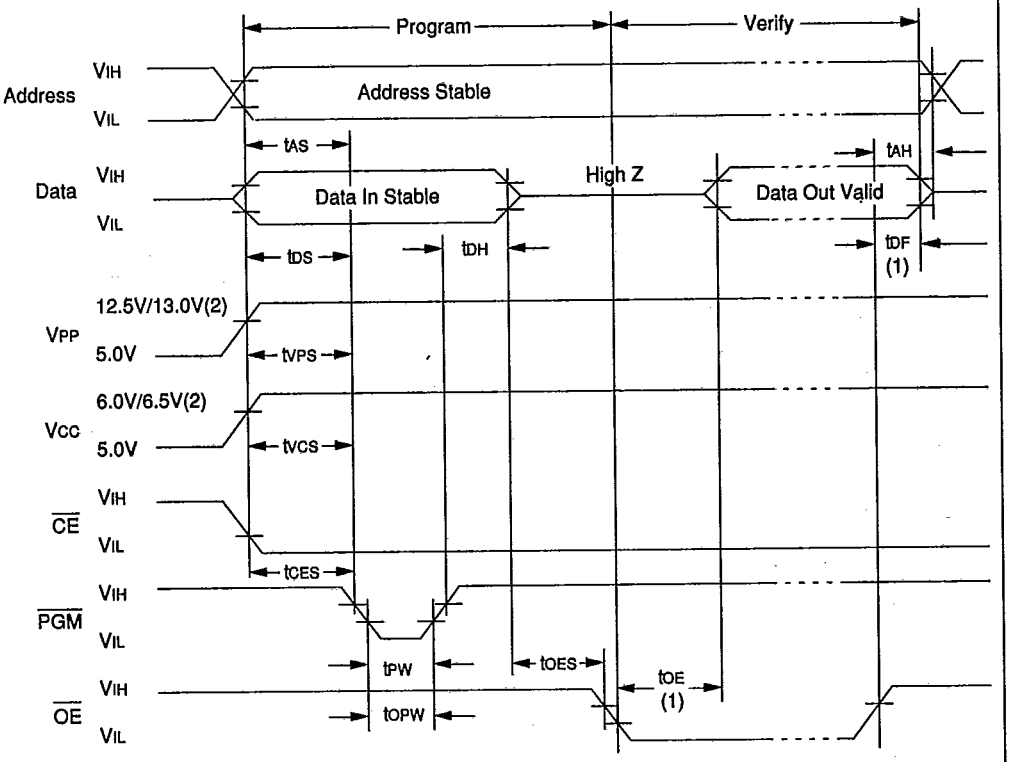
PROGRAMMING DC Characteristics	Ambient Temperature: 25° C ±5° C For VPP and Vcc Voltages refer to Programming Algorithms					
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -.1V to VCC + 1.0V
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 2mA IOL = 8mA
Vcc Current, program & verify		ICC		90	mA	Note 1
VPP Current,program		IPP		50	mA	Note 1
A9 Product Identification		VH	11.5	12.5	V	

Note: (1) Vcc must be applied simultaneously or before VPP and removed simultaneously or after VPP

PROGRAMMING AC Characteristics for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH = 2.4V; VIL = 0.45V; VOH = 2.0V and VOL = 0.8V Output Load: 1 TTL Load + 100 pF Ambient Temperature: 25° C ±5° C For VPP and Vcc Voltages, refer to Programming Algorithms				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	2		µs	
Data Set-Up Time	tDS	2		µs	
Data Hold Time	tDH	2		µs	
Address Hold Time	tAH	0		µs	
Float Delay (3)	tDF	0	130	ns	
Vcc Set-Up Time	tVCS	2		µs	
Program Pulse Width (1)	tPW	0.95	1.05	ms	1 ms typical
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2		µs	
$\overline{OE}$ Set-Up Time	tOES	2		µs	
VPP Set-Up Time	tVPS	2		µs	
Overprogram Pulse Width (2)	tOPW	2.85	78.75	ms	
Data Valid from $\overline{OE}$	tOE		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1 msec ± 5%.
(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.
(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accomodated by the programmer
(2) V_{CC} = 6.0V ±0.25V, V_{PP} = V_H = 12.5V ±0.5V for fast programming algorithm
V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for express algorithm

FUNCTIONAL DESCRIPTION

The 27HC1616 has the following functional modes:

—Operation: The 27HC1616 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.

—Programming: To receive its permanent data, the 27HC1616 must be programmed. Both a program and program/verify procedure is available. It can be programmed with Fast or Express algorithm.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

For the general characteristics in these operation and programming modes, refer to the table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A9	O0 - O15
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	X	D_{out}
Program	V_{IL}	V_{IH}	V_{IL}	V_H	X	D_{in}
Program Verify	V_{IH}	V_{IL}	V_{IH}	V_H	X	D_{out}
Program Inhibit	V_{IH}	X	X	V_H	X	High Z
Standby	V_{IH}	X	X	V_{CC}	X	High Z
Output Disable	X	V_{IH}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_H	Identity Code

X = Don't Care
V_H = 12.0 ±0.5V

OPERATION

Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC1616's memory data is accessed when

—the chip is enabled by setting the $\overline{CE}$ pin low.
—the data is gated to the output pins by setting the $\overline{OE}$ pin low.

For Read operations on the Low Power version, once the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). A faster $\overline{CE}$ access time (t_{CE}) is available on the standard part to provide the additional time for decoding the $\overline{CE}$ signal. Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$.

Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and the program mode is not defined. When these conditions are met, the supply current will drop from 90mA to 100µA on the low power part, and to 50mA on the standard part.

Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

Programming/Verification

The 27HC1616 has to be programmed, and afterward the programmed information verified. Before these operations, the Identity Code can be read to properly set up automated equipment. Multiple devices in parallel can be programmed using the programming and inhibit modes.

Programming Algorithms

Two programming algorithms are available: fast programming and express.

The fast programming algorithm is the industry standard programming mode that requires both initial programming pulses and overprogramming pulses. A flowchart of the algorithm is shown in Figure 1.

The express algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100µsec each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure 2.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ pin is pulsed low.

Since the erase state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A13, and the data is presented to pins O0 - O15. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{OE}$ line is low
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ line is high.

Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{PGM}$ needs to be under separate control to each device. By pulsing the $\overline{PGM}$ line low on a particular device, that device will be programmed, and all other devices with corresponding $\overline{PGM}$ or $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin →	Input	Output*								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	1	1	1	97

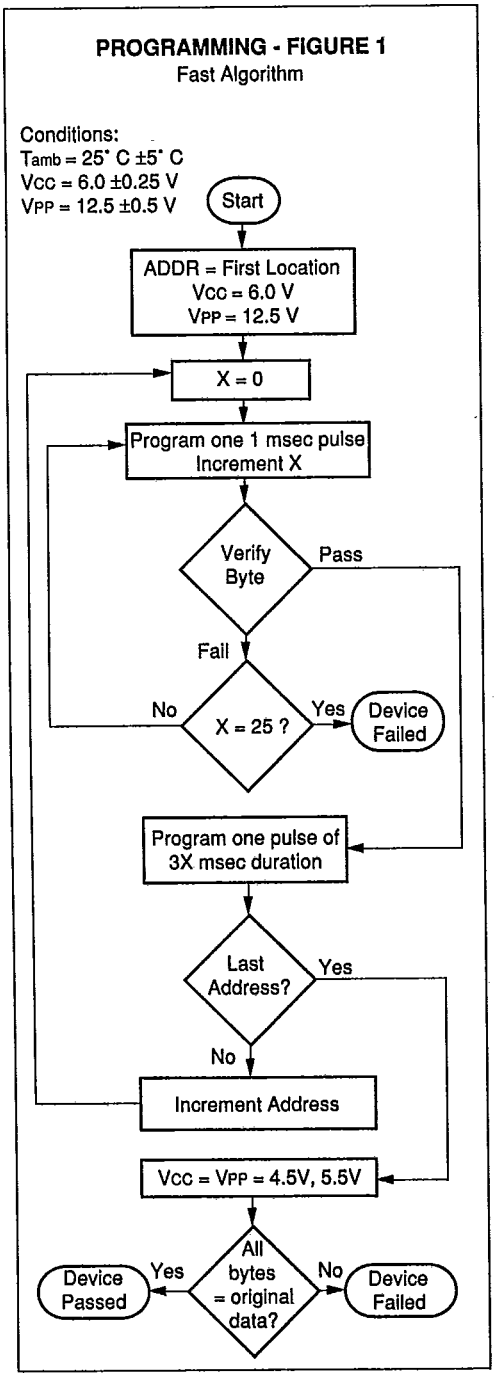
*Code subject to change.
Note: O15 - O8 are 00 for the manufacturer and device type code.

Erasure

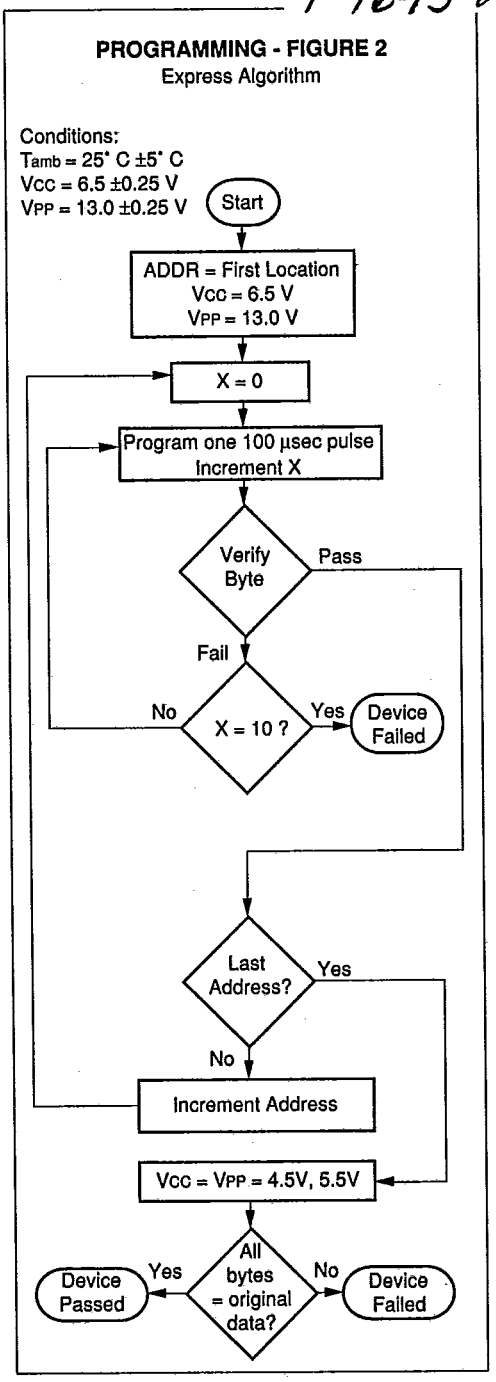
Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537Å with an intensity of 12,000µW/cm² at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

PROGRAMMING - FIGURE 1
Fast Algorithm



PROGRAMMING - FIGURE 2
Express Algorithm



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27HC1616 - 45 I / K

Package:	J	Cerdip DIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
Temperature Range:	Blank	0° C to 70° C
	I	-40° C to 85° C
Access Time:	45	45 nsec
	55	55 nsec
	70	70 nsec
Device	27HC1616	256K (16K x 16) High Speed CMOS EPROM
	27HC1616L	256K (16K x 16) High Speed Low Power CMOS EPROM