7.0 Electrical and Mechanical Specifications

7.1 Electrical and Environmental Specifications

7.1.1 Absolute Maximum Ratings

CAUTION

Stressing the device parameters above absolute maximum ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{dd}	–0.3 to 7	V
DC Input Voltage	V_{in}	–0.5 to V_{dd} +0.5	V
Continuous Power Dissipation	P_d	750	mW
Operating Junction Temperature	T_{jc}	125	°C
Storage Temperature	T_s	–55 to +125	°C

7.1.2 Recommended Operating Conditions

Table 7-2. Recommended 5 V Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{dd}	4.75 to 5.25	V
Ambient Operating Temperature KPF EPF	T_{ac}	 0 to +70 –40 to +85	 °C °C
High-Level Input Voltage	V_{ih}	2.0 to V_{dd} +0.3	V
Low-Level Input Voltage	V_{il}	–0.3 to 0.8	V
High-Level Output Current Source	I_{oh}	200 to 400	µA
Low Level Output Current Sink	I_{ol}	2 to 3	mA
Output Capacitive Loading	C_{ld}	60	pF

7.1.3 Electrical Characteristics

Table 7-3. Electrical Characteristics for 5 V Operation

Parameter	Symbol	Value	Unit
High-Level Output Voltage	V_{oh}	2.4	V
Low-Level Output Voltage	V_{ol}	0.4	V
Input Leakage Current	I_{l}	–10 to 10	µA
Three-state Leakage Current	I_{oz}	–10 to 10	µA
Resistive Pullup Current	I_{pr}	100 to 500	µA
Supply Current	I_{dd}	130	µA

7.2 Timing and Switching Specifications

7.2.1 Overview

The major subsystems of MUSYCC include the host interface, the expansion bus interface, and the serial interface. The host interface is Peripheral Component Interface (PCI) compliant. For other references to PCI, see the PCI Local Bus Specification, Revision 2.1, June 1, 1995. The expansion bus and serial bus interfaces are similar to the host interface timing characteristics; the differences and specific characteristics common to either interface are further defined.

7.2.2 Host Interface (PCI) Timing and Switching Characteristic

Reference the PCI Local Bus Specification, Revision 2.1, June 1, 1995 for information on:

- Indeterminate inputs and metastability.
- Power requirements, sequencing, decoupling.
- PCI DC specifications.
- PCI AC specifications.
- PCI V/I curves.
- Maximum AC ratings and device protection.

Table 7-4. PCI Interface DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
V_{dd}	Supply Voltage	—	4.75	5.25	V
V_{ih}	Input High Voltage	—	2.0	V_{dd}+ 0.5	V
V_{il}	Input Low Voltage	—	–0.5	0.8	V
I_{ih}	Input High Leakage Current(1)	V_{in} = 2.7 V	—	70	µA
I_{il}	Input Low Leakage Current(1)	V_{in} = 0.5 V	—	–70	µA
V_{oh}	Output High Voltage	I_{out} = –2 mA	2.4	—	V
V_{ol}	Output Low Voltage(2)	I_{out} = 3 mA I_{out} = 6 mA	—	0.55	V
C_{in}	Input Pin Capacitance	—	—	10	pF
C_{clk}	PCLK Pin Capacitance	—	5	12	pF
C_{idsel}	IDSEL Pin Capacitance(3)	—	—	8	pF
L_{pin}	Pin Inductance	—	—	20	nH

NOTE(S):
(1) Input leakage currents include hi-Z output leakage for all bidirectional buffers with three-state outputs.
(2) Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include FRAME*, TRDY*, IRDY*, DEVSEL*, STOP*, SERR*, and PERR*.
(3) Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

Table 7-5. PCI Clock (PCLK) Waveform Parameters, 5 V Clock

Symbol	Parameter	Min	Max	Unit
T_{cyc}	Clock Cycle Time(1)	30	—	ns
T_{high}	Clock High Time	11	—	ns
T_{low}	Clock Low Time	11	—	ns
–	Clock Slew Rate(2)	1	4	mV/ns
V_{ptp}	Peak-to-Peak Voltage	2	—	V

NOTE(S):
(1) MUSYCC works with any clock frequency between DC and 33 MHz, nominally. The clock frequency may be changed at any time during operation of the system as long as clock edges remain monotonic, and minimum cycle and high and low times are not violated. The clock may only be stopped in a low state.
(2) Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.

Figure 7-1. PCI Clock (PCLK) Waveform, 5 V Clock

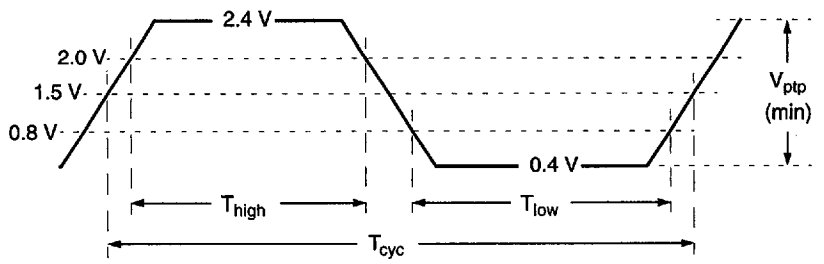


Table 7-6. PCI Reset Parameters

Symbol	Parameter	Min	Max	Unit
T_{rst}	Reset Active Time after Power Stable	1	—	ms
T_{rst_clk}	Reset Active Time after Clock Stable	100	—	µs
V_{nom}	Nominal Voltage Level(1)	—	—	V
–	RST* Slew Rate(2)	50	—	mV/ns
T_{fail}	Power Failure Detect Time(3)	—	—	—
$T_{rst-off}$	Reset Active to Float Delay	—	—	—

NOTE(S):
(1) The nominal voltage level refers to a voltage test point in the power up curve where the system can declare start of a "power good" signal.
(2) The minimum RST* slew rate applies only to the rising (deassertion) edge of the reset signal, and ensures that system noise cannot render an otherwise monotonic signal to appear to bounce in the switching range.
(3) The value of T_{fail} is the minimum of:
a. 500 ns (max) from power rail going out of specification by exceeding specified tolerances by more than 500 mV
b. 100 ns (max) from 5 V rail falling below 3.3 V rail by more than 300 mV.

Figure 7-2. PCI Reset Timing

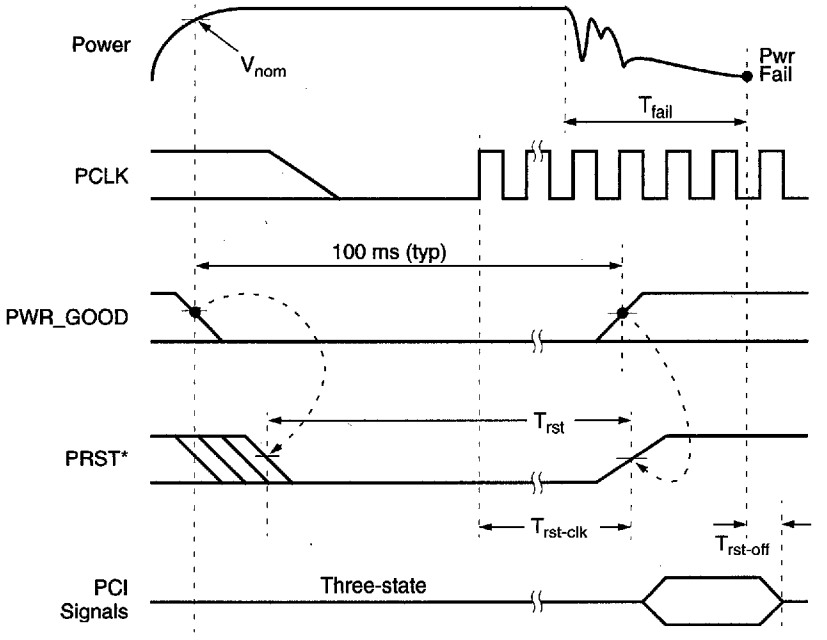


Table 7-7. PCI Input/Output Timing Parameters

Symbol	Parameter	Min	Max	Unit
T_{val}	PCLK to Signal Valid Delay – Bused Signal(1, 2)	2	11	ns
T_{val} (ptp)	PCLK to Signal Valid Delay – Point To Point(1, 2)	2	12	ns
T_{on}	Float to Active Delay(3)	2	—	ns
T_{off}	Active to Float Delay(3)	—	28	ns
T_{ds}	Input Setup Time to Clock– Bused Signal(2)	8.5	—	ns
T_{su} (ptp)	Input Setup Time to Clock – Point To Point(2)	10, 12	—	ns
T_{dh}	Input Hold Time from Clock	2.5	—	ns

NOTE(S):
(1) Minimum and maximum times are evaluated at 80 pF equivalent load. Actual test capacitance may vary, and results should be correlated to these specifications.
(2) REQ* and GNT* are the only point-to-point signals, and have different output valid delay and input setup times than do bused signals. GNT* has a setup of 10; REQ* has a setup of 12.
(3) For purposes of active/float timing measurements, the high-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification at 80 pF equivalent load.

Table 7-8. PCI Input/Output Measure Conditions

Symbol	Parameter	Value	Unit
V_{th}	Voltage Threshold High(1)	2.4	V
V_{tl}	Voltage Threshold Low(1)	0.4	V
V_{test}	Voltage Test Point	1.5	V
V_{max}	Maximum Peak-to-Peak(2)	2.0(3)	V
–	Input Signal Edge Rate	1	V/ns

NOTE(S):
(1) The input test for the 5 V environment is done with 400 mV of overdrive (over V_{ih} and V_{il}). Timing parameters must be met with no more overdrive than this. Production testing may use different voltage values, but must correlate results back to these parameters.
(2) V_{max} specifies the maximum peak-to-peak voltage waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.
(3) For TCLK the value is changed from 2.0 V to 2.5 V.

Figure 7-3. PCI Output Timing Waveform

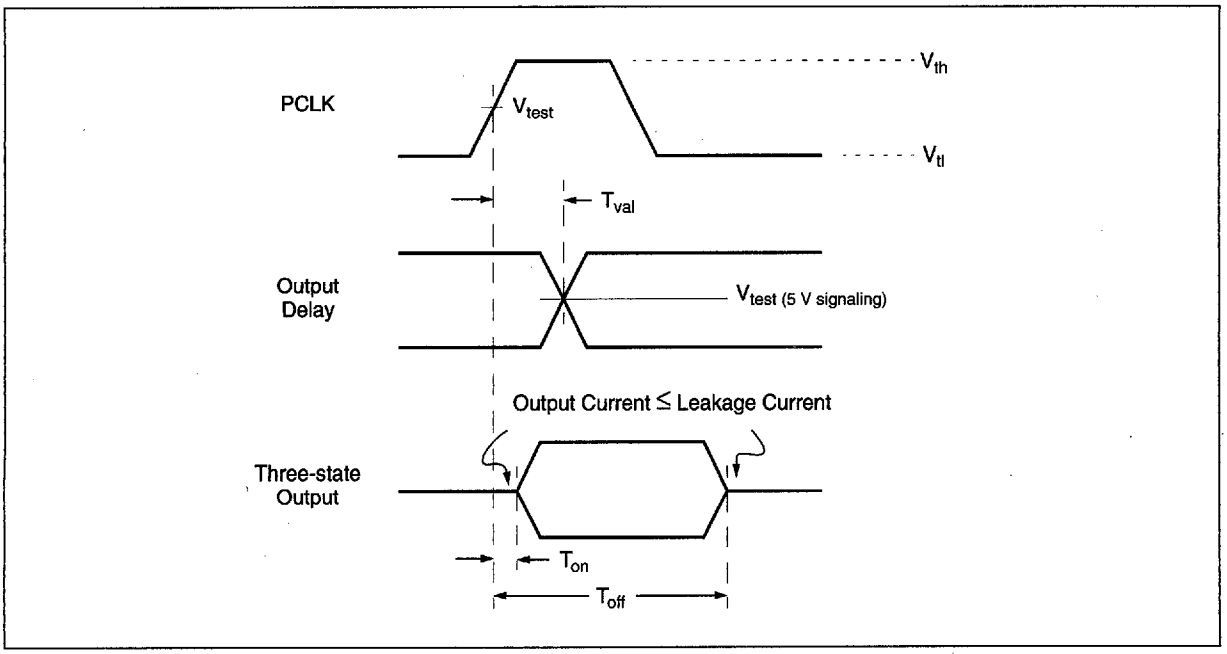


Figure 7-4. PCI Input Timing Waveform

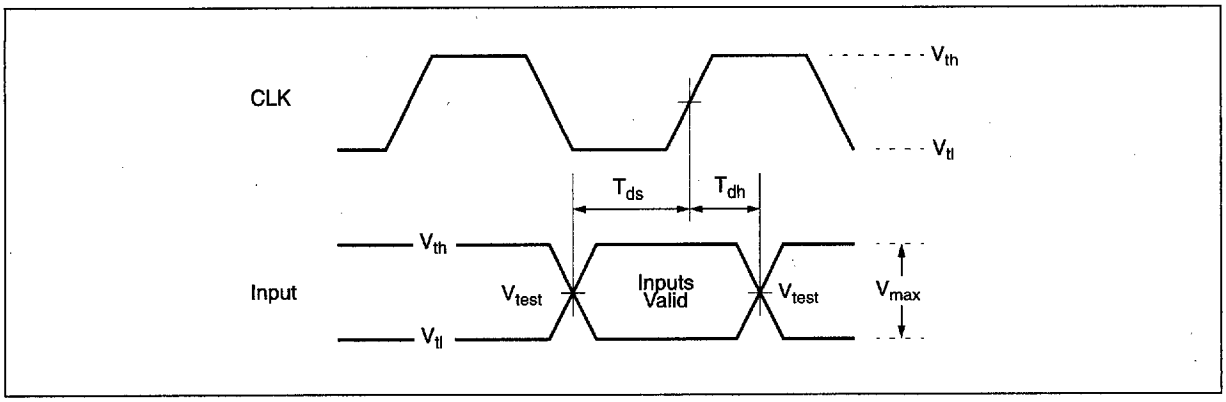


Figure 7-5. PCI Read Multiple Operation

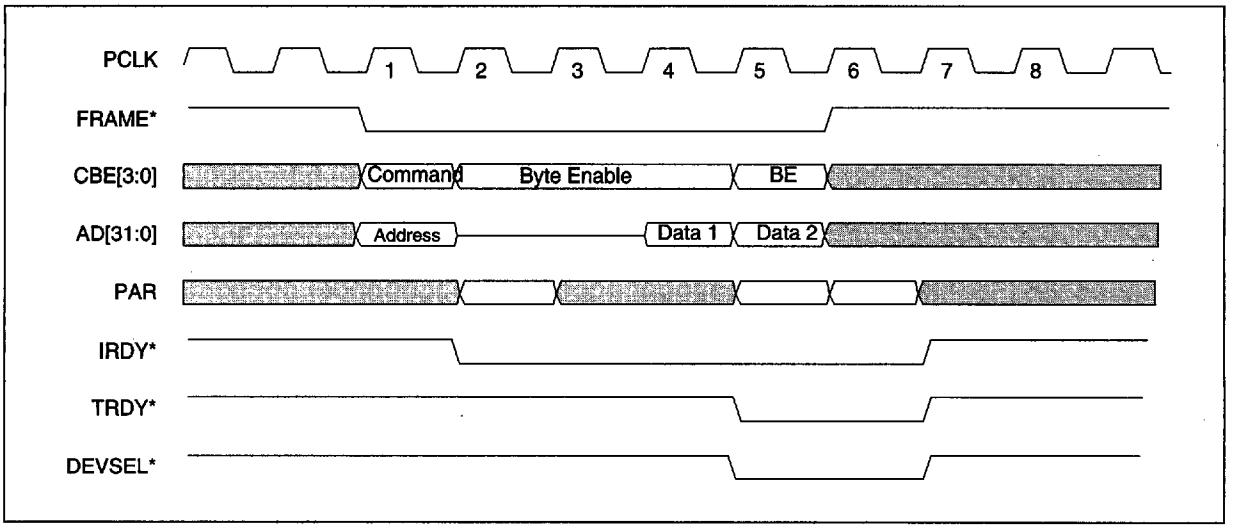


Figure 7-6. PCI Write Multiple Operation

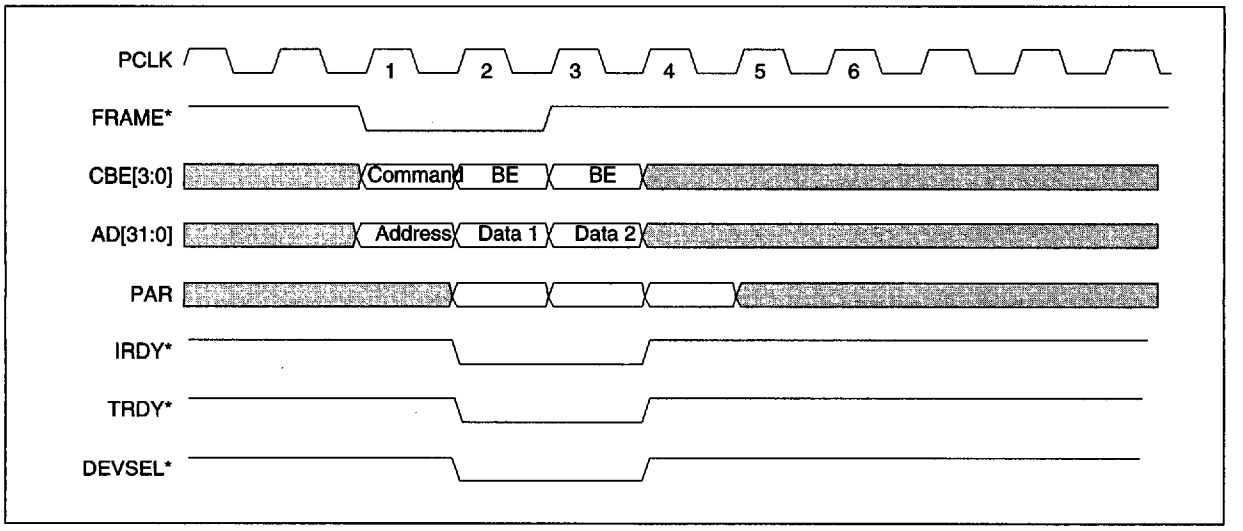
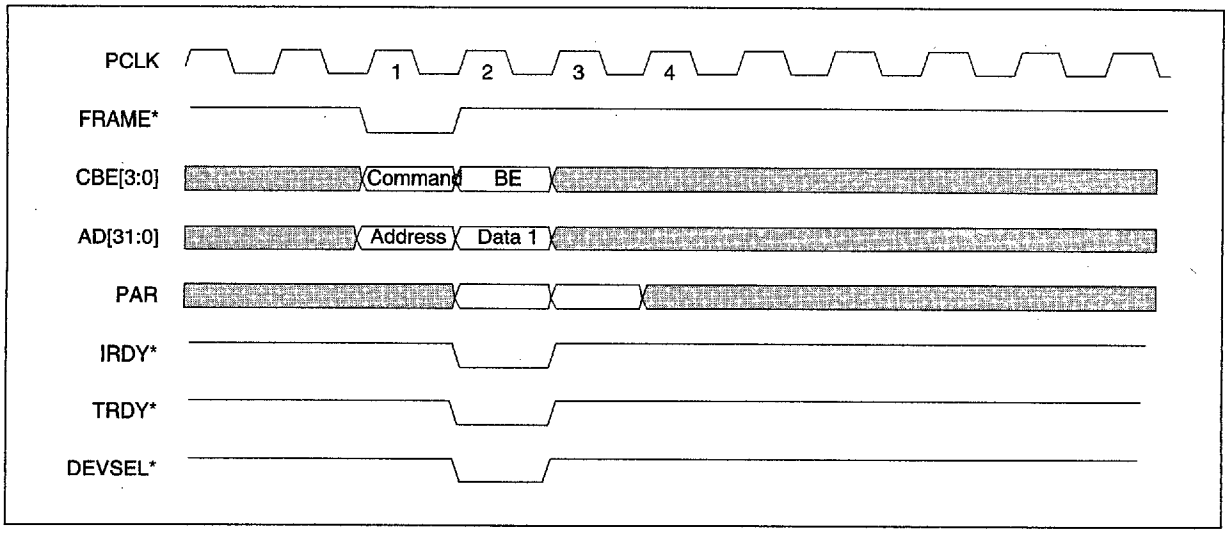


Figure 7-7. PCI Write Single Operation



7.2.3 Expansion Bus (EBUS) Timing and Switching Characteristic

The EBUS timing is derived directly from the PCI clock (PCLK) input to MUSYCC. The ECLK output is output as an inverted and a half-clock phase shifted PCLK (see Figure 7-8).

The EBUS input/output timing characteristics are identical to the PCI input/output timing characteristics.

The EBUS clock waveform characteristics are identical to the PCI clock waveform characteristics (see Tables 7-9 through 7-11 and Figures 7-9 through 7-11).

Figure 7-8. ECLK to PCLK Relationship

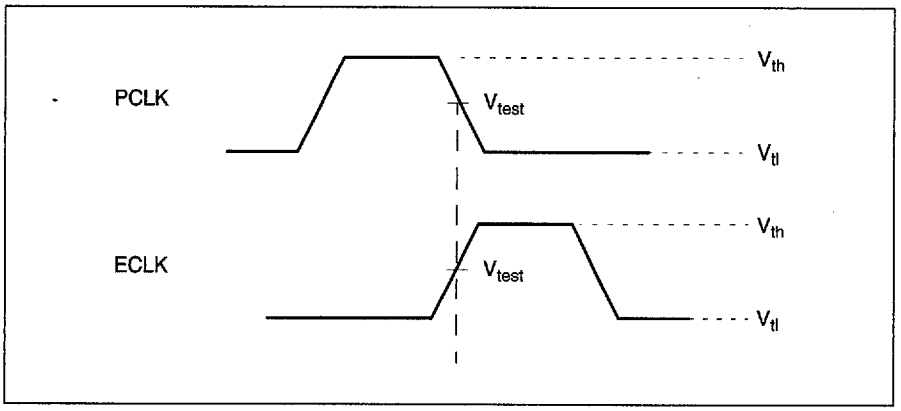
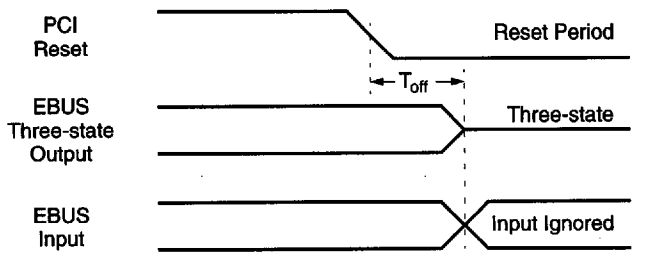


Table 7-9. EBUS Reset Parameters

Symbol	Parameter	Min	Max	Units
T_{off}	Active to Inactive Delay(1)		28	ns

NOTE(S):
(1) For purposes of active/float timing measurements, the high-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 7-9. EBUS Reset Timing



NOTE(S): The EBUS reset is dependent on the PRST* (PCI Reset) signal being asserted low.

Table 7-10. EBUS Input/Output Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{val}	ECLK to Signal Valid Delay – Bused Signal(1)	2	11	ns
T_{val} (ptp)	ECLK to Signal Valid Delay – Point To Point(1)	2	12	ns
T_{on}	Float to Active Delay(2)	2		ns
T_{off}	Active to Float Delay(2)		28	ns
T_{ds}	Input Setup Time to Clock – Bused Signal	8.5		ns
T_{ds} (ptp)	Input Setup Time to Clock – Point To Point	10		ns
T_{dh}	Input Hold Time from Clock	2.5		ns

NOTE(S):
(1) Minimum and maximum times are evaluated at 80 pF equivalent load. Actual test capacitance may vary, and results should be correlated to these specifications.
(2) For purposes of active/float timing measurements, the hi-z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification at 80 pF equivalent load.

Table 7-11. EBUS Input/Output Measure Conditions

Symbol	Parameter	Value	Units
V_{th}	Voltage Threshold High(1)	2.4	V
V_{tl}	Voltage Threshold Low(1)	0.4	V
V_{test}	Voltage Test Point	1.5	V
V_{max}	Maximum Peak-to-Peak(2)	2.0	V
–	Input Signal Edge Rate	1	V/ns

NOTE(S):
(1) The input test for the 5 V environment is done with 400 mV of overdrive (over V_{ih} and V_{il}). Timing parameters must be met with no more overdrive than this. Production testing may use different voltage values, but must correlate results back to these parameters.
(2) V_{max} specifies the maximum peak-to-peak voltage waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.

Figure 7-10. EBUS Output Timing Waveform

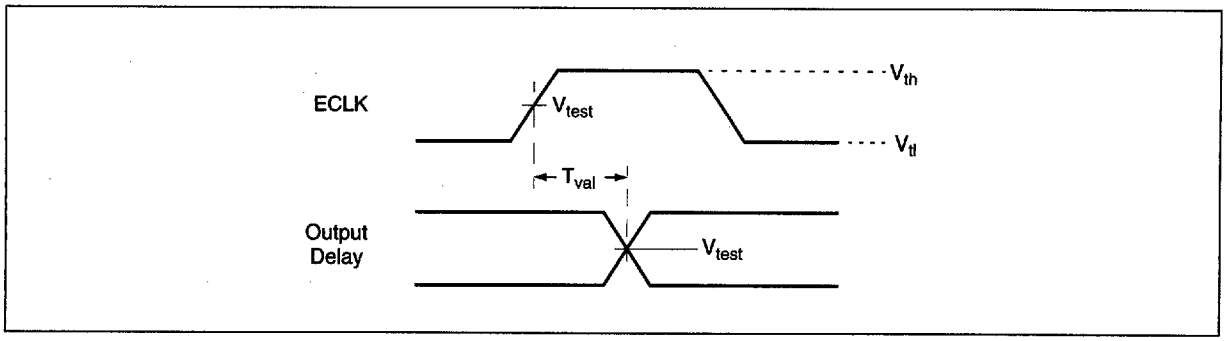
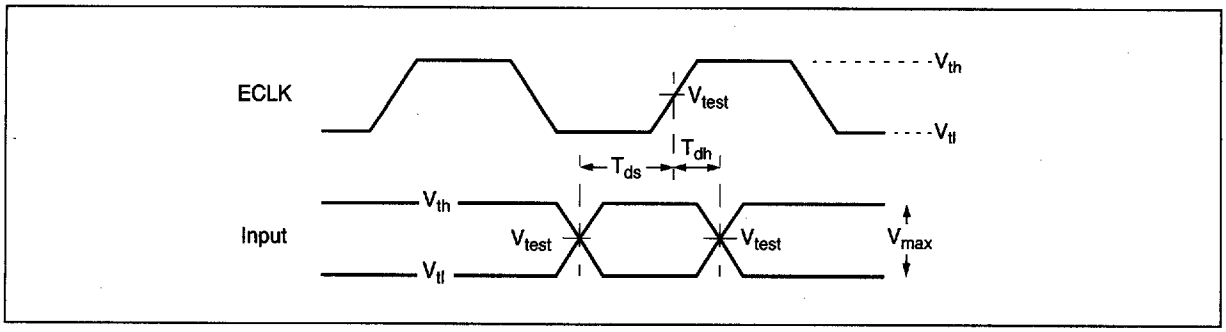


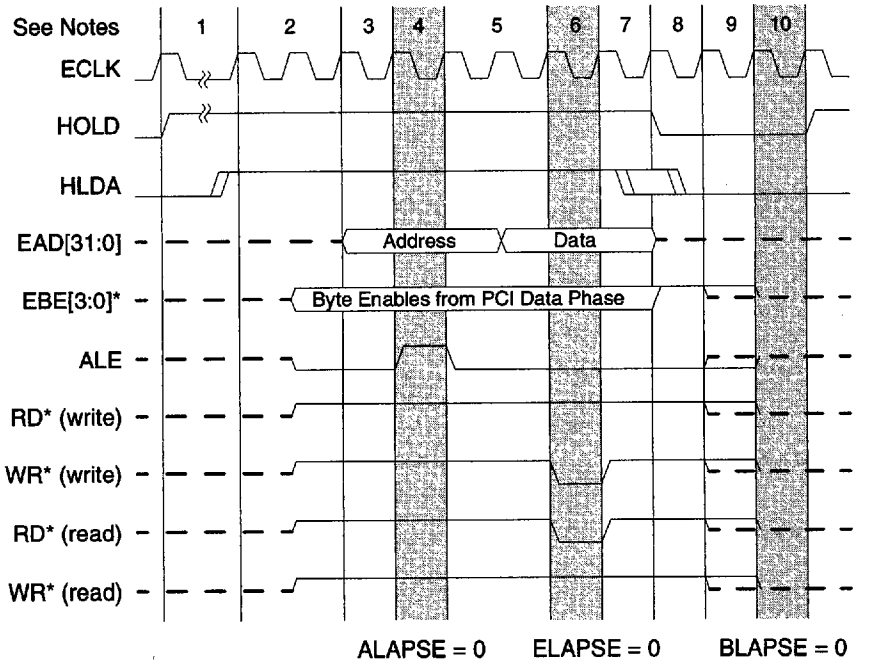
Figure 7-11. EBUS Input Timing Waveform



7.2.4 EBUS Arbitration Timing

Intel-style write/read transactions are illustrated in Figure 7-12. Motorola-style write/read transactions are illustrated in Figure 7-13.

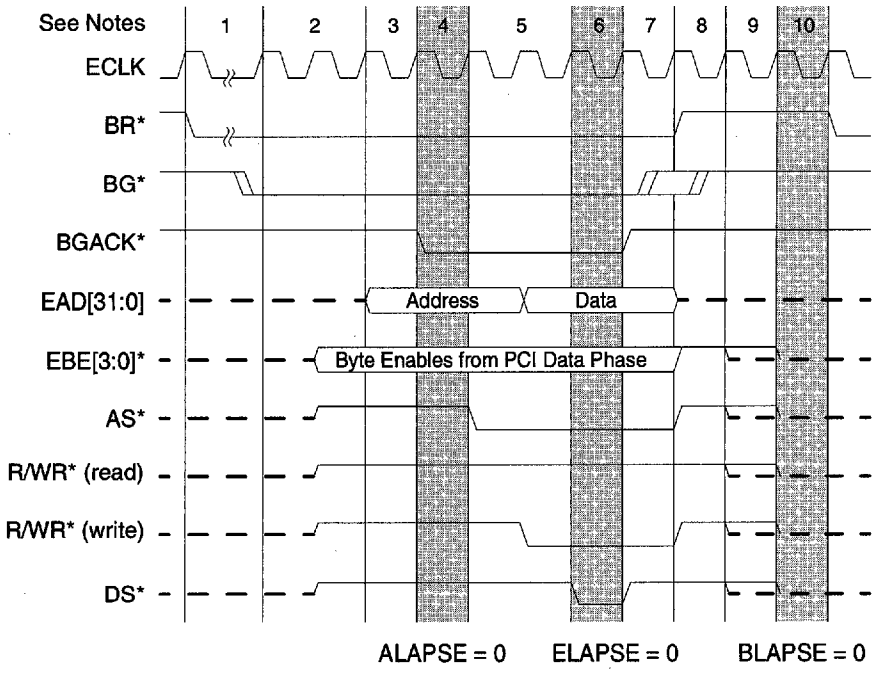
Figure 7-12. EBUS Write/Read Transactions, Intel-Style



NOTE(S):

1. HLDA assertion depends on the external bus arbiter. While HOLD and HLDA are both deasserted, MUSYCC places shared EBUS signals in high impedance (tri-state, shown as dashed lines).
2. One ECLK cycle after HLDA assertion, MUSYCC outputs valid command bus signals: EBE, ALE, RD* and WR*.
3. Two ECLK cycles after HLDA assertion, MUSYCC outputs valid EAD address signals.
4. ALE assertion occurs 3 ECLK cycles after HOLD and HLDA are both asserted.ALAPSE inserts a variable number of ECLK cycles to extend ALE high pulse width and EAD address interval.
5. EAD address remains valid for one ECLK cycle after ALE falling edge. During a write transaction, MUSYCC outputs valid EAD write data one ECLK prior to WR* assertion. During a read transaction, EAD data lines are inputs.
6. ELAPSE inserts a variable number of ECLK cycles to extend RD*/WR* low pulse width and EAD data intervals. Read data inputs are sampled on ECLK rising edge coincident with RD* deassertion.
7. EAD write data and EBE byte enables remain valid for one ECLK cycle after RD*/WR* deassertion.
8. One ECLK after RD* or WR* deassertion, HOLD is deasserted and the bus is parked (command bus deasserted, EAD tristate). The bus parked state ends when HLDA is deasserted.
9. Command bus is unparked (tri-stated) one ECLK after HLDA deassertion; two different unpark phases are shown, indicating the dependence on HLDA deassertion. If HLDA remained asserted until the next bus request, then command bus remains parked until one ECLK cycle following the next HOLD assertion. Warning: Whenever HLDA is deasserted, all shared EBUS signals are forced to tri-state after one ECLK cycle, regardless of whether the EBUS transaction was completed. MUSYCC won't reissue or repeat such an aborted transaction.
10. BLAPSE inserts a variable number of ECLK cycles to extend HOLD deassertion interval until the next bus request.

Figure 7-13. EBUS Write/Read Transactions, Motorola-Style



NOTE(S):

1. BG* assertion depends on the external bus arbiter. While BG* and BR* are both deasserted, MUSYCC places shared EBUS signals in high impedance (tri-state, shown as dashed lines).
2. One ECLK cycle after BG* assertion, MUSYCC outputs valid command bus signals: EBE, AS*, R/WR* and DS*.
3. Two ECLK cycles after BG* assertion, MUSYCC outputs valid EAD address signals. BGACK* assertion occurs three ECLK cycles after BG* and BR* are both asserted.
4. ALAPSE inserts a variable number of ECLK cycles to extend AS* high pulse width and EAD address interval.
5. EAD address remains valid for one ECLK cycle after AS* falling edge. During a write transaction, MUSYCC asserts R/WR* and outputs valid EAD write data one ECLK prior to DS* assertion. During a read transaction, EAD data lines are inputs.
6. ELAPSE inserts a variable number of ECLK cycles to extend DS* low pulse width and EAD data interval. Read data inputs are sampled on ECLK rising edge coincident with DS* deassertion.
7. EAD write data, EBE, R/WR* and AS* signals remain valid for one ECLK cycle after BGACK* and DS* are deasserted.
8. One ECLK cycle after BGACK* deassertion, the BR* output is deasserted and the bus is parked (command bus deasserted, EAD tristate). The bus parked state ends when the external bus arbiter deasserts BG*.
9. Command bus is unparked (tri-stated) one ECLK after BG* deassertion; two different unpark phases are shown, indicating the dependence on BG* deassertion. If BG* remained asserted until the next bus request, then command bus remains parked until one ECLK following the next BR* assertion. Warning: Whenever BG* is deasserted, all shared EBUS signals are forced to tri-state after one ECLK cycle, regardless of whether the EBUS transaction was completed. MUSYCC won't reissue or repeat such an aborted transaction.
10. BLAPSE inserts a variable number of ECLK cycles to extend BR* deassertion interval until the next bus request.

7.2.5 Serial Interface Timing and Switching Characteristics

Serial interface timing and switching characteristics are displayed in Tables 7-12 through 7-14 and Figures 7-14 through 7-16.

Table 7-12. Serial Interface Clock (RCLK, TCLK) Parameters

Symbol	Parameter	Min	Max	Units
F_c	Clock Frequency	DC	8.192 ±10%	MHz
T_r	Clock Rise Time	–	2	ns
T_f	Clock Fall Time	–	2	ns

Figure 7-14. Serial Interface Clock (RCLK,TCLK) Waveform

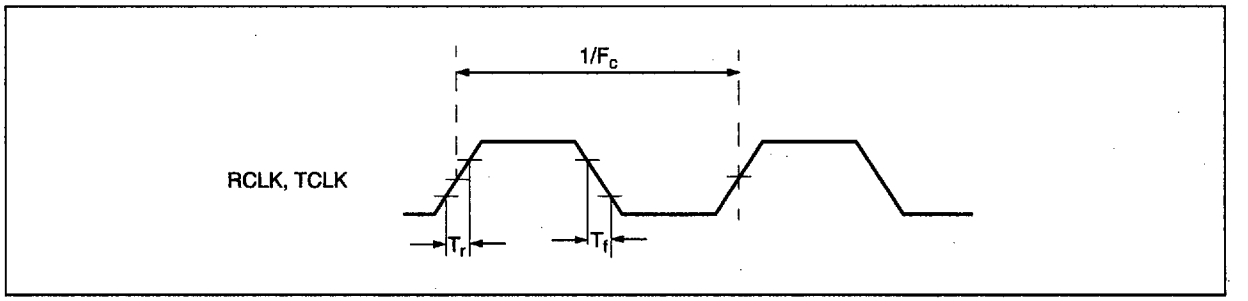


Table 7-13. Serial Interface Input/Output Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{val}	Clock to Signal Valid Delay	2	17	ns
T_{ds}	Data Setup Time	10	–	ns
T_{dh}	Data Hold Time	10	–	ns

Table 7-14. Serial Interface Input/Output Measure Conditions

Symbol	Parameter	Value	Units
V_{th}	Voltage Threshold High(1)	2.4	V
V_{tl}	Voltage Threshold Low(1)	0.4	V
V_{test}	Voltage Test Point	1.5	V
V_{max}	Maximum Peak-to-Peak(2)	2.0(3)	V
–	Input Signal Edge Rate	1	V/ns

NOTE(S):
(1) The input test for the 5 V environment is done with 400 mV of overdrive (over V_{ih} and V_{il}). Timing parameters must be met with no more overdrive than this. Production testing may use different voltage values, but must correlate results back to these parameters.
(2) V_{max} specifies the maximum peak-to-peak voltage waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.
(3) For TCLK, the value changes from 2.0 V to 2.5 V.

Figure 7-15. Serial Interface Data Input Waveform

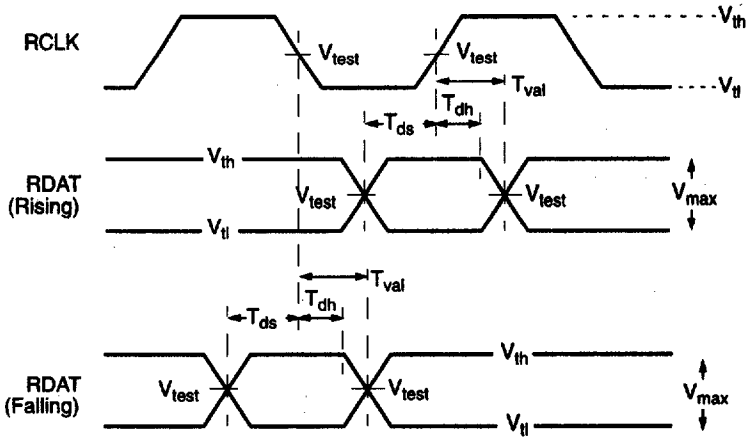
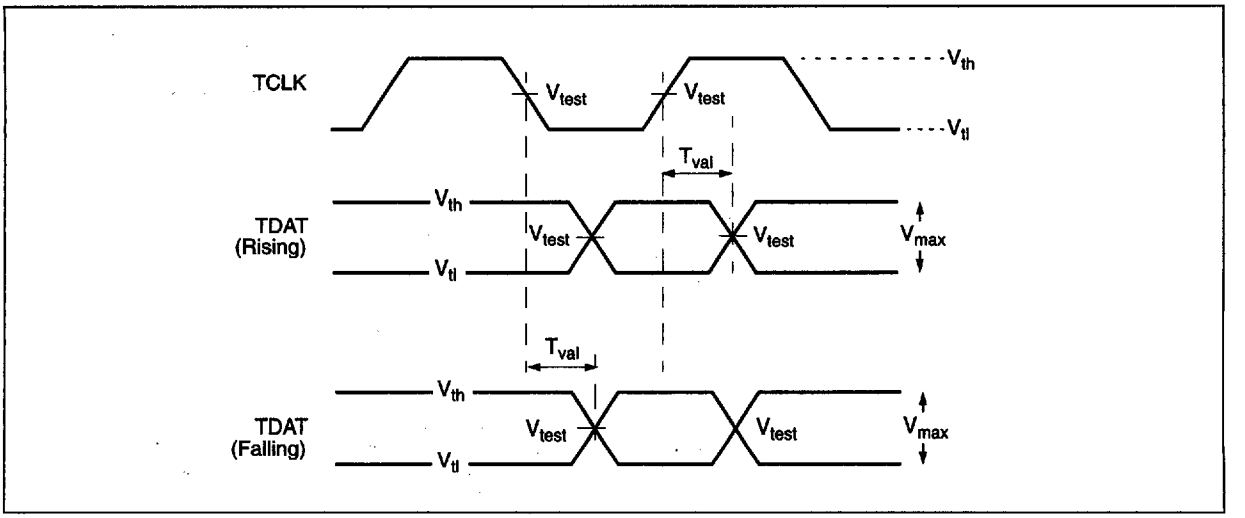


Figure 7-16. Serial Interface Data Delay Output Waveform



7.2.6 Test and Diagnostic Interface Timing

Test and diagnostic interface timing characteristics are displayed in Tables 7-15 and 7-16, as well as Figure 7-17.

Table 7-15. Test and Diagnostic Interface Timing Requirements

Symbol	Parameter	Minimum	Maximum	Unit
1	TCK Pulse-Width High	80	—	ns
2	TCK Pulse-Width Low	80	—	ns
3	TMS, TDI Setup Prior to TCK Rising Edge(1)	20	—	ns
4	TMS, TDI Hold after TCK High(1)	20	—	ns

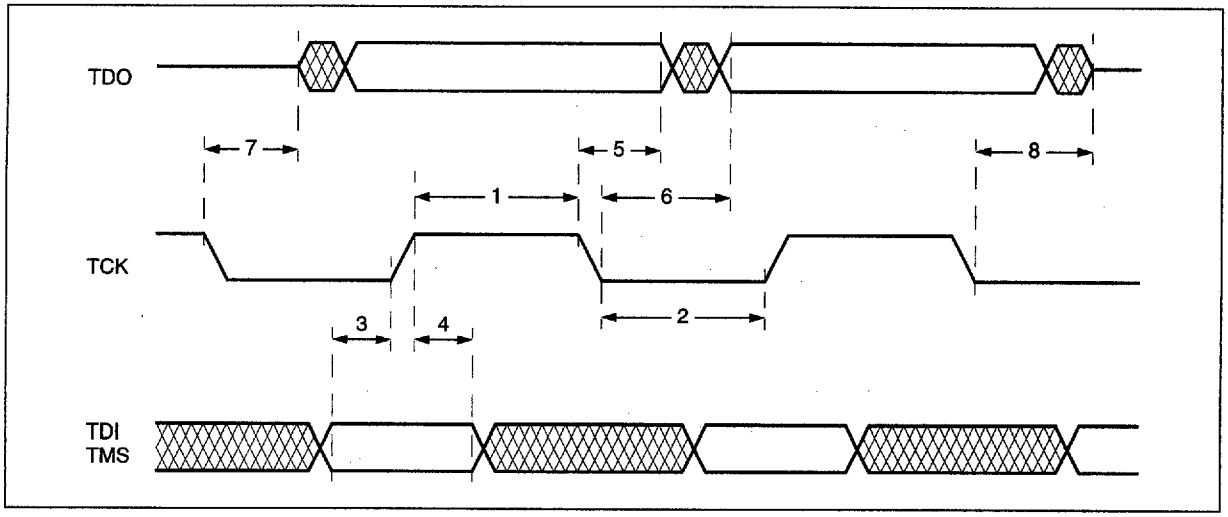
NOTE(S):
(1) Also applies to functional inputs for SAMPLE/PRELOAD and EXTEST instructions.

Table 7-16. Test and Diagnostic Interface Switching Characteristics

Symbol	Parameter	Minimum	Maximum	Unit
5	TDO Hold after TCK Falling Edge(1)	0	—	ns
6	TDO Delay after TCK Low(1)	—	50	ns
7	TDO Enable (Low Z) after TCK Falling Edge(1)	2	—	ns
8	TDO Disable (High Z) after TCK Low(1)	—	25	ns

NOTE(S):
(1) Also applies to functional outputs for the EXTEST instruction.

Figure 7-17. JTAG Interface Timing



7.2.7 Package Thermal Specification

Table 7-17 displays the package thermal specifications.

Table 7-17. MUSYCC 160-Pin PQFP Package Thermal Resistance Characteristics

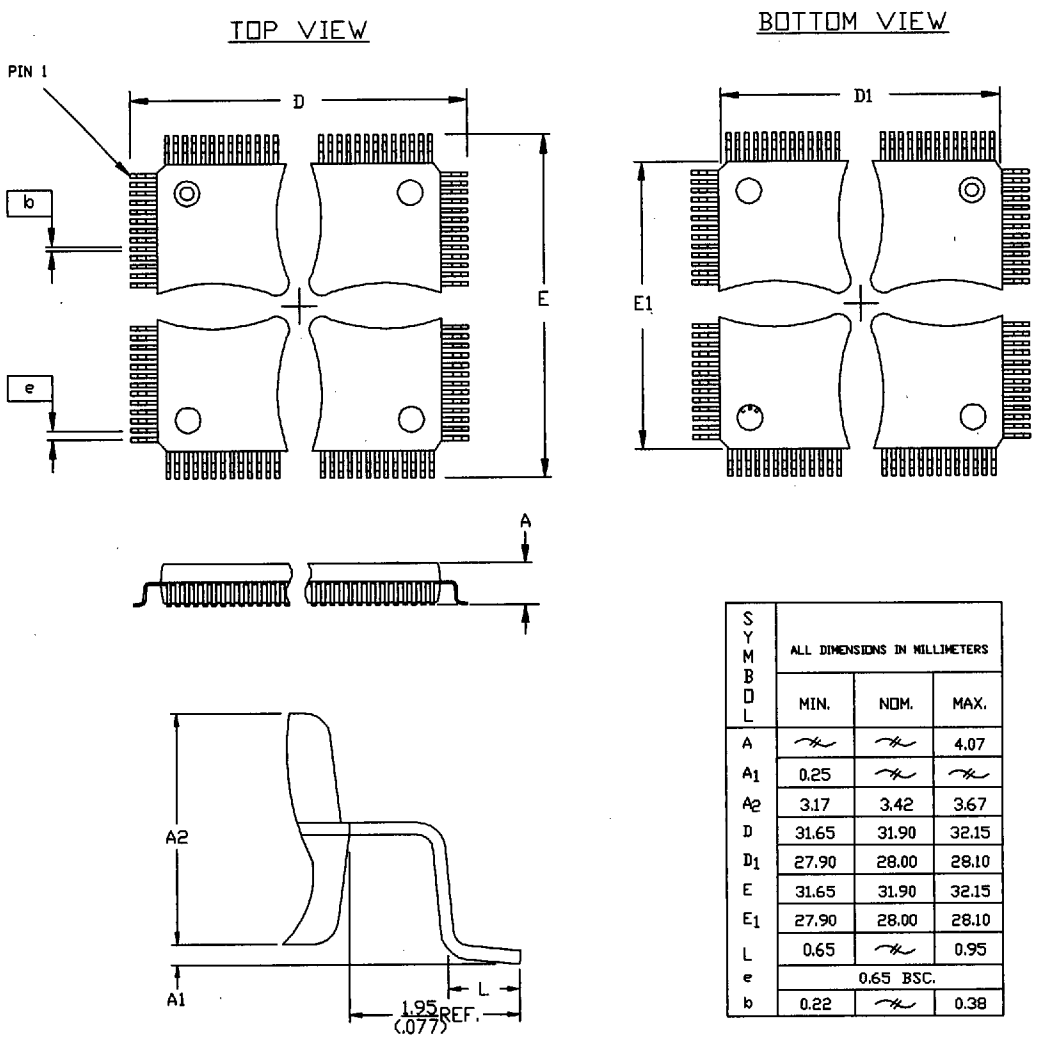
PQFP Package	Mounting Conditions	Airflow–LFM (LMS)				
		0 (0.000)	50 (0.256)	100 (0.505)	200 (1.01)	400 (2.03)
Thermal Resistance (junction to ambient) = **C/W						
Standard	Surface–Board	28	26	25	23	21
Standard	Socket	36	35	33	30	25

NOTE(S):
1. LFM–linear feet per minute.
2. LMS–linear meters per second.
3. Junction to case temperature (°C): $T_{jc} = T_{ac} + (\theta_{ja} \times P_d)$.
   Tjc = θja x Pd(measured) + Tac(measured)
   Where:Tjc = Junction Temperature (see Table 7-1).
   θja = Thermal Resistance (θ-ja, see Table 7-17).
   Tac = Ambient Case Temperature (see Table 7-2).
   Pd = Power Dissipation = Vdd x Idd (Table 7-1).

7.2.8 Mechanical Specifications

Figure 7-18 shows the mechanical specifications.

Figure 7-18. 160-Pin PQFP Package Mechanical Drawing



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A			4.07
A_1	0.25		
A_2	3.17	3.42	3.67
D	31.65	31.90	32.15
D_1	27.90	28.00	28.10
E	31.65	31.90	32.15
E_1	27.90	28.00	28.10
L	0.65		0.95
e	0.65 BSC.		
b	0.22		0.38

7.3 Revision History

Table 7-18. Bt8474/2 Datasheet Revisions

Revision	Date	Change	Description
Rev. A	01/10/97		Initial Release
Rev. B	09/ /98		Includes updates to Rev. A and Errata 1.