PRELIMINARY

GSS

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An Introduction to SUNTAC Super286 CHIP SET*

FEATURES:

- Fully IBM PC/AT compatible .
- Supports 16MHz and 20MHz operations.
- 4-way page-interleaved memory operation; Supports up to 8MB on-board memory.
- 57 modes of memory mapping configuration.
- Supports DRAM access time ranging from 150ns to 70ns with 16 various timing combinations.
- Flexible and efficient shadow RAM implementation.
- Supports LIM EMS 4.0 and EEMS (Enhanced EMS).
- Independent 8284 clock circuitry to optimize the 80287 operation.
- 6 modes of selectable wait state ranging from 1.3 to 0.6 wait state.
- Supports 8-bit/16-bit BIOS PROM.
- Synchronous and asynchronous AT bus clock options.
- Register setting by either hardware switch or software setup without BIOS modification.
- Quick reset and gate A20 control for OS/2 optimization.
- High level integration.
- Advanced 1.2μm CMOS technology (ST62C201 and ST62C202) provides high speed operation with minimal power consumption.

* For detailed technical information, please refer to SUNTAC Super286 Chip Set Specifications and Technical Manual.

SUNTAC Super286 CHIP SET

DESCRIPTION:

The SUNTAC Super286 chip set is designed for use in 16 to 20 MHz 80286 based systems and provides complete support for the IBM PC/AT bus architecture. Its high level integration design provides the standard IBM PC/AT motherboard functions with only 25 ICs plus memory devices.

The SUNTAC Super286 chip set provides a 4-bank, 4-way interleaved memory sub-system with page mode operation. It supports up to 8MB of on-board memory and a total of 57 modes of memory mapping. The using of 256Kbit and 1Mbit DRAM in each memory bank can be arbitrarily mixed; for example, one bank of 1Mbit DRAM plus two banks of 256Kbit DRAM can be used to provide a total of 3MB memory for running the DOS compatible box of OS/2. Special design is incorporated in the Super286 chip set to allow a 5 to 15 percent enhancement in DRAM efficiency. For instance, 100ns DRAM can be used for both 16MHz and 20 MHz operation with 0.5 and 0.65 wait state, respectively.

The LIM EMS version 4.0 is fully supported by the EMS registers built into the SUNTAC Super286 chip set. With an external SRAM, this EMS can be further enhanced to EEMS with 512 EMS mapper registers (8 sets of 64 page frames) to perform faster data swapping in multi-user applications. Unlike chip sets offered by other vendors, the entire real mode 1MB address space can be defined as the EMS window.

The memory sub-system provided by the Super286 chip set is efficient and flexible; either 640KB or 512KB can be used as the base memory, and the remaining DRAM and be used as extended memory, EMS memory, BIOS shadow RAM, and video shadow RAM. For example, when 1MB memory is available with 640KB base memory, 96KB can be used as the BIOS shadow RAM and 32KB can be used as the video shadow RAM (the BIOS shadow RAM is 32KB per step and the video shadow RAM is 16KB per step). The remaining 256KB can be configured as conventional extended memory or 16 pages of EMS memory, or as 64KB extended memory with 12 pages of EMS memory.

Both synchronous and asynchronous AT bus operations are provided for efficiency and compatibility purposes. The CPU clock can be selected from the high speed clock or AT bus clock by either hardware switch or software programming. The wait state of the BIOS PROM are automatically adjusted; a 250ns PROM can be used in 20MHz configuration.

The SUNTAC Super286 chip set supports both 8-bit and 16-bit PROM. The 8-bit mode operation not only reduces the board space but also reduces cost and inventory. With the BIOS shadow RAM enabled, the 8-bit mode of operation is faster than the 16-bit mode operation.

An independent 8284 clock circuitry is included to allow an 80287 co-processor running at CLKM = 1 mode. The performance enhancement of CLKM = 1 mode is more than 20 percent faster than the normal CLKM = 0 mode.

The SUNTAC Super286 chip set provides quick reset and gate A20 functions to allow fast switching between protected and real modes for OS/2 optimization instead of using keyboard controller. The memory and bus operations may be selected by hardware design options using DIP switches without any BIOS modification. One the other hand, this chip set can be implemented into a motherboard without DIP switches, in this case, the memory and bus options are software configured.

The SUNTAC Super286 chip set includes five (5) CMOS chips:

ST62C201: System bus controller with asynchronous AT bus clock; 100-pin flat package.

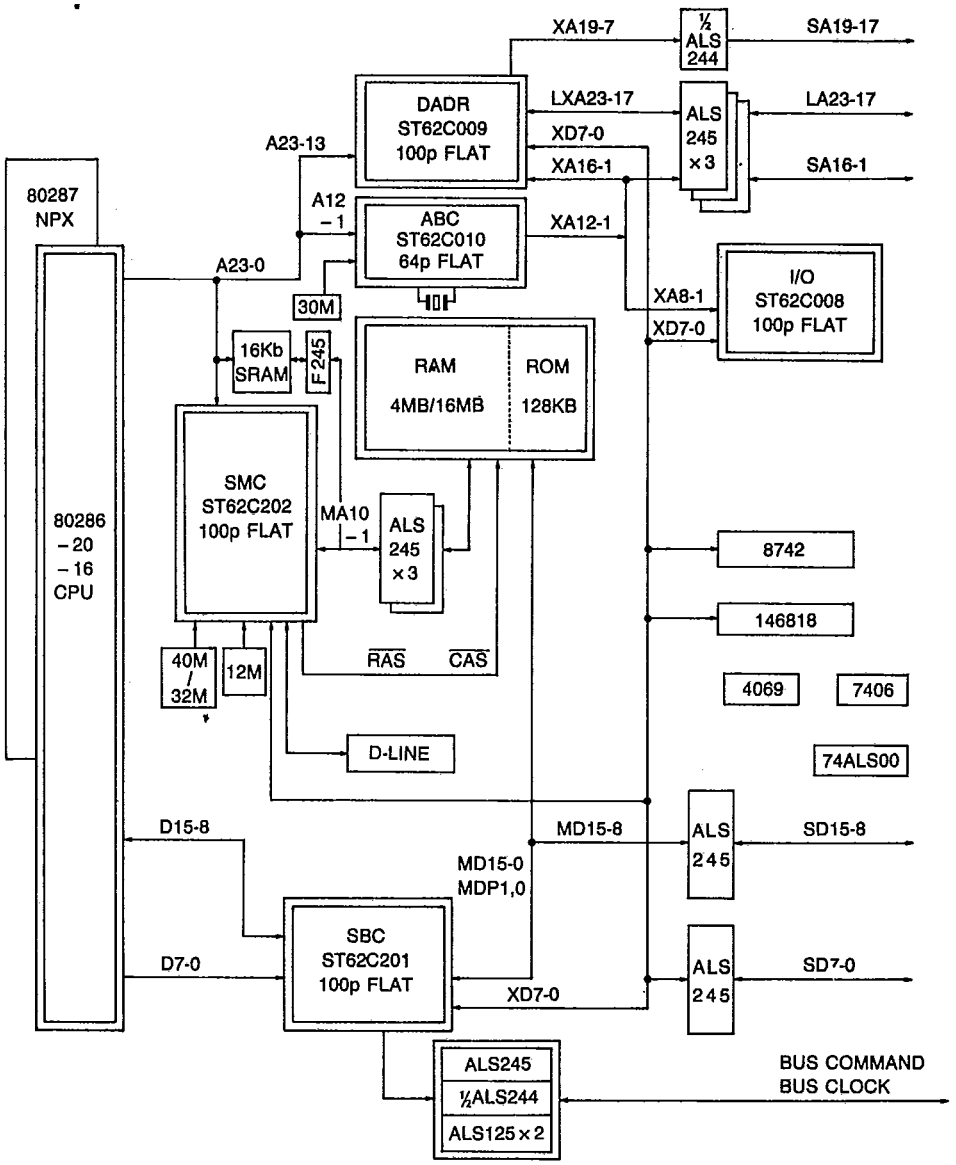
ST62C202: System controller with page interleaved memory controller and EMS memory mapper; 100-pin flat package.

ST62C008: Integrated peripheral controller; 100-pin flat package.

ST62C009: DMA address controller; 100-pin flat package.

ST62C010: Address bus controller; 64-pin flat package.

SUNTAC Super286
SYSTEM BLOCK DIAGRAM



SUNTAC Super286 CHIP SET

System Memory Configuration

Total System Memory	DRAM Type				Interleave
	Bank 0	Bandk 1	Bnak 2	Bank 3	
512KB	256K	0K	0K	0K	No
1MB	256K	256K	0K	0K	2 way
2MB	256K	256K	256K	256K	4 way
3MB	256K	256K	1M	0K	2 way/No
5MB	256K	256K	1M	1M	2 way
2MB	1M	0K	0K	0K	No
4MB	1M	1M	0K	0K	2 way
8MB	1M	1M	1M	1M	4 way

Examples of Various Memory Mapping for 1MB System RAM

Memory Name	Memory Mapping Mode							
	0	1	2	3	4	5	6	7
Base Memory	640K	640K	512K	512K	640K	640K	512K	512K
Extended Memory	384K	256K	512K	384K	64K	---	64K	---
Shadow RAM (max)	---	128K	---	128K	128K	128K	128K	128K
EMS (16K/page)	---	---	---	---	12page	16page	20page	24page

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SUNTAC Super286 CHIP SET

Modes of DRAM Access Time Selection

DRAM Access Time	System Speed			
	25MHz*	20MHz	16MHz	12MHz
150 ns	---	---	3	6
120 ns	---	---	6	7
100 ns	---	4	7	1
80 ns	---	6	1	0
70 ns	4	7	1	0
60 ns	6	7	0	0
FP 120 ns**		3	6	1
FP 100 ns	2	4	7	1
FP 80 ns	3	6	1	0

* For reference only.
** FP = Fast page mode

Average Wait State Reference Table*

Mode Number	Interleave		
	No	2 Way	4 Way
0	0.58	0.28	0.10
1	0.76	0.45	0.18
7	0.84	0.54	0.30
6 or 5	0.98	0.64	0.37
4	1.12	0.78	0.46
3	1.36	0.88	0.54
2	N/A	N/A	N/A

* All wait states are simulated results from Power Meter Aggregate System Test Program.

ADDITIONAL CIRCUIT FOR EEMS OPTIONAL FUNCTION (512 Mapper Registers)