



28C04A

4K (512 x 8) CMOS EEPROM

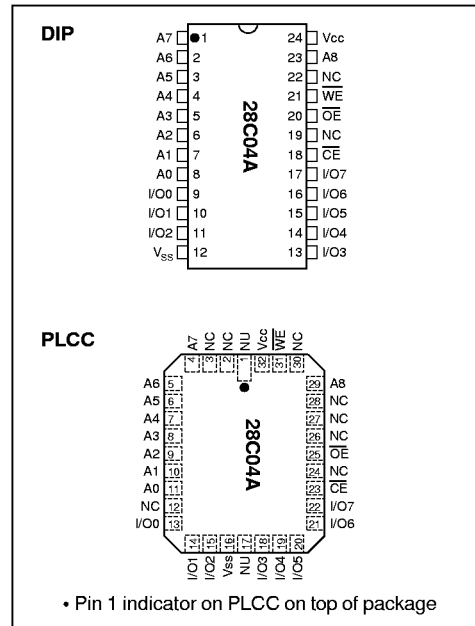
FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
 - 30 mA Active
 - 100 μ A Standby
- Fast Byte Write Time—200 μ s or 1 ms
- Data Retention >200 years
- Endurance - Minimum 10^4 Erase/Write Cycles
 - Automatic Write Operation
 - Internal Control Timer
 - Auto-Clear Before Write Operation
 - On-Chip Address and Data Latches
- Data Polling
- Chip Clear Operation
- Enhanced Data Protection
 - VCC Detector
 - Pulse Filter
 - Write Inhibit
- 5-Volt-Only Operation
- Organized 512x8 JEDEC standard pinout
 - 24-pin Dual-In-Line Package
 - 32-pin PLCC Package
- Available for Extended Temperature Ranges:
 - Commercial: 0°C to +70°C
 - Industrial: -40°C to +85°C

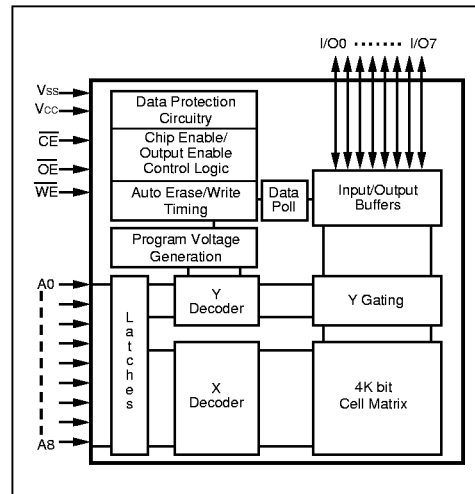
DESCRIPTION

The Microchip Technology Inc. 28C04A is a CMOS 4K non-volatile electrically Erasable and Programmable Read Only Memory (EEPROM). The 28C04A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C04A uses Data polling. Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPES



BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

V_{CC} and input voltages w.r.t. V_{SS}..... -0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. V_{SS} -0.6V to +13.5V
Output Voltage w.r.t. V_{SS}..... -0.6V to V_{CC}+0.6V
Storage temperature -65°C to +125°C
Ambient temp. with power applied..... -50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A8	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
V _{CC}	+5V Power Supply
V _{SS}	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

V _{CC} = +5V ±10% Commercial (C): T _{amb} = 0°C to +70°C Industrial (I): T _{amb} = -40°C to +85°C						
Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic '1' Logic '0'	V _{IH} V _{IL}	2.0 -0.1	V _{CC} +1 0.8	V V	
Input Leakage		I _{LI}	-10	10	μA	V _{IN} = -0.1V to V _{CC} +1
Input Capacitance		C _{IN}		10	pF	V _{IN} = 0V; T _{amb} = 25°C; f = 1 MHz
Output Voltages	Logic '1' Logic '0'	V _{OH} V _{OL}	2.4	0.45	V V	I _{OH} = -400 μA I _{OL} = 2.1 mA
Output Leakage		I _{LO}	-10	10	μA	V _{OUT} = -0.1V to V _{CC} + 0.1V
Output Capacitance		C _{OUT}		12	pF	V _{IN} = 0V; T _{AMB} = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	I _{CC}		30	mA	f = 5 MHz (Note 1) V _{CC} = 5.5V
Power Supply Current, Standby	TTL input TTL input CMOS input	I _{CC} (S) _{TTL} I _{CC} (S) _{TTL} I _{CC} (S) _{CMOS}		2 3 100	mA mA μA	$\overline{CE}$ = V _{IH} (0°C to +70°C) $\overline{CE}$ = V _{IH} (-40°C to +85°C) $\overline{CE}$ = V _{CC} -0.3 to V _{CC} +1 $\overline{OE}$ = V _{CC} All inputs equal V _{CC} or V _{SS}

Note 1: AC power supply current above 5 MHz; 1 mA/MHz.

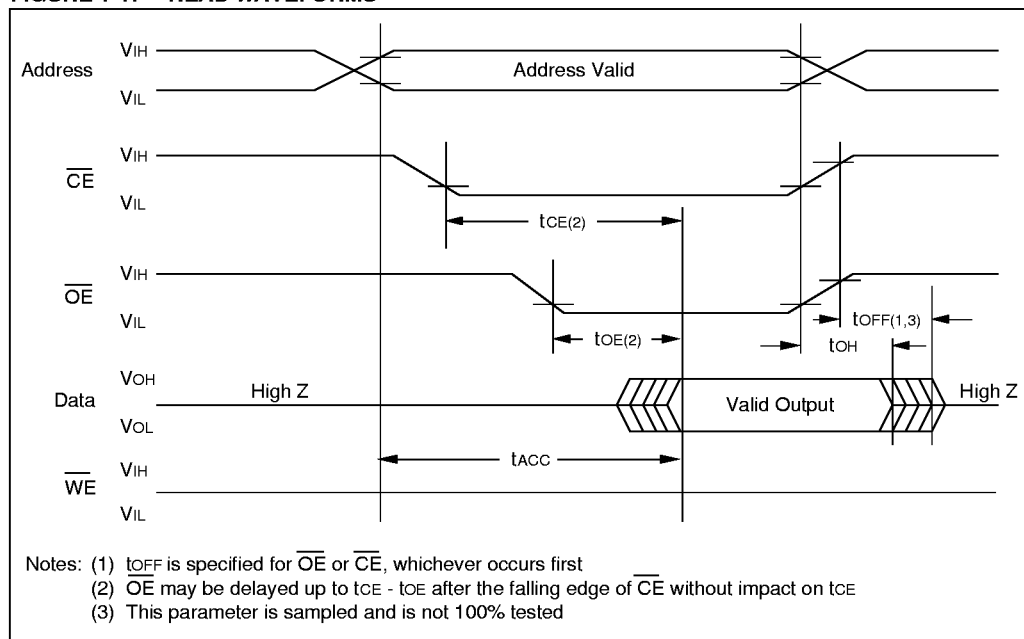
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TABLE 1-3: READ OPERATION AC CHARACTERISTICS

		AC Testing Waveform:		$V_{IH} = 2.4V$; $V_{IL} = 0.45V$; $V_{OH} = 2.0V$; $V_{OL} = 0.8V$					
		Output Load:		1 TTL Load + 100 pF					
		Input Rise and Fall Times:		20 ns					
		Ambient Temperature:		Commercial (C): $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ Industrial (I): $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$					
Parameter	Sym	28C04A-15		28C04A-20		28C04A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE} = \overline{CE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE} = V_{IL}$
$\overline{CE}$ to $\overline{OE}$ High Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0		0		0		ns	
Endurance	—	1M	—	1M	—	1M	—	cycles	$25^{\circ}C$, $V_{CC} = 5.0V$, Block Mode (Note)

Note: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



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TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

		AC Testing Waveform:		VIH = 2.4V; VIL = 0.45V; VOH = 2.0V; VOL = 0.8V	
		Output Load:		1 TTL Load + 100 pF	
		Input Rise/Fall Times:		20 nsec	
		Ambient Temperature:		Commercial (C): Tamb= 0°C to 70°C	
				Industrial (I): Tamb= -40°C to 85°C	
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	tAS	10		ns	
Address Hold Time	tAH	50		ns	
Data Set-Up Time	tDS	50		ns	
Data Hold Time	tDH	10		ns	
Write Pulse Width	twPL	100		ns	Note 1
Write Pulse High Time	twPH	50		ns	
$\overline{OE}$ Hold Time	toEH	10		ns	
$\overline{OE}$ Set-Up Time	toES	10		ns	
Data Valid Time	tDV		1000	ns	Note 2
Write Cycle Time (28C04A)	twC		1	ms	0.5 ms typical
Write Cycle Time (28C04AF)	twC		200	μ s	100 μ s typical

- Note 1: A write cycle can be initiated by $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
- 2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until tDH after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

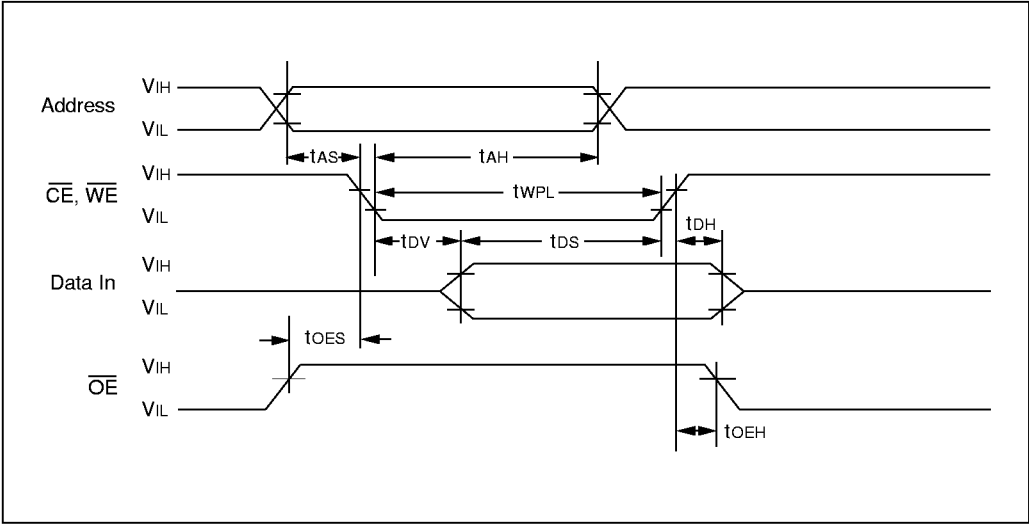


FIGURE 1-3: DATA POLLING WAVEFORMS

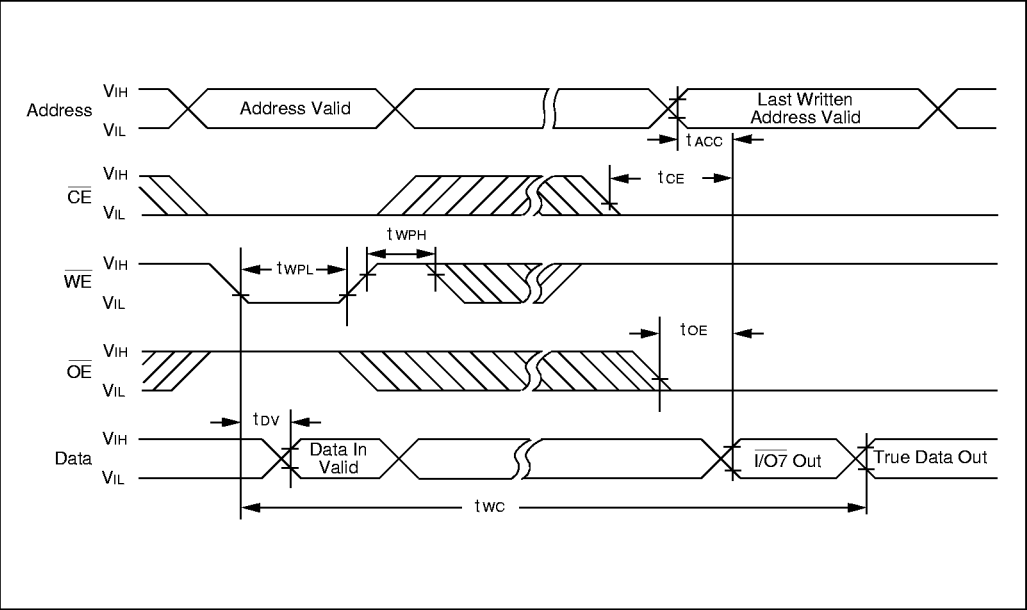
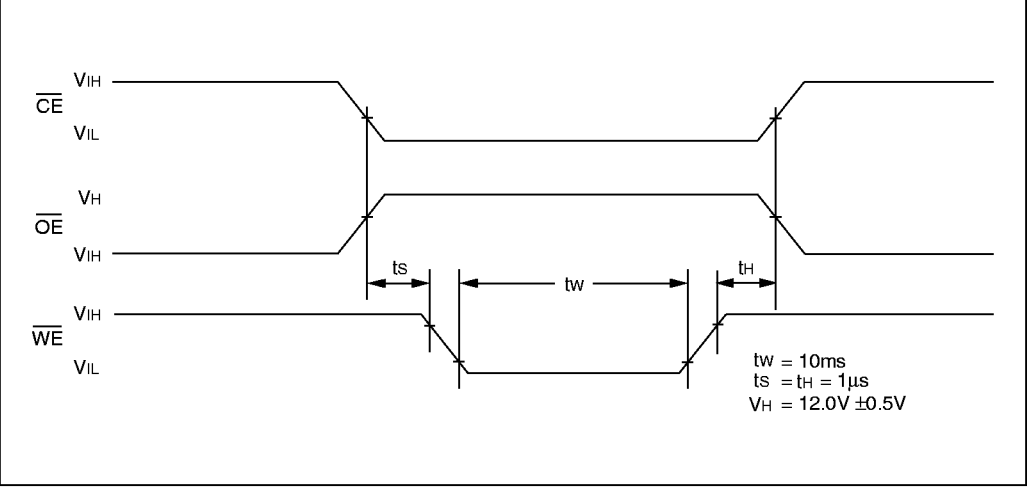


FIGURE 1-4: CHIP CLEAR WAVEFORMS



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2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C04A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{IE}$	$\overline{WE}$	I/O
Read	L	L	H	DO _{UT}
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DI _N
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

2.1 Read Mode

The 28C04A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

2.2 Standby Mode

The 28C04A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

2.4 Write Mode

The 28C04A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

2.5 Data Polling

The 28C04A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminate). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data.

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28C04A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

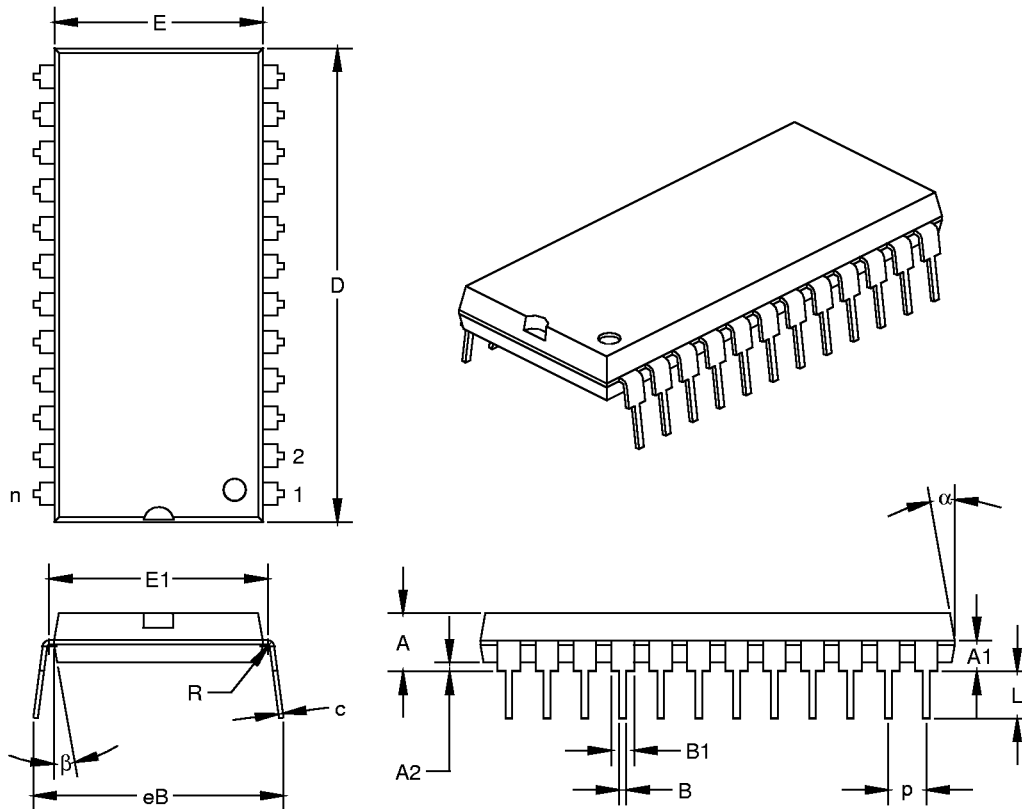
28C04A	F	T	-	15	I	/P	
							Package:
							L = Plastic Leaded Chip Carrier (PLCC) P = Plastic DIP (600mill)
							Temperature Range:
							Blank = 0°C to +70°C I = -40°C to +85°C
							Access Time:
							15 150 ns 20 200 ns 25 250 ns
							Shipping:
							Blank Tube T Tape and Reel "L" only
							Option:
							Blank = t _{wc} = 1ms F = t _{wc} = 200 μs
							Device:
							28C04A 512 x 8 CMOS EEPROM



MICROCHIP

Packaging Diagrams and Parameters

Package Type: K04-081 24-Lead Plastic Dual In-line (P) – 600 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		24			24	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.018	0.022	0.36	0.46	0.56
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.140	0.165	0.190	3.56	4.19	4.83
Top of Lead to Seating Plane	A1	0.064	0.084	0.104	1.61	2.12	2.63
Base to Seating Plane	A2	0.020	0.025	0.030	0.51	0.64	0.76
Tip to Seating Plane	L	0.115	0.125	0.135	2.92	3.18	3.43
Package Length	D‡	1.245	1.250	1.255	31.62	31.75	31.88
Molded Package Width	E‡	0.540	0.550	0.560	13.72	13.97	14.22
Radius to Radius Width	E1	0.562	0.577	0.592	14.27	14.66	15.04
Overall Row Spacing	eB	0.630	0.660	0.690	16.00	16.76	17.53
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

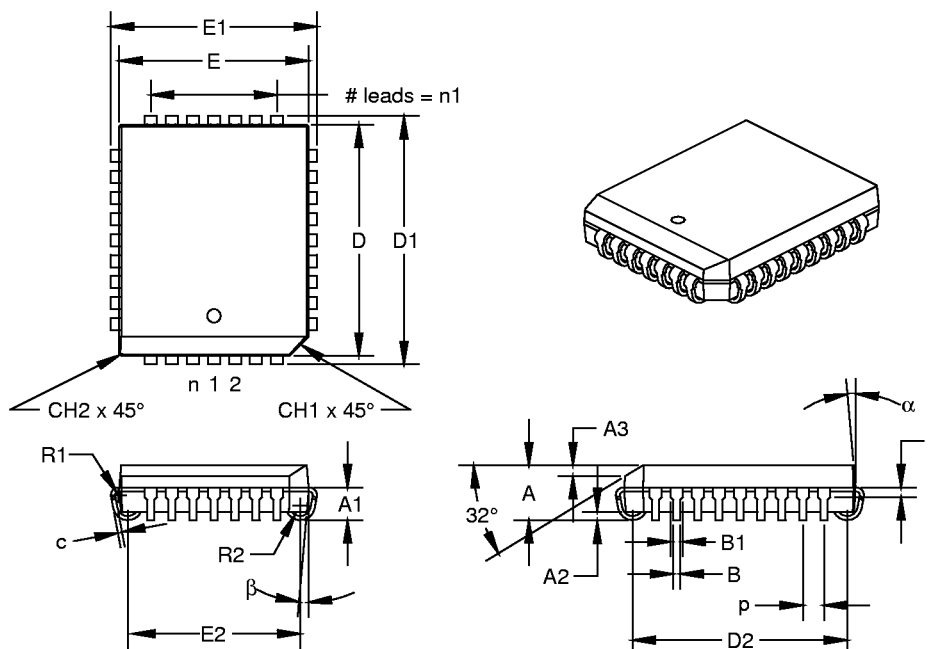
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-011 AA

Packaging Diagrams and Parameters

Package Type: K04-023 32-Lead Plastic Leaded Chip Carrier (L) – Rectangle



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		32			32	
Pitch	p		0.050			1.27	
Overall Pack. Height	A	0.127	0.131	0.135	3.23	3.33	3.43
Shoulder Height	A1	0.060	0.078	0.095	1.52	1.97	2.41
Standoff	A2	0.015	0.020	0.025	0.38	0.51	0.64
Side 1 Chamfer Dim.	A3	0.021	0.026	0.031	0.53	0.66	0.79
Corner Chamfer (1)	CH1	0.035	0.045	0.055	0.89	1.14	1.40
Corner Chamfer (other)	CH2	0.000	0.005	0.010	0.00	0.13	0.25
Overall Pack. Width	E1	0.485	0.490	0.495	12.32	12.45	12.57
Overall Pack. Length	D1	0.585	0.590	0.595	14.86	14.99	15.11
Molded Pack. Width	E [‡]	0.447	0.450	0.453	11.35	11.43	11.51
Molded Pack. Length	D [‡]	0.547	0.550	0.553	13.89	13.97	14.05
Footprint Width	E2	0.380	0.410	0.440	9.65	10.41	11.18
Footprint Length	D2	0.480	0.510	0.540	12.19	12.95	13.72
Pins along Width	n1		7			7	
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Upper Lead Width	B1 [†]	0.026	0.029	0.032	0.66	0.74	0.81
Lower Lead Width	B	0.013	0.017	0.021	0.33	0.43	0.53
Upper Lead Length	L	0.010	0.020	0.030	0.25	0.51	0.76
Shoulder Inside Radius	R1	0.003	0.008	0.013	0.08	0.20	0.33
J-Bend Inside Radius	R2	0.020	0.025	0.030	0.51	0.64	0.76
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-016 AE