REVISIONS							
SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP

June 24, 1985

PRELIMINARY CUSTOMER PROCUREMENT SPECIFICATION

28C16/28C17/28C291

16K

ELECTRICALLY ERASABLE PROM

6085

SHEET	1-14													
LAST REV	A													

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TITLE CPS FOR 16K (2Kx8) CMOS ELECTRICALLY ERASABLE PROM (28C16/28C17/28C291)

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED					
BY	R. Herber						
DATE	7-2-85						

SHEET 1 OF 14

SPEC. NO. 10163

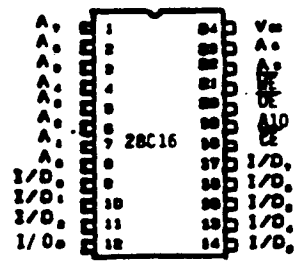
REV 7-2 A

SM 1E104 (3/81)

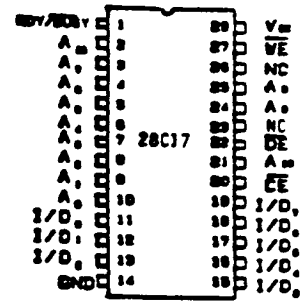
28C16/28C17/28C291
16K (2Kx8) CMOS ELECTRICALLY ERASABLE PROM

Features

- 5 Volt Only Operation
- High Performance/Reliability Double Metal CMOS Technology
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
- Ready/BUSY Open Drain (28C17 only)
- Data Polling
- Electronic Signature
  - Device Identification
  - Tracking
- On-Chip Address and Data Latches
- Direct Bipolar Prom Replacement (28C291)
- Optimal Chip Clear Function
- Low Power
  - 100uA Standby
  - 80mA Active
- Enhanced/Timed Data Protection Circuitry
- Data Retention > 10 years
- Endurance 10^4 Erase/Write Cycles per Byte
- Full Military & Extended Temperature Ranges
  - 0° to 70°C Commercial
  - -40° to 85°C Industrial
  - -55° to 125°C Military
- Extremely Fast 1mS Byte Write Time
- Ultra Fast Access Time
  - 28C16 -3.5 35nS max
  - 28C16 -10 100nS max
  - 28C16 -15 150nS max
  - 28C291-3.5 35nS max
- Chip Clear Operation
- JEDEC Approved Byte-Wide Pin Out



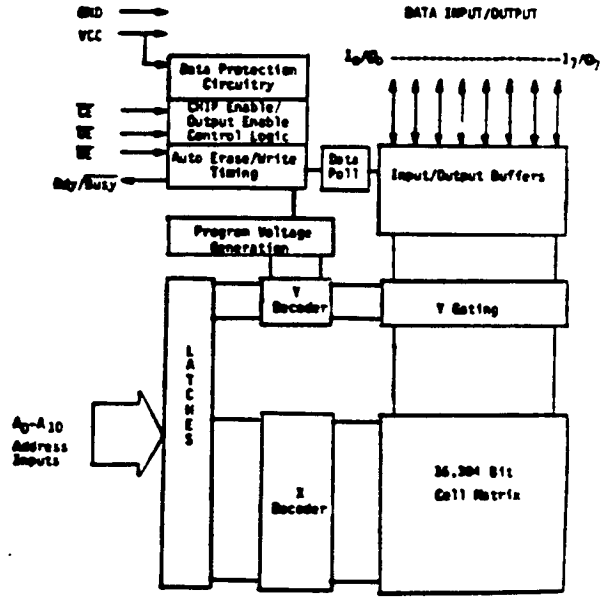
PIN CONFIGURATION
28C16



PIN CONFIGURATION
28C17

A_0 - A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_0 - I/O_7	DATA INPUTS/OUTPUTS
RDY/$\overline{BUSY}$	READY/$\overline{BUSY}$

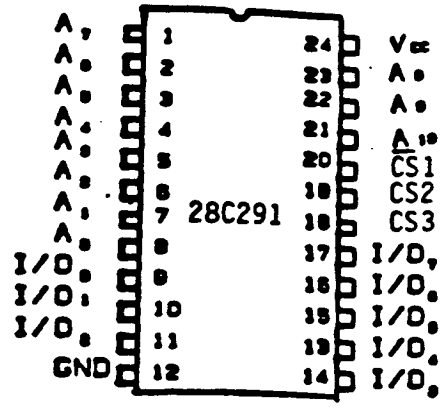
PIN NAMES



FUNCTIONAL BLOCK DIAGRAM
28C16/28C17/28C291

$A_0 - A_{10}$	ADDRESSES
$I/O_0 - I/O_7$	DATA INPUTS/OUTPUTS
$\overline{CS1}$, CS2, CS3	CHIP SELECTS

PIN NAMES



PIN CONFIGURATION
28C291

28C16/28C291

DESCRIPTION

The General Instrument 28C16, 28C17 and 28C291 are low power, high performance byte wide, 16,384 bit electricelly erasable, programmable, non-volatile read-only-memory devices. They are manufactured with General Instrument's advanced non-volatile CMOS technology. This device requires only a five-volt power supply for all modes of operation. An onboard DC to DC converter generates the internal VPP voltage necessary to perform the programming (erase/write) on the non-volatile memory elements.

Data, addresses, and input control signal are latched by the chip during programming, thus freeing the system to perform other functions. Byte writes are self-timed and include an automatic erase before write. All necessary programming voltages are internally generated and timed.

The fast-read access times (28C16/17-3.5 and 28C291-3.5) are compatible with high performance microprocessor applications. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using the Data polling mode. The Ready/Busy pin is an open drain output, allowing easy configuration in multiple systems. Alternatively, $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete.

An enhanced power-up/down protection system is included to ensure data integrity. To guard against inadvertent writes, especially during the critical power-up/down transistions, a VCC detect, input control (CE, OE, and WE) and an internal timer are used.

The 28C16 is upwards compatible to "Second Generation" 16KEE devices (i.e., Intel 2817, Xicor 2816, etc.) currently being developed/introduced.

DEVICE OPERATION

The General Instrument 28C16 has four basic modes of operation as outlined in the following table.

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13,15-19)	Rdy/$\overline{Busy}$ (1) Note 1
READ	L	L	H	Dout	H
STANDBY	H	X	X	High Z	H
WRITE INHIBIT	H	X	X	High Z	H
WRITE INHIBIT	X	L	X	-	H
WRITE INHIBIT	X	X	H	-	H
BYTE WRITE	L	H	L	Din	L
BYTE ERASE	Automatic Before Each "Write"				

Note 1: Open Drain Output - Pertains to 28C16 only

Read Mode

The General Instrument 28C16/28C17 and 28C291 have exceptionally fast access times that make it compatible with high performance microprocessor application. With tacc typically less than 35 nSec, its read cycle is similar to that of Eproms and static Rams.

In a microprocessor application, these devices can be read by applying a decoded system address signal to the $\overline{CE}$ input while using the uProcessor $\overline{RD}$ signal connected to the $\overline{OE}$ input.

The 28C16/28C17 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

DEVICE OPERATION- continued

Standby Mode

The 28C16/28C17 has a standby mode in which power consumption is reduced by 300 percent. This offers power supply benefits and reduced system bus noise. This mode is initiated when the device is deselected (CE = VIH). The data pins are put into the high impedance state regardless of the signals applied to the OE and WE - which may be left active for the reading and writing of other devices in the system.

Write Mode

When commanded to byte write, the 28C16/28C17 and 28C291 automatically latches the address, data and control signals, and starts the write. While in the write operation, the Ready/$\overline{\text{Busy}}$ open drain output is low. The data bus is not used by the 28C16/28C291 while writing, allowing the system to perform other tasks.

After the write cycle is initiated with the $\overline{\text{WE}}$ strobe pulse, the 28C16/28C17/28C291 completes the cycle off line in two transparent steps which are completely self-timed. First, the existing data at the addressed location is auto- matically erased. At the beginning of this step, the inputs are locked out, the data lines are brought to a high impedence state, and the Ready/ $\overline{\text{Busy}}$ signal is lowered to VOL. Second, the new data byte is written into the device. At the end of this write process, the Ready/$\overline{\text{Busy}}$ signal will be allowed to raise to VOH which may be used to notify the processor that the write cycle is complete and the device is ready for new read or write commands.

$\overline{\text{DATA}}$ POLLING

The 28C16/28C17 and 28C219 features $\overline{\text{Data}}$ Polling to signal the completion of a byte or page write cycle. During a write cycle, an attempted read of the last byte written results in the data compliment of that byte at I/O_7. After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

RETENTION/ENDURANCE

Read retention for data written into the 28C16/28C17 and 28C291 is greater than 10 years, with up to 10^4 write cycles. There is no limit to the number of times data may be read.

DATA PROTECTION

In order to insure data integrity, especially during critical power up and power down transitions, the following enhanced data protection circuits are incorporated.

An internal VCC detect (3.8 volts typical) will inhibit the initiation of a non-volatile programming operation when VCC is less than the VCC detect circuit trip. In addition, on power up an internal timer (1mSec) will inhibit the recognition of any program operation. During this period, all normal read functions will be operational. After both the VCC detection and the internal timer have expired, normal programming operation may be exercised.

There is a $\overline{\text{WE}}$ lockout circuit that prevents $\overline{\text{WE}}$ pulses of less that 20nS duration from initiating a write cycle.

Holding $\overline{\text{WE}}$ or $\overline{\text{CE}}$ high, or $\overline{\text{OE}}$ low, inhibits a write cycle during power-on and power-off (VCC).

OPTIONAL CHIP ERASE (Write)

All data may be written to "1"'s (erased) in a chip erase cycle by raising $\overline{\text{OE}}$ to 12 volts and bringing the $\overline{\text{WE}}$ low.

All "0"'s condition may be obtained by raising both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ to 12 volts and then bringing $\overline{\text{WE}}$ low.

PRODUCT AVAILABILITY BY TEMPERATURE RANGE

Temperature Range	28C16-3.5 28C17-3.5 28C291-3.5	28C16-10 28C17-10	28C16-15 28C17-15
0°C - +70°C	✓	✓	✓
-40°C - +85°C	Note 1	✓	✓
-55°C - +125°C	Note 2	✓	✓

Note 1: Tacc max 45nS
Note 2: Tacc max 55nS

Absolute Maximum Ratings - 28C16/28C17

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input Voltages with Respect to Ground	+6.25V to -0.6V
All Output Voltages with Respect to Ground	VCC+.6V to -.6V
Voltage on Pin 22 with Respect to Ground	+13.5V to -0.6V

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

TA = 0°C to 70°C, VCC = 5V±10%, unless otherwise specified.

Symbol	Parameter	Min	Max	Units	Conditions
ILI	Input Leakage Current		10	uA	-.1 to VCC + 1
ILO	Output Leakage Current		10	uA	-.1 to VCC + .1
ICC1	VCC Current Standby		100	uA	$\overline{CE}$=VCC+1 to VCC-.3
			2	mA	$\overline{CE}$=VIH (+12v)
ICC2	VCC Current Active		80	mA	f=20MHz
VIL	Input Low Voltge	-.1	+.8	V	
VIH	Input High Voltage	2.0	VCC+1V		
VOL	Output Low Voltage		.40	V	IOL=2.1mA
VOH	Output High Voltage	2.4		V	IOH=-400uA
VLKO	VCC Lockout Level for Data Protection	3.5	4.25	V	

Absolute Maximum Ratings - 28C291

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input Voltages with Respect to Ground	+6.25V to -0.6V
All Output Voltages with Respect to Ground	VCC+.6V to -.6V
Voltage on Pin 22 with Respect to Ground	+13.5V to -0.6V

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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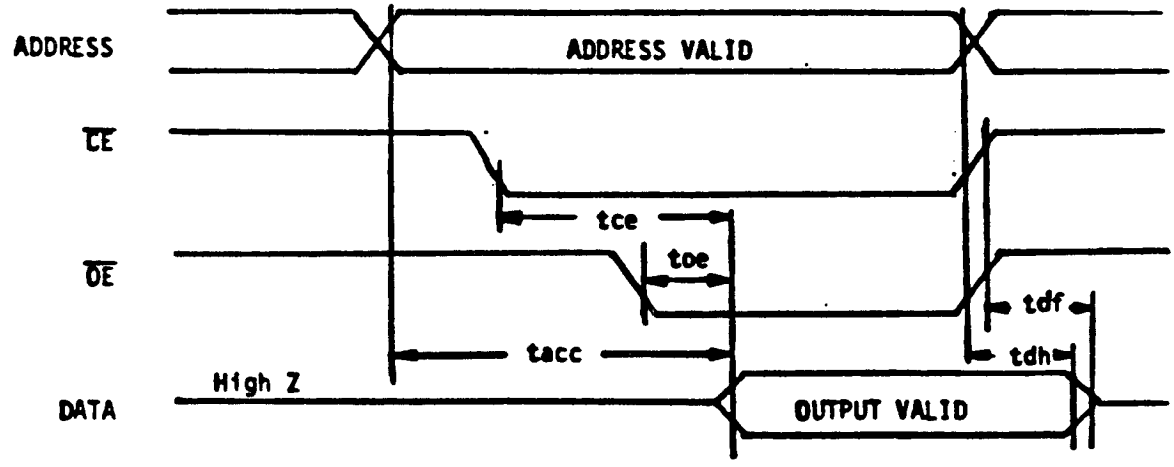
ILO	Output Leakage Current		10	uA	-.1 to VCC + .1
ICC1	VCC Current Standby		100	uA	$\overline{CE}$=VCC+1 to VCC-.3
			40	mA	$\overline{CE}$=VIH (+12v)
ICC2	VCC Current Active		80	mA	f=20MHz
VIL	Input Low Voltge	-.1	+.8	V	
VIH	Input High Voltage	2.0	VCC+1V		
VOL	Output Low Voltage		.40	V	IOL=2.1mA
VOH	Output High Voltage	2.4		V	IOH=-400uA
VLKO	VCC Lockout Level for Data Protection	3.5	4.25	V	

AC ELECTRICAL CHARACTERISTICS

Read Cycle 28C16/28C17

VCC = +5V ± 10% (unless otherwise specified)

Symbol	Parameter	28C16-3.5 28C291-3.5 Min	Max	28C16-10 Min	Max	28C16-15 Min	Max	Units	Test Conditions
tACC (2)	Address to Output Delay		35		100		55	nS	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay	35		100		150		nS	$\overline{OE}$=VIL
tWCE	$\overline{CE}$ Pulse Width	35		100		150		nS	$\overline{CE}$=$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		20		40		50	nS	$\overline{CE}$=VIL
tDF (1,3)	$\overline{OE}$ High to Output Float	0	20	0	40	0	50	nS	$\overline{CE}$=VIL
tDH	Output Hold from Address, CE or OE, whichever occurred first	0		0		0		nS	$\overline{CE}$=$\overline{OE}$=VIL



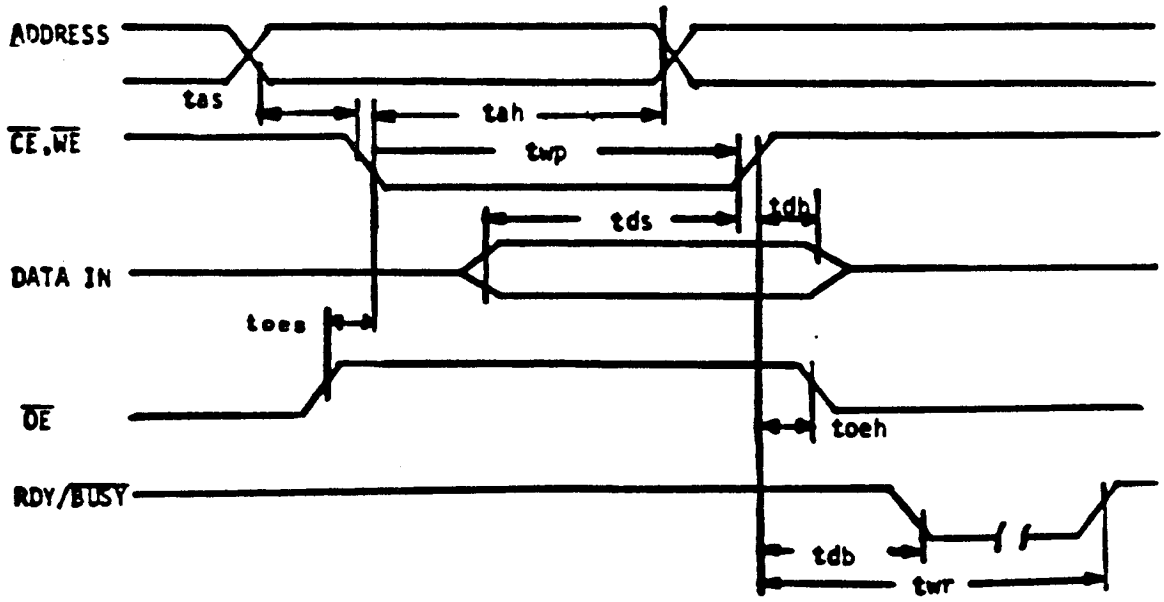
NOTES:
1. This parameter is only sampled and is not 100% tested.
2. OE may be delayed up to tACC-tOE after the falling edge of $\overline{CE}$ without impact on tACC.
3. tDF is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC ELECTRICAL CHARACTERISTICS

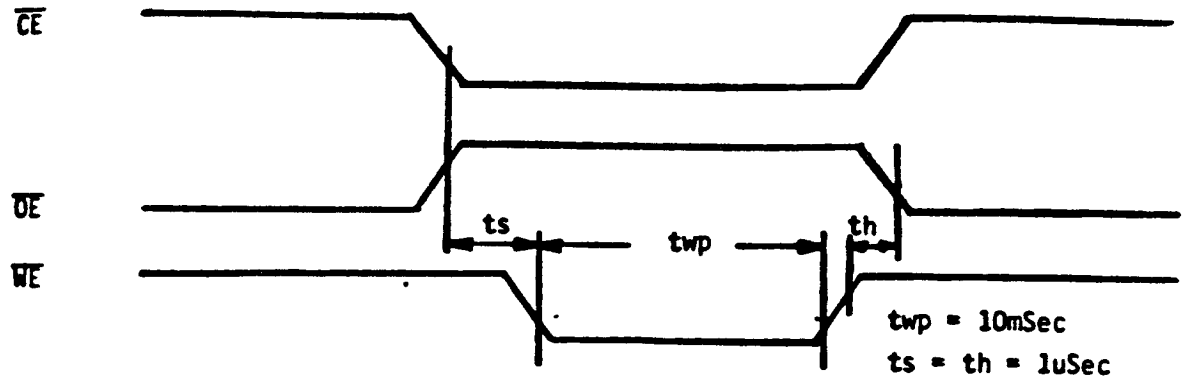
BYTE Write Cycle 28C16/28C17

TA = 0°C to 70°C, VCC = +5V ± 10% (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
tAS	Address, Setup Time	0			nS	
tAH	Address, Hold Time	25			nS	
tWP	Write Pulse Width	25		1000	nS	
tDS	Data Setup Time	25			nS	
tDH	Data Hold Time	0			nS	
tDB	Time to Device Busy			25	nS	
tWR	Write Cycle Time			1	mSec	
tOEH	$\overline{OE}$ Hold Time	20			nS	
tOES	$\overline{OE}$ Setup Time	20			nS	



CHIP ERASE WRITE 28C16/28C17



SUPPLEMENTARY CONTROL

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	Ai	VCC	Di - Oi (11-13,15-19)	RDY/$\overline{BUSY}$ (1)
Chip Erase	VIL	VH		X	VCC		
Extra Row Read	VIL	VIL	VIH	A9=VH	VCC	DOUT	
Extra Row Write		VIH		A9=VH	VCC	DIN	

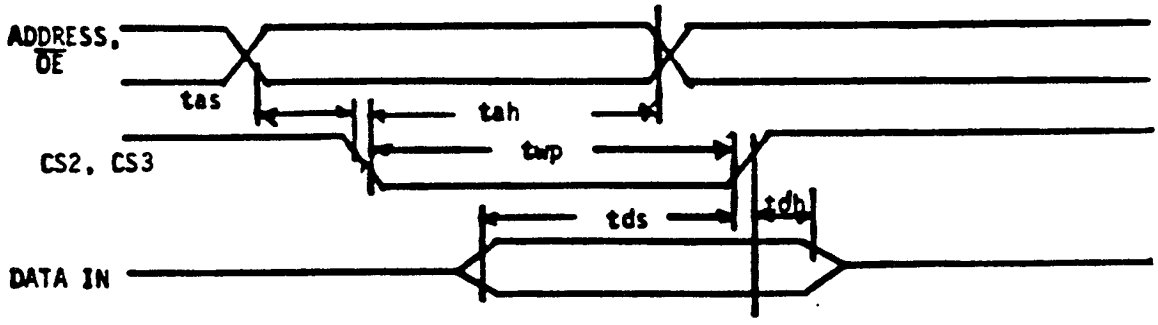
VH = 12.0 ± .5 volts

AC ELECTRICAL CHARACTERISTICS

BYTE Write Cycle 28C291

TA = 0°C to 70°C, VCC = +5V ± 10% (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
tAS	Address Setup Time	0			nS	
tAH,tOEH	Address Hold Time	40			nS	
tWP	Write Pulse Width	40		1000	nS	
tDS	Data Setup Time	40			nS	
tDH	Data Hold Time	0			nS	
tWR	Write Cycle Time			1	mSec	

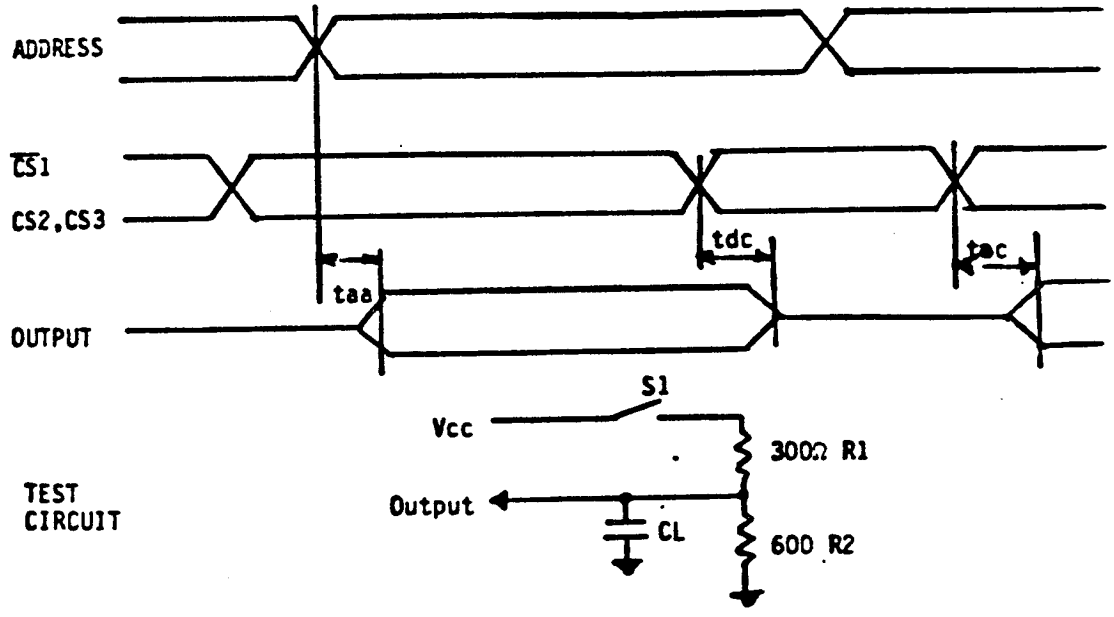


AC ELECTRICAL CHARACTERISTICS

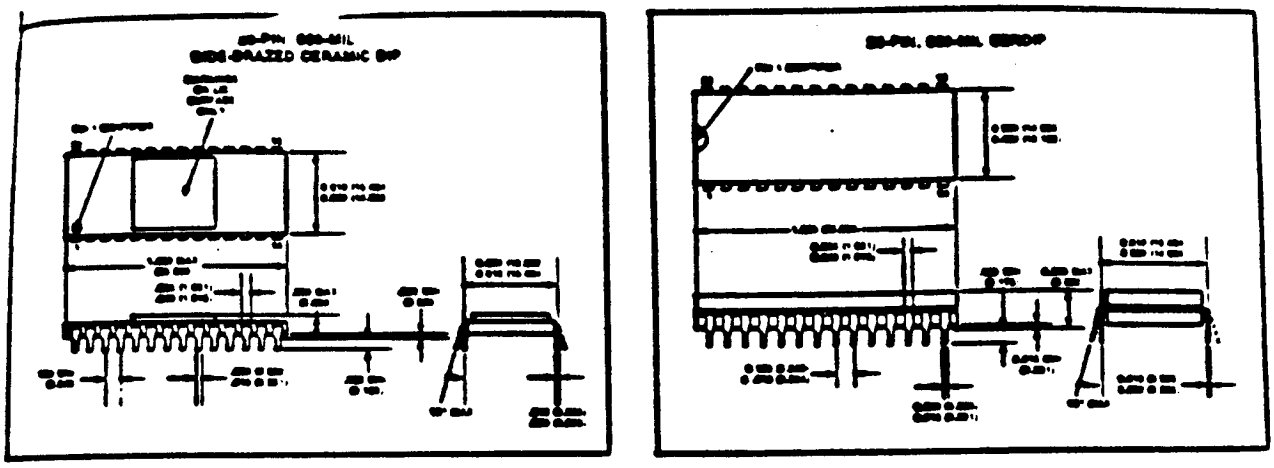
Read Cycle 28C291

TA = 0°C to 70°C, VCC = +5v ± 10% (unless otherwise specified)

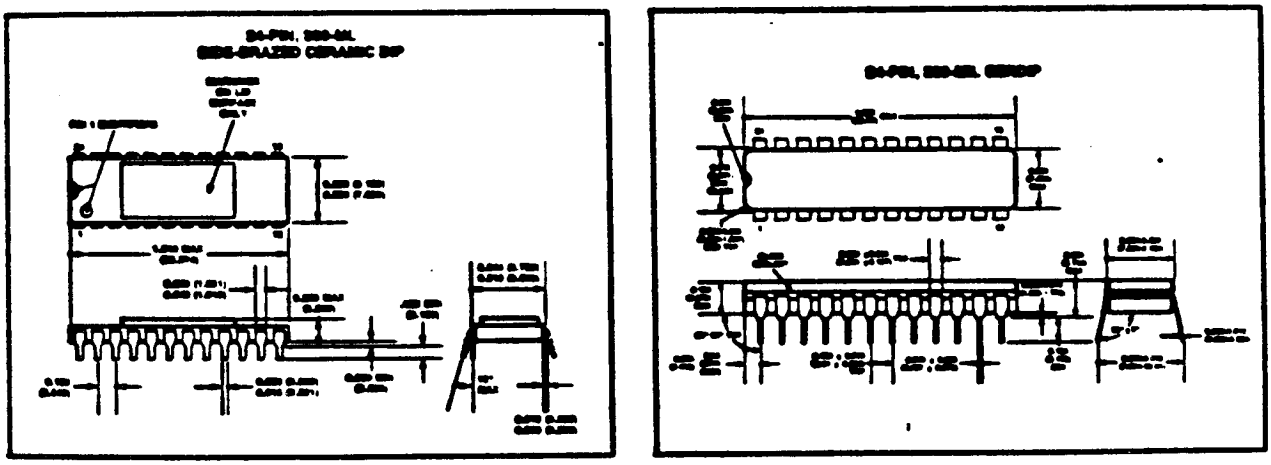
Symbol	Parameter	Min	Typ	Max	Units
tAA	Address Access Time			35	nSec
tAC	Enable Access Time			25	nSec
tDC	Enable Recovery Time			25	nSec



Output Load: tAA is tested with switch S_1 closed and CL=3-pf. tAC is tested with CL=30pf to the 1.5v level. S_1 is open for high impedance to High test and closed for high impedance to low tests. tER is tested with CL=5pf. High to high impedance tests are made with S_1 open to an output voltage of VOH -.5v with S_1 open. Low to high impedance tests are made to the VOL +.5v level with S_1 closed.



28C17



28C291/28C16