

29F52•29F53

8-Bit Registered Transceiver

General Description

The 29F52 and 29F53 are 8-bit registered transceivers. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The A₀–A₇ output pins are guaranteed to sink 24 mA (20 mA mil.) while the B₀–B₇ output pins are designed for 64 mA.

The 29F53 is an inverting option of the 29F52. Both transceivers are AMD Am2952/2953 functional equivalents.

Features

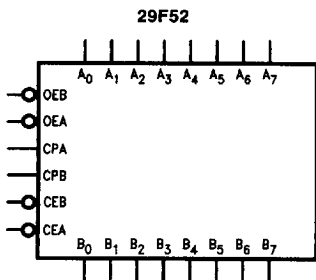
- 8-bit registered transceivers
- Separate clock, clock enable and TRI-STATE output enable provided for each register
- AMD Am2952/2953 functional equivalents
- Both inverting and non-inverting options available
- 24-Pin slimline package

Ordering Code: See Section 11

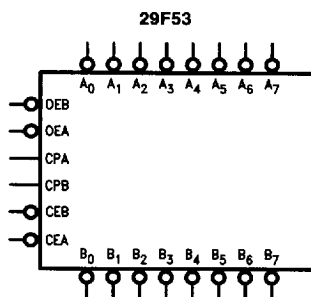
Commercial	Package Number	Package Description
29F52SPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
29F52SC (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
29F53SPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Logic Symbols

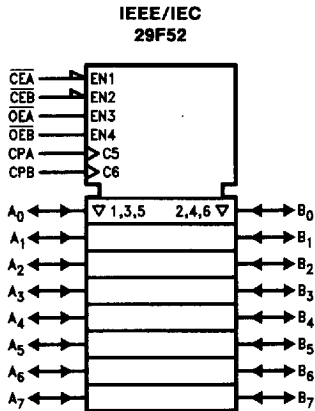


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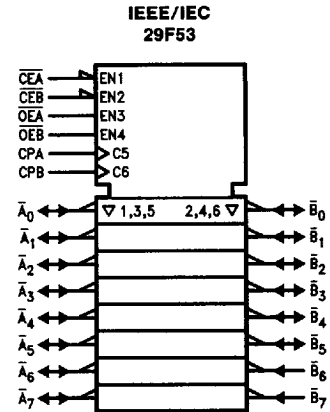


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Logic Symbols (Continued)



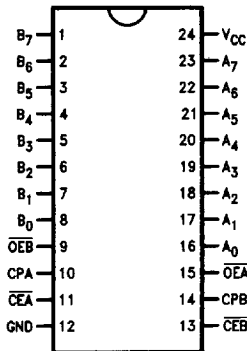
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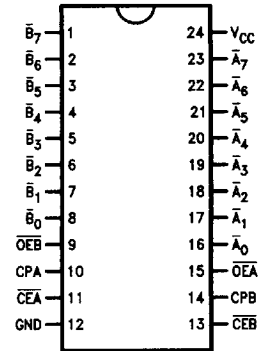
Connection Diagrams

**Pin Assignment
for DIP and SOIC
29F52**



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**Pin Assignment
for DIP
29F53**



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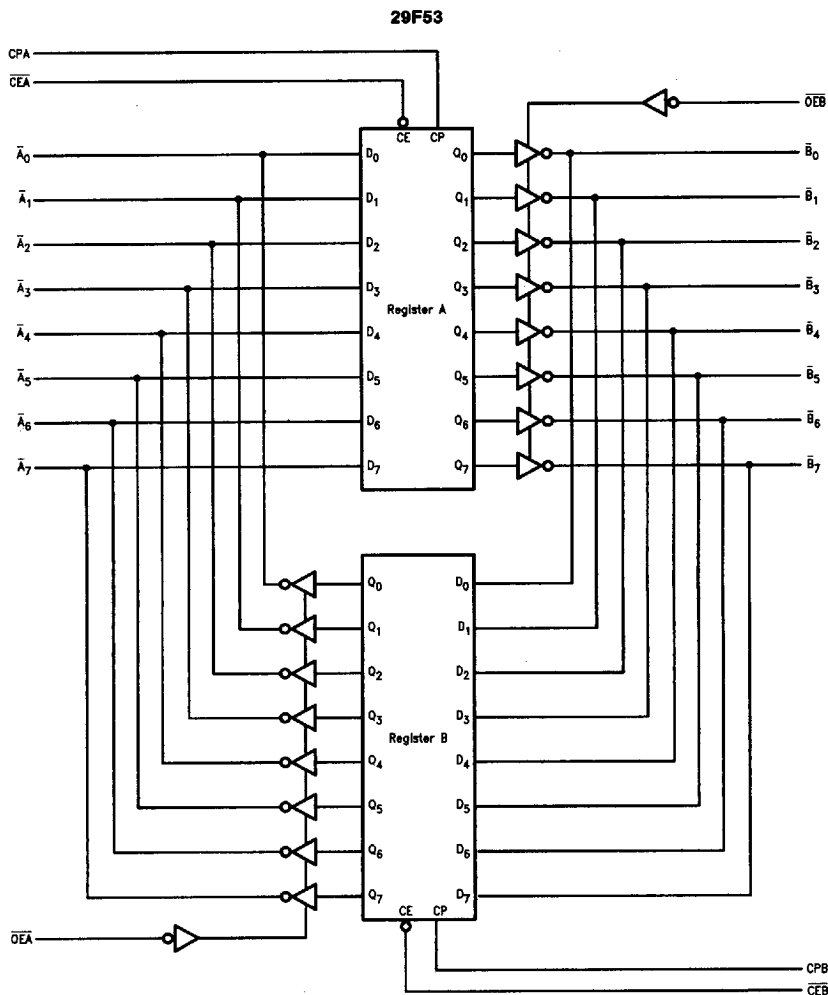
Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A ₀ -A ₇	A-Register Inputs/ B-Register TRI-STATE Outputs	3.5/1.083	70 μ A/0.65 mA
B ₀ -B ₇	B-Register Inputs/ A-Register TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
$\overline{OEA}$	Output Enable A-Register	3.5/1.083	70 μ A/0.65 mA
CPA	A-Register Clock	600/106.6 (80)	-12 mA/64 mA (48 mA)
$\overline{CEA}$	A-Register Clock Enable	1.0/1.0	20 μ A/-0.6 mA
$\overline{OEB}$	Output Enable B-Register	1.0/1.0	20 μ A/-0.6 mA
CPB	B-Register Clock	1.0/1.0	20 μ A/-0.6 mA
$\overline{CEB}$	B-Register Clock Enable	1.0/1.0	20 μ A/-0.6 mA

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Block Diagrams (Continued)



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Output Control

OE	Internal Q	Y-Output		Function
		29F52	29F53	
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = HIGH Impedance

— = LOW-to-HIGH Transition

NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	CE		
X	X	H	NC	Hold Data
L	—	L	L	Load Data
H	—	L	H	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	−55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.0 2.5 2.4 2.0 2.7 2.7		V	Min	I _{OH} = −1 mA (A _N) I _{OH} = −3 mA (A _N , B _N) I _{OH} = −12 mA (B _N) I _{OH} = −1 mA (A _N) I _{OH} = −3 mA (A _N , B _N) I _{OH} = −15 mA (B _N) I _{OH} = −1 mA (A _N) I _{OH} = −3 mA (A _N , B _N)
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC}		0.5 0.55 0.5 0.55	V	Min	I _{OL} = 20 mA (A _N) I _{OL} = 48 mA (B _N) I _{OL} = 24 mA (A _N) I _{OL} = 64 mA (B _N)
I _{IH}	Input HIGH Current			20	μA	Max	V _{IN} = 2.7V (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			100	μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V _{IN} = 5.5V (A _N , B _N)
I _{IL}	Input LOW Current			−0.6	mA	Max	V _{IN} = 0.5V (Non-I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (A _N , B _N)
I _{IL} + I _{OZL}	Output Leakage Current			−650	μA	Max	V _{OUT} = 0.5V (A _N , B _N)
I _{OS}	Output Short-Circuit Current	−60 −100		−150 −225	mA	Max	V _{OUT} = 0V (A _N) V _{OUT} = 0V (B _N)
I _{CEX}	Output HIGH Leakage Current			250	μA	Max	V _{OUT} = V _{CC} (A _N , B _N)
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V (A _N , B _N)
I _{CCH}	Power Supply Current		130	190	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			190	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current			190	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPA or CPB to A_n or B_n	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	2-3
t_{pZH} t_{pZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	2-5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5 2.5	6.5 5.5	9.0 7.5			2.0 2.0	10.0 8.5	ns	2-5

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW A_n or B_n to CPA or CPB	4.0 4.0				4.5 4.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW A_n or B_n to CPA or CPB	2.0 2.0				2.5 2.5		ns	2-6
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{CEA}}$ or $\overline{\text{CEB}}$ to CPA or CPB	1.0 4.0				1.5 4.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{CEA}}$ or $\overline{\text{CEB}}$ to CPA or CPB	2.0 2.0				2.5 2.5		ns	2-6
$t_w(\text{H})$ $t_w(\text{L})$	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0				3.5 3.5		ns	2-4