



128K x 32 Synchronous-Pipelined Cache RAM

Features

- Supports 100-MHz bus for Pentium® and PowerPC™ operations with zero wait states
- Fully registered inputs and outputs for pipelined operation
- 128K by 32 common I/O architecture
- 3.3V core power supply
- 2.5V / 3.3V I/O operation
- Fast clock-to-output times
 - 3.5 ns (for 166-MHz device)
 - 4.0 ns (for 133-MHz device)
 - 5.5 ns (for 100-MHz device)
- User-selectable burst counter supporting Intel® Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- JEDEC-standard 100 TQFP pinout
- “ZZ” Sleep Mode option and Stop Clock option

Functional Description

The CY7C1339 is a 3.3V, 128K by 32 synchronous-pipelined cache SRAM designed to support zero wait state secondary cache with minimal glue logic.

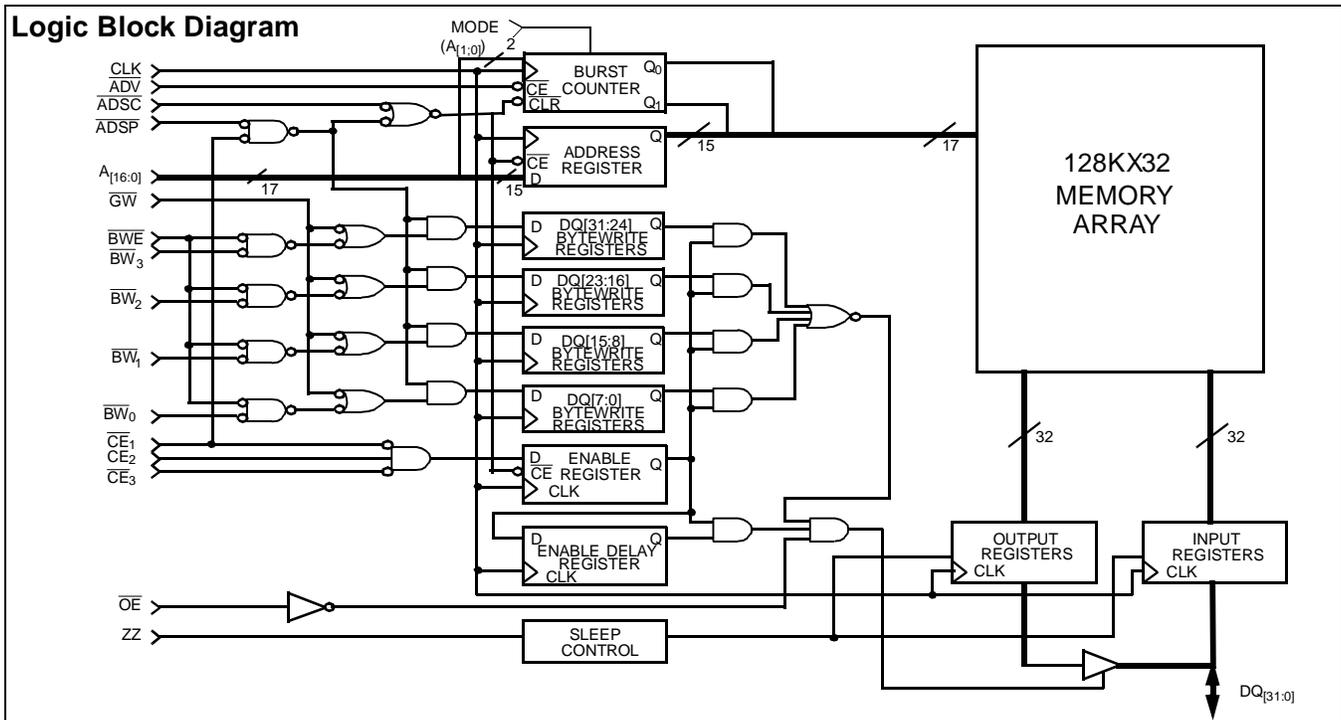
The CY7C1339 I/O pins can operate at either the 2.5V or the 3.3V level; the I/O pins are 3.3V tolerant when $V_{DDQ}=2.5V$.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 3.5 ns (166-MHz device).

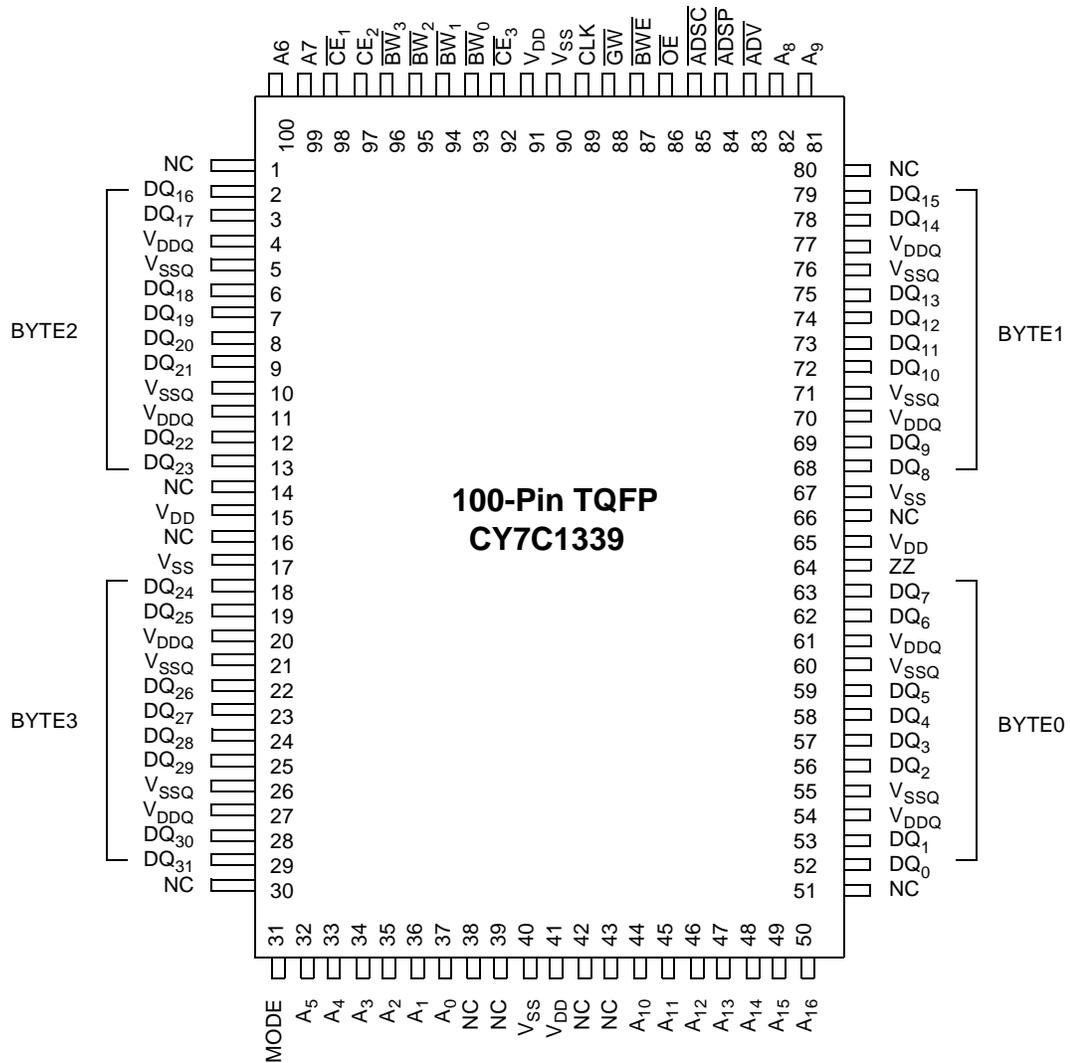
The CY7C1339 supports either the interleaved burst sequence used by the Intel Pentium processor or a linear burst sequence used by processors such as the PowerPC. The burst sequence is selected through the MODE pin. Accesses can be initiated by asserting either the Processor Address Strobe (\overline{ADSP}) or the Controller Address Strobe (\overline{ADSC}) at clock rise. Address advancement through the burst sequence is controlled by the ADV input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the four Byte Write Select ($BW_{[3:0]}$) inputs. A Global Write Enable (\overline{GW}) overrides all byte write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects (\overline{CE}_1 , CE_2 , \overline{CE}_3) and an asynchronous Output Enable (\overline{OE}) provide for easy bank selection and output three-state control. In order to provide proper data during depth expansion, \overline{OE} is masked during the first clock of a read cycle when emerging from a deselected state.



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Pin Configuration

Selection Guide

		7C1339-166	7C1339-133	7C1339-100
Maximum Access Time (ns)		3.5	4.0	5.5
Maximum Operating Current (mA)	Commercial	420	375	325
Maximum CMOS Standby Current (mA)	Commercial	10	10	10

Pin Definitions

Pin Number	Name	I/O	Description
50–44, 81, 82, 99, 100, 32–37	A _[16:0]	Input-Synchronous	Address Inputs used to select one of the 64K address locations. Sampled at the rising edge of the CLK if $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is active LOW, and $\overline{\text{CE}}_1$, CE ₂ , and $\overline{\text{CE}}_3$ are sampled active. A _[1:0] feed the 2-bit counter.
96–93	BW _[3:0]	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{\text{BWE}}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
88	$\overline{\text{GW}}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on BW _[3:0] and $\overline{\text{BWE}}$).
87	$\overline{\text{BWE}}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
89	CLK	Input-Clock	Clock input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{\text{ADV}}$ is asserted LOW, during a burst operation.
98	$\overline{\text{CE}}_1$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE ₂ and $\overline{\text{CE}}_3$ to select/deselect the device. $\overline{\text{ADSP}}$ is ignored if $\overline{\text{CE}}_1$ is HIGH.
97	CE ₂	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_3$ to select/deselect the device.
92	$\overline{\text{CE}}_3$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and CE ₂ to select/deselect the device.
86	$\overline{\text{OE}}$	Input-Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When asserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{\text{OE}}$ is masked during the first clock of a read cycle when emerging from a deselected state.
83	$\overline{\text{ADV}}$	Input-Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
84	$\overline{\text{ADSP}}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, A _[16:0] is captured in the address registers. A _[1:0] are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized. $\overline{\text{ADSP}}$ is ignored when $\overline{\text{CE}}_1$ is asserted HIGH.
85	$\overline{\text{ADSC}}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, A _[16:0] is captured in the address registers. A _[1:0] are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized.
64	ZZ	Input-Asynchronous	ZZ “sleep” Input. This active HIGH input places the device in a non-time-critical “sleep” condition with data integrity preserved. Leaving ZZ floating or NC will default the device into an active state. ZZ has an internal pull down.
29, 28, 25-22, 19, 18,13,12, 9–6, 3, 2, 79, 78, 75–72, 69, 68, 63, 62 59–56, 53, 52	DQ _[31:0]	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A _[16:0] during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{\text{OE}}$. When $\overline{\text{OE}}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ _[31:0] are placed in a three-state condition.
15, 41, 65, 91	V _{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 3.3V power supply.
17, 40, 67, 90	V _{SS}	Ground	Ground for the core of the device. Should be connected to ground of the system.
4, 11, 20, 27, 54, 61, 70, 77	V _{DDQ}	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 3.3V or 2.5V power supply.
5, 10, 21, 26, 55, 60, 71, 76	V _{SSQ}	I/O Ground	Ground for the I/O circuitry. Should be connected to ground of the system.
31	MODE	Input-Static	Selects burst order. When tied to GND selects linear burst sequence. When tied to V _{DDQ} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. When left floating or NC, defaults to interleaved burst order. Mode pin has an internal pull up.
1, 14, 16, 30, 38, 39, 42, 43, 51, 66, 80	NC	-	No Connects.

Introduction

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.5 ns (166-MHz device).

The CY7C1339 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (\overline{ADSP}) or the Controller Address Strobe (\overline{ADSC}). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (\overline{BWE}) and Byte Write Select ($\overline{BW}_{[3:0]}$) inputs. A Global Write Enable (\overline{GW}) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects (\overline{CE}_1 , CE_2 , \overline{CE}_3) and an asynchronous Output Enable (\overline{OE}) provide for easy bank selection and output three-state control. \overline{ADSP} is ignored if \overline{CE}_1 is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) \overline{ADSP} or \overline{ADSC} is asserted LOW, (2) \overline{CE}_1 , CE_2 , \overline{CE}_3 are all asserted active, and (3) the write signals (\overline{GW} , \overline{BWE}) are all deserted HIGH. \overline{ADSP} is ignored if \overline{CE}_1 is HIGH. The address presented to the address inputs ($A_{[16:0]}$) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 3.5 ns (166-MHz device) if \overline{OE} is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the \overline{OE} signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either \overline{ADSP} or \overline{ADSC} signals, its output will three-state immediately.

Single Write Accesses Initiated by \overline{ADSP}

This access is initiated when both of the following conditions are satisfied at clock rise: (1) \overline{ADSP} is asserted LOW, and (2) \overline{CE}_1 , CE_2 , \overline{CE}_3 are all asserted active. The address presented to $A_{[16:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The write signals (\overline{GW} , \overline{BWE} , and $\overline{BW}_{[3:0]}$) and ADV inputs are ignored during this first cycle.

\overline{ADSP} -triggered write accesses require two clock cycles to complete. If \overline{GW} is asserted LOW on the second clock rise, the data presented to the $DQ_{[31:0]}$ inputs is written into the corre-

sponding address location in the RAM core. If \overline{GW} is HIGH, then the write operation is controlled by \overline{BWE} and $\overline{BW}_{[3:0]}$ signals. The CY7C1339 provides byte write capability that is described in the Write Cycle Descriptions table. Asserting the Byte Write Enable input (\overline{BWE}) with the selected Byte Write ($\overline{BW}_{[3:0]}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1339 is a common I/O device, the Output Enable (\overline{OE}) must be deserted HIGH before presenting data to the $DQ_{[31:0]}$ inputs. Doing so will three-state the output drivers. As a safety precaution, $DQ_{[31:0]}$ are automatically three-stated whenever a write cycle is detected, regardless of the state of \overline{OE} .

Single Write Accesses Initiated by \overline{ADSC}

\overline{ADSC} write accesses are initiated when the following conditions are satisfied: (1) \overline{ADSC} is asserted LOW, (2) \overline{ADSP} is deserted HIGH, (3) \overline{CE}_1 , CE_2 , \overline{CE}_3 are all asserted active, and (4) the appropriate combination of the write inputs (\overline{GW} , \overline{BWE} , and $\overline{BW}_{[3:0]}$) are asserted active to conduct a write to the desired byte(s). \overline{ADSC} -triggered write accesses require a single clock cycle to complete. The address presented to $A_{[16:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The ADV input is ignored during this cycle. If a global write is conducted, the data presented to the $DQ_{[31:0]}$ is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1339 is a common I/O device, the Output Enable (\overline{OE}) must be deserted HIGH before presenting data to the $DQ_{[31:0]}$ inputs. Doing so will three-state the output drivers. As a safety precaution, $DQ_{[31:0]}$ are automatically three-stated whenever a write cycle is detected, regardless of the state of \overline{OE} .

Burst Sequences

The CY7C1339 provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting \overline{ADV} LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. \overline{CE}_1 , CE_2 , \overline{CE}_3 , \overline{ADSP} , and \overline{ADSC} must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		3	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

Cycle Descriptions^[1, 2, 3]

Next Cycle	Add. Used	ZZ	\overline{CE}_3	CE_2	CE_1	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{OE}	DQ	Write
Unselected	None	L	X	X	1	X	0	X	X	Hi-Z	X
Unselected	None	L	1	X	0	0	X	X	X	Hi-Z	X
Unselected	None	L	X	0	0	0	X	X	X	Hi-Z	X
Unselected	None	L	1	X	0	1	0	X	X	Hi-Z	X
Unselected	None	L	X	0	0	1	0	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	0	DQ	Read
Continue Read	Next	L	X	X	1	X	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	1	X	1	0	0	DQ	Read
Suspend Read	Current	L	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	X	1	1	1	0	DQ	Read
Suspend Read	Current	L	X	X	1	X	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	1	X	1	1	0	DQ	Read
Begin Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
Begin Write	External	L	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	L	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	L	X	X	1	X	1	0	X	Hi-Z	Write
Suspend Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
ZZ "Sleep"	None	H	X	X	X	X	X	X	X	Hi-Z	X

Note:

1. X="Don't Care," 1=HIGH, 0=LOW.
2. Write is defined by \overline{BWE} , $BW_{[3:0]}$, and \overline{GW} . See Write Cycle Descriptions table.
3. The DQ pins are controlled by the current cycle and the \overline{OE} signal. \overline{OE} is asynchronous and is not sampled with the clock.

Write Cycle Descriptions^[4, 5, 6]

Function	\overline{GW}	\overline{BWE}	\overline{BW}_3	\overline{BW}_2	\overline{BW}_1	\overline{BW}_0
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0 - DQ _[7:0]	1	0	1	1	1	0
Write Byte 1 - DQ _[15:8]	1	0	1	1	0	1
Write Bytes 1, 0	1	0	1	1	0	0
Write Byte 2 - DQ _[23:16]	1	0	1	0	1	1
Write Bytes 2, 0	1	0	1	0	1	0
Write Bytes 2, 1	1	0	1	0	0	1
Write Bytes 2, 1, 0	1	0	1	0	0	0
Write Byte 3 - DQ _[31:24]	1	0	0	1	1	1
Write Bytes 3, 0	1	0	0	1	1	0
Write Bytes 3, 1	1	0	0	1	0	1
Write Bytes 3, 1, 0	1	0	0	1	0	0
Write Bytes 3, 2	1	0	0	0	1	1
Write Bytes 3, 2, 0	1	0	0	0	1	0
Write Bytes 3, 2, 1	1	0	0	0	0	1
Write All Bytes	1	0	0	0	0	0
Write All Bytes	0	X	X	X	X	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage on V_{DD} Relative to GND -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State^[7] -0.5V to $V_{DD} + 0.5V$

DC Input Voltage^[7] -0.5V to $V_{DD} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[8]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	3.3V -5%/+10%	2.5V -5% 3.3V /+10%
Ind'l	-40°C to +85°C	3.3V -5%/+10%	2.5V -5% 3.3V /+10%

Note:

- X="Don't Care," 1=Logic HIGH, 0=Logic LOW.
- The SRAM always initiates a read cycle when ADSP asserted, regardless of the state of \overline{GW} , \overline{BWE} , or $\overline{BW}_{[3:0]}$. Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result, \overline{OE} must be driven HIGH prior to the start of the write cycle to allow the outputs to three-state. \overline{OE} is a don't care for the remainder of the write cycle.
- \overline{OE} is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQ=High-Z when \overline{OE} is inactive or when the device is deselected, and DQ=data when \overline{OE} is active.
- Minimum voltage equals -2.0V for pulse durations of less than 20 ns.
- T_A is the case temperature.

Electrical Characteristics Over the Operating Range

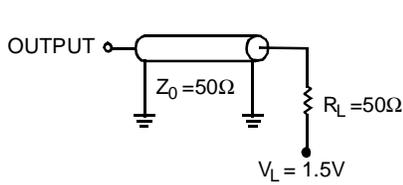
Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{DD}	Power Supply Voltage	3.3V -5%/+10%	3.135	3.6	V
V _{DDQ}	I/O Supply Voltage	2.5V -5% to 3.3V +10%	2.375	3.6	V
V _{OH}	Output HIGH Voltage	V _{DDQ} = 3.3V, V _{DD} = Min., I _{OH} = -4.0 mA	2.4		V
		V _{DDQ} = 2.5V, V _{DD} = Min., I _{OH} = -2.0 mA	2.0		V
V _{OL}	Output LOW Voltage	V _{DDQ} = 3.3V, V _{DD} = Min., I _{OL} = 8.0 mA		0.4	V
		V _{DDQ} = 2.5V, V _{DD} = Min., I _{OL} = 2.0 mA		0.7	V
V _{IH}	Input HIGH Voltage	V _{DDQ} = 3.3V	2.0	V _{DD} + 0.3V	V
V _{IH}	Input HIGH Voltage	V _{DDQ} = 2.5V	1.7	V _{DD} + 0.3V	V
V _{IL}	Input LOW Voltage ^[7]	V _{DDQ} = 3.3V	-0.3	0.8	V
V _{IL}	Input LOW Voltage ^[7]	V _{DDQ} = 2.5V	-0.3	0.7	V
I _X	Input Load Current except ZZ and MODE	GND ≤ V _I ≤ V _{DDQ}	-5	5	μA
	Input Current of MODE	Input = V _{SS}	-30		μA
		Input = V _{DDQ}		5	μA
	Input Current of ZZ	Input = V _{SS}	-5		μA
Input = V _{DDQ}			30	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{DDQ} , Output Disabled	-5	5	μA
I _{DD}	V _{DD} Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{CYC}	6-ns cycle, 166 MHz	420	mA
			7.5-ns cycle, 133 MHz	375	mA
			10-ns cycle, 100 MHz	325	mA
I _{SB1}	Automatic CS Power-Down Current—TTL Inputs	Max. V _{DD} , Device Deselected, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} = 1/t _{CYC}	6-ns cycle, 166 MHz	150	mA
			7.5-ns cycle, 133 MHz	125	mA
			10-ns cycle, 100 MHz	115	mA
I _{SB2}	Automatic CS Power-Down Current—CMOS Inputs	Max. V _{DD} , Device Deselected, V _{IN} ≤ 0.3V or V _{IN} ≥ V _{DDQ} - 0.3V, f = 0	All speeds	10	mA
I _{SB3}	Automatic CS Power-Down Current—CMOS Inputs	Max. V _{DD} , Device Deselected, or V _{IN} ≤ 0.3V or V _{IN} ≥ V _{DDQ} - 0.3V, f = f _{MAX} = 1/t _{CYC}	6-ns cycle, 166 MHz	125	mA
			7.5-ns cycle, 133 MHz	95	mA
			10-ns cycle, 100 MHz	85	mA
I _{SB4}	Automatic CS Power-Down Current—TTL Inputs	Max. V _{DD} , Device Deselected, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = 0		18	mA

Capacitance^[9]

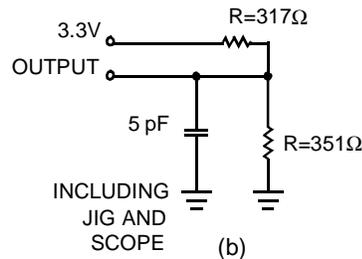
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{DD} = 3.3V, V _{DDQ} = 3.3V	4	pF
C _{CLK}	Clock Input Capacitance		4	pF
C _{I/O}	Input/Output Capacitance		4	pF

Note:

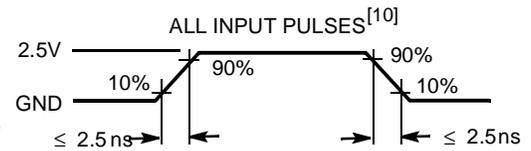
9. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


(a)



(b)



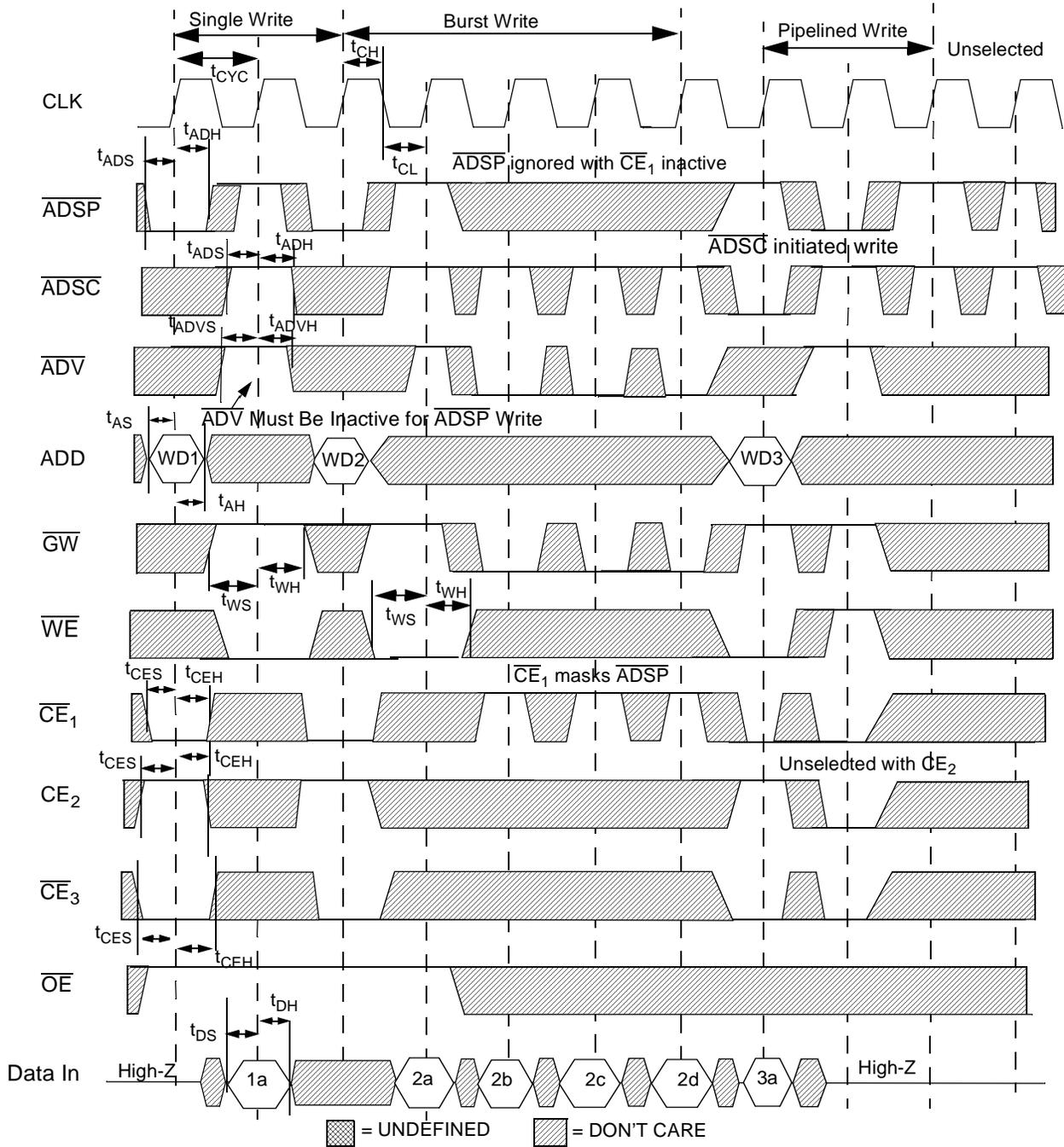
(c)

Switching Characteristics Over the Operating Range^[11,12,13]

Parameter	Description	-166		-133		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	6.0		7.5		10		ns
t _{CH}	Clock HIGH	1.7		1.9		3.5		ns
t _{CL}	Clock LOW	1.7		1.9		3.5		ns
t _{AS}	Address Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t _{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t _{CO}	Data Output Valid After CLK Rise		3.5		4.0		5.5	ns
t _{DOH}	Data Output Hold After CLK Rise	1.5		2.0		2.0		ns
t _{ADS}	\overline{ADSP} , \overline{ADSC} Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t _{ADH}	\overline{ADSP} , \overline{ADSC} Hold After CLK Rise	0.5		0.5		0.5		ns
t _{WES}	\overline{BWE} , \overline{GW} , $\overline{BW}[3:0]$ Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t _{WEH}	\overline{BWE} , \overline{GW} , $\overline{BW}[3:0]$ Hold After CLK Rise	0.5		0.5		0.5		ns
t _{ADVS}	\overline{ADV} Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t _{ADVH}	\overline{ADV} Hold After CLK Rise	0.5		0.5		0.5		ns
t _{DS}	Data Input Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t _{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t _{CES}	Chip Select Set-Up	2.0		2.5		2.5		ns
t _{CEH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
t _{CHZ}	Clock to High-Z ^[12]		3.5		3.5		3.5	ns
t _{CLZ}	Clock to Low-Z ^[12]	0		0		0		ns
t _{EOHZ}	\overline{OE} HIGH to Output High-Z ^[12, 13]		3.5		3.5		5.5	ns
t _{EOLZ}	\overline{OE} LOW to Output Low-Z ^[12, 13]	0		0		0		ns
t _{EOV}	\overline{OE} LOW to Output Valid ^[12]		3.5		4.0		5.5	ns

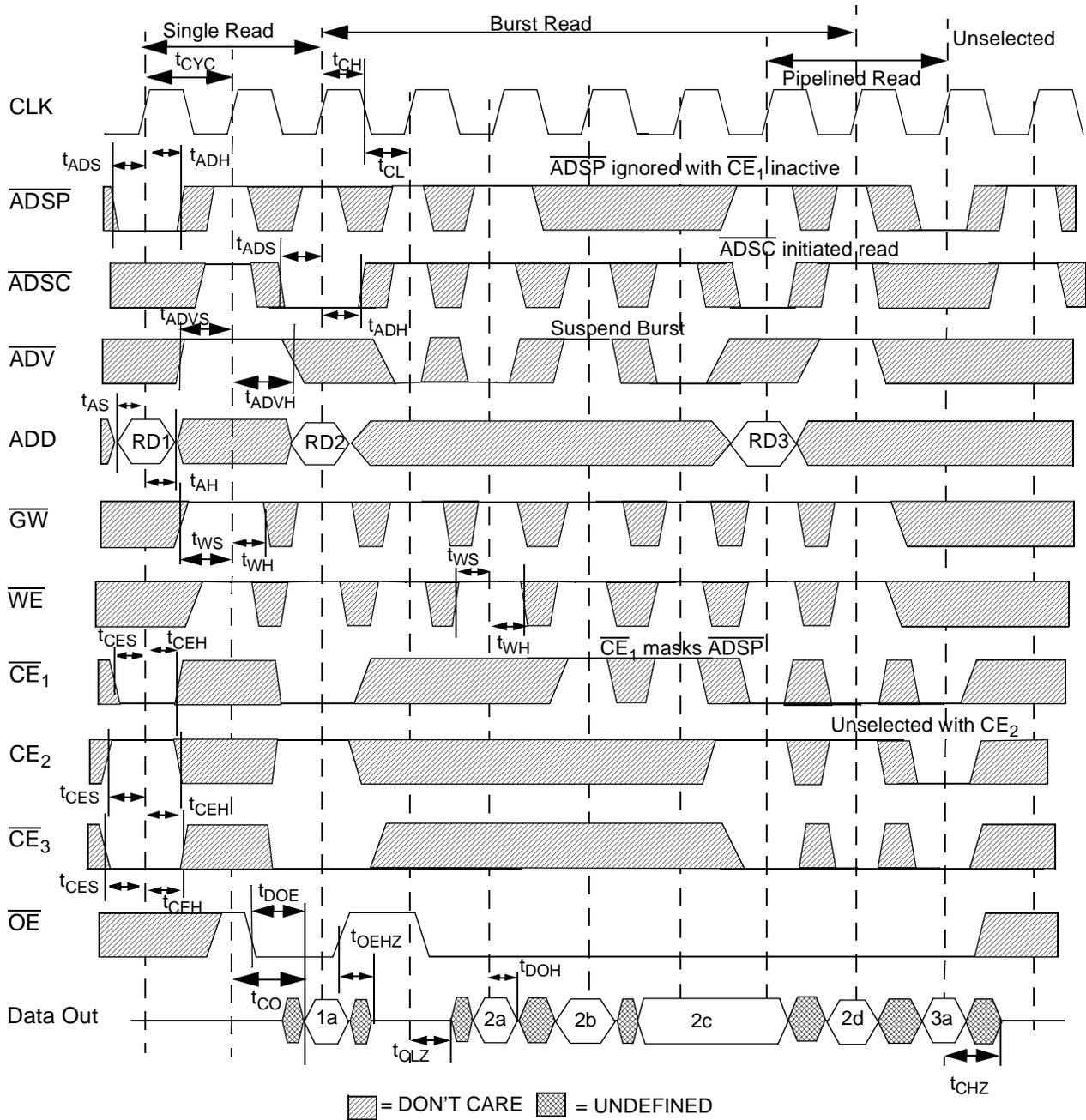
Notes:

- Input waveform should have a slew rate of 1 V/ns.
- Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC test loads.
- t_{CHZ}, t_{CLZ}, t_{EOV}, t_{EOLZ}, and t_{EOHZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mf from steady-state voltage.
- At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ}.

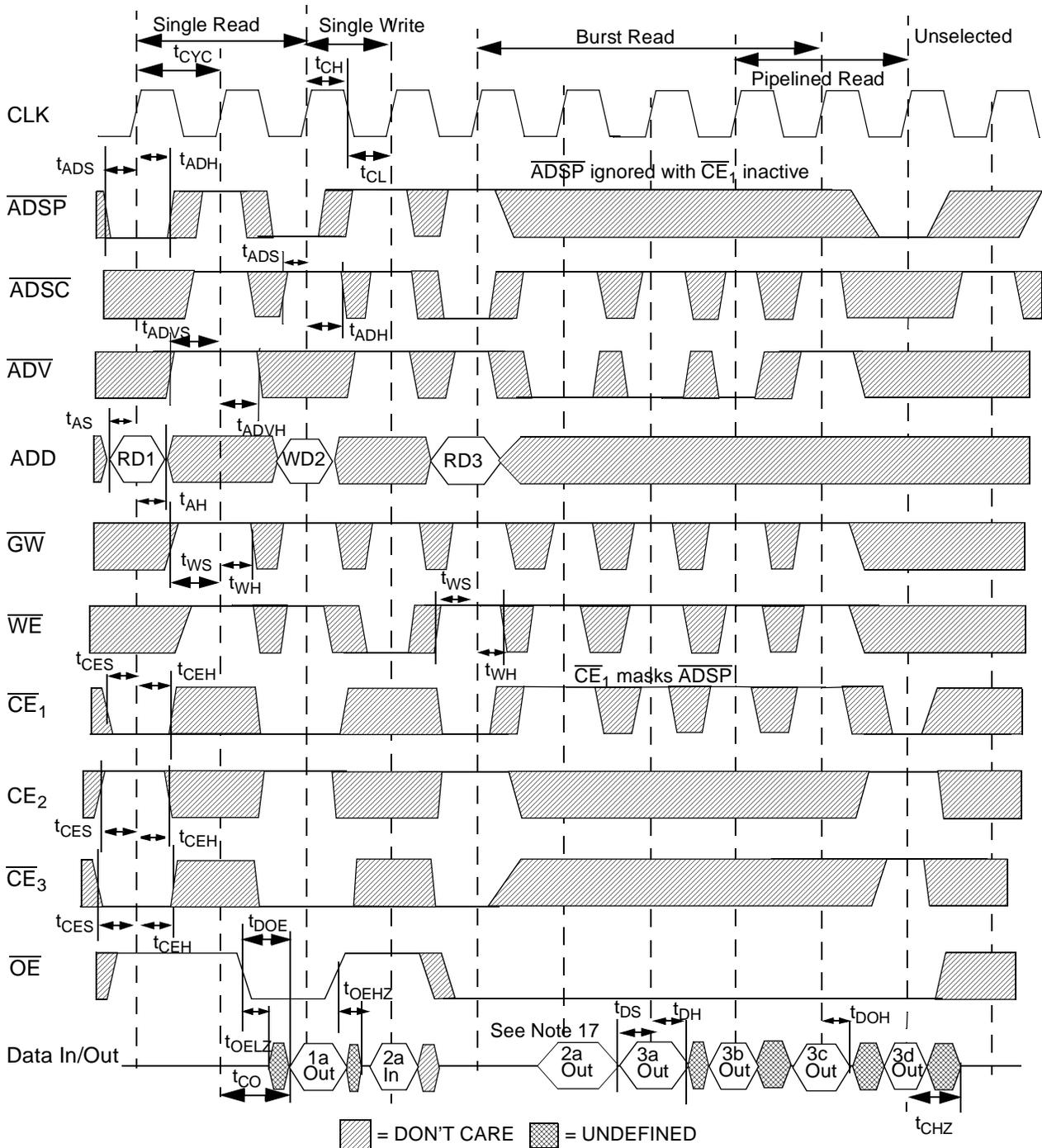
Switching Waveforms
Write Cycle Timing^[14, 15]

Notes:

14. WE is the combination of \overline{BWE} , $\overline{BW}_{[3:0]}$, and \overline{GW} to define a write cycle (see Write Cycle Descriptions table).
15. WDX stands for Write Data to Address X.

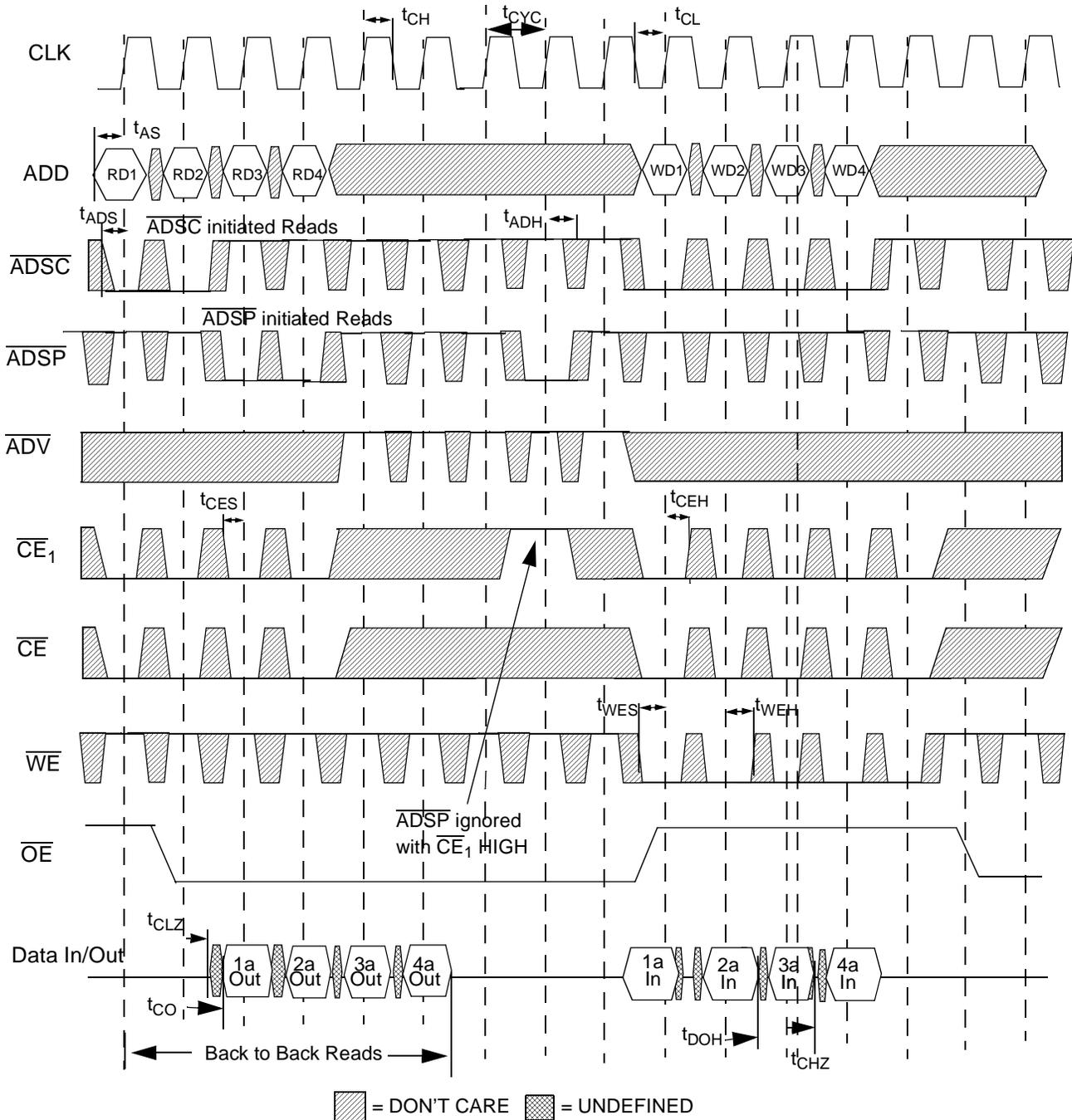
Switching Waveforms (continued)

Read Cycle Timing^[14, 16]

Note:

16. RDx stands for Read Data from Address X.

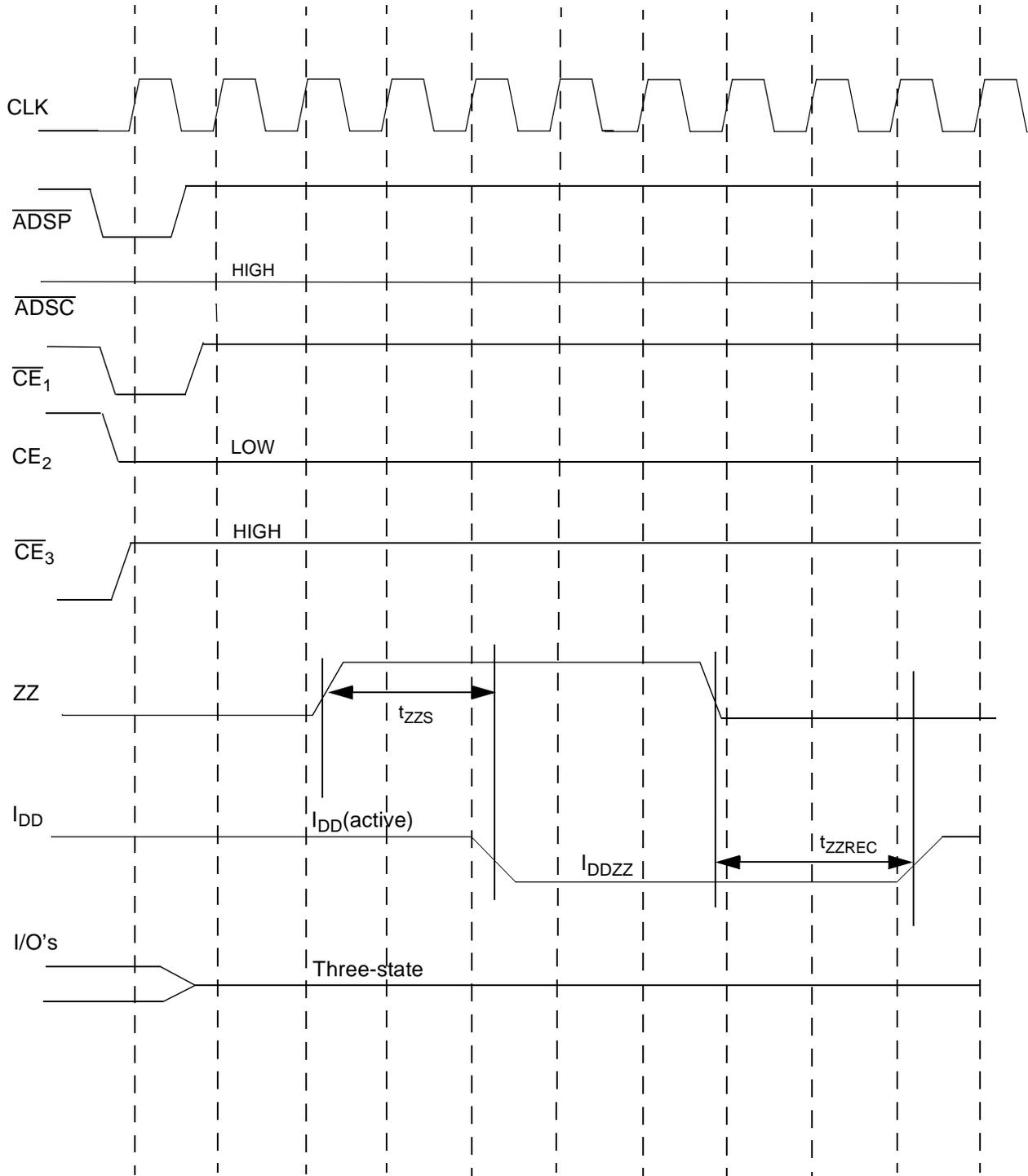
Switching Waveforms (continued)
Read/Write Cycle Timing^[14, 15, 16, 17]


Note:
 17. Data bus is driven by SRAM, but data is not guaranteed.

Switching Waveforms (continued)
Pipeline Timing^[18, 19]

Notes:

18. Device originally deselected.
19. CE is the combination of CE₂ and CE₃. All chip selects need to be active in order to select the device.

Switching Waveforms (continued)

ZZ Mode Timing ^[20, 21]

Note:

20. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
 21. I/Os are in three-state when exiting ZZ sleep mode.

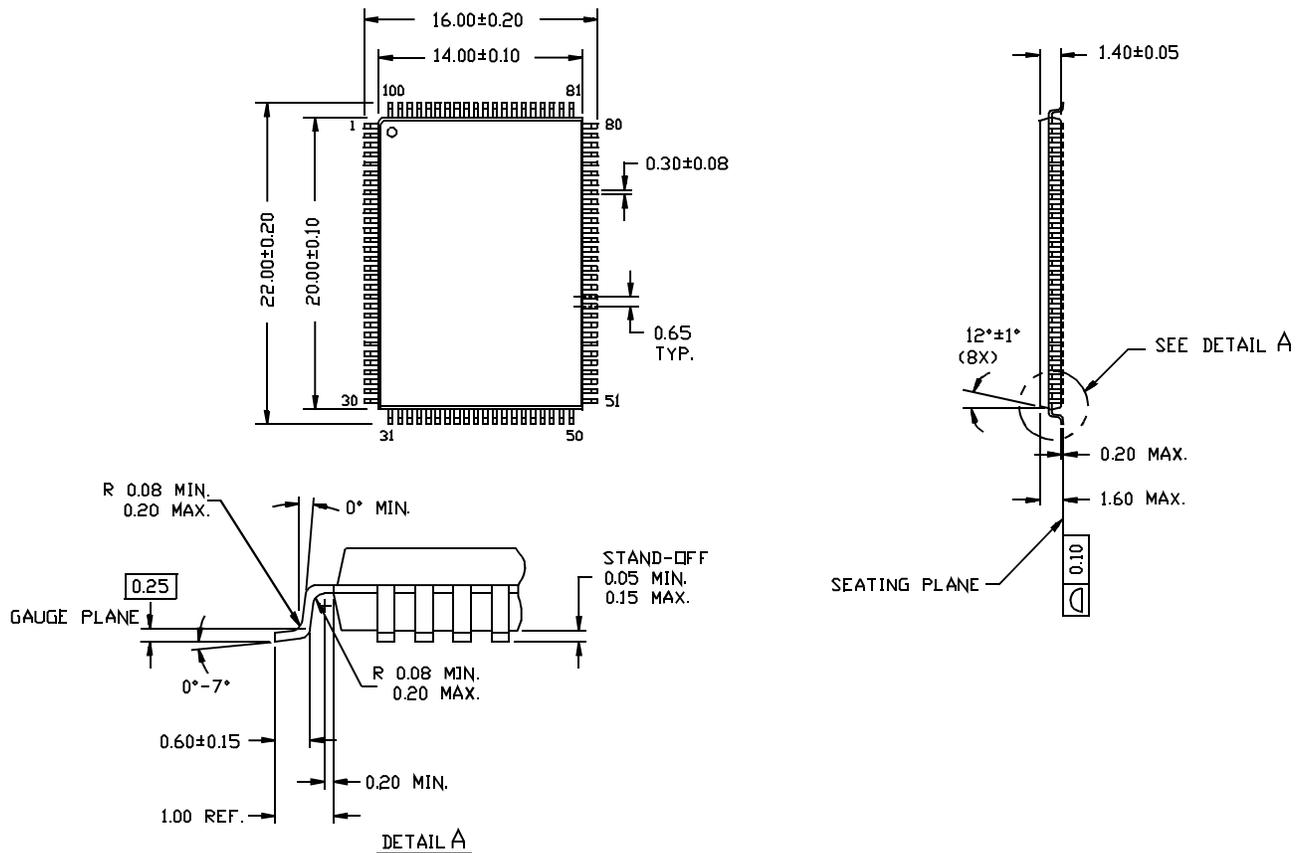
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	CY7C1339-166AC	A101	100-Lead Thin Quad Flat Pack	Commercial
133	CY7C1339-133AC			
100	CY7C1339-100AC			
133	CY7C1339-133AI			Industrial

Document #: 38-00723-C

Package Diagram
100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

DIMENSIONS ARE IN MILLIMETERS.



51-85050-A

GERMANIUM PNP HIGH POWER TRANSISTORS

DEVICES	PKG	DEVICES	PKG	DEVICES	PKG	DEVICES	PKG	DEVICES	PKG
2N58A	R173	2N629	T03	2N2144A	T03	2N2612	T03	2N5436	T03
2N143/13	T013	2N630	T03	2N2145A	T03	2N2833	T03	2N5437	T03
2N174A	T036	2N665	T03	2N2146A	T03	2N2834	T03	2N5438	T03
2N277	T036	2N669	T03	2N2152	T85	2N2912	R74	2N5439	T03
2N278	T036	2N1011	T03	2N2152A	T85	2N4048	T036	2N5440	T03
2N297A	T03	2N1038	R122	2N2153	T85	2N4049	T036	2N5887	T066
2N350	T03	2N1042	T6	2N2154	T85	2N4050	T036	2N5888	T066
2N351	T03	2N1073	T15	2N2155	T85	2N4051	T036	2N5889	T066
2N375	T03	2N1073A	F15	2N2155A	T85	2N4052	T036	2N5890	T066
2N376	T03	2N1099	T036	2N2156	T85	2N4053	T036	2N5891	T066
2N379	T03	2N1100	T036	2N2156A	T85	2N4276	T03	2N5892	T066
2N380	T03	2N1159	T03	2N2157	T85	2N4277	T03	2N5893	T066
2N441	T036	2N1261	T36	2N2157A	T85	2N4278	T03	2N5894	T066
2N442	T036	2N1502	T036	2N2158	T85	2N4279	T03	2N5895	T066
2N443	T036	2N1521	T036	2N2158A	T85	2N4280	T03	2N5896	T066
2N456A	T03	2N1541A	T03	2N2159	T85	2N4281	T03	2N5897	T066
2N458A	T03	2N1751	F35	2N2553	T27	2N4282	T03	2N5898	T066
2N459A	F4a	2N1760	T03	2N2555	T27	2N4283	T03	2N5899	T066
2N574A	T7	2N2076A	T036	2N2558	T28	2N5324	T03	2N5900	T066
2N627	T03	2N2142A	T03	2N2560	T28	2N5325	T03	2N5901	T066
2N628	T03	2N2143A	T03	2N2564	R122	2N5435	T03	DTG2400	Y204a

GERMANIUM NPN LOW POWER TRANSISTORS

DEVICES	PKG	DEVICES	PKG
2N35	03J	2N228	T022
2N78	05	2N229	T022
2N94	T022	2N333	T022
2N97	T05	2N388A	T05
2N98	03e	2N1302	T05
2N99	03e	2N1304	T05
2N103	03e	2N1306	T05
2N124	03e	2N1308	T05
2N125	03e		
2N212	T022		
2N213	03e		
2N214	T022		

TO64

NOTES

- The outline contour with exception of hexagon is optional within zone or dimension specified.
- Minimum difference in terminal lengths to establish datum line for numbering terminals.
- Contour and orientation of fixed terminal lugs are optional.
- A chamfer (or undercut) on one or both ends of hexagonal portion is optional.
- Pitch diameter - thread 10-32 UNF-2A (coated). Reference (screw thread standards for federal services - handbook H-28).
- Minimum diameter of seating plane.
- Minimum spacing between terminals.

TO66

NOTES

- Dimension does not include sealing flanges.
- The outline contour is optional within zone defined by these dimensions.

TO83

W52

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q
W52	.970	.375	.239	.220	.085	.004	.720	.790	.122	.390	.245	40*			.117
	.980	.383	.281	.230	.105	.006	.730	.810	.127	.410	.255	50*			.123
W52a	.970	.465	.229	.085	.084	.004	.720	1.40	.122	.700	.245	40*			.117
	.980	.475	.265	.155	.100	.006	.730	1.50	.127	.750	.255	50*			.123
W52b	.970	.373	.239	.220	.085	.004	.720	.850	.123	.425	.245	40*	.150		.117
	.980	.383	.281	.230	.105	.006	.730	.870	.127	.435	.255	50*	.180		.123
W52c		.375	.260	.225	.100	.005	.725				.250	45*	.160	.160	.125
W52d		.500	.285	.225	.125	.005	.725				.250	45*	.165	.160	.125
W52e		.450	.244	.221	.085	.004	.720	1.05			.245	40*	.145	.159	.122
		.510	.286	.229	.105	.006	.730	1.06			.255	50*	.175	.181	.127
W52f	.970	.464	.229	.085	.083	.003	.720	1.39	.122	.698	.244	40*	.144		.116
	.979	.509	.264	.155	.100	.005	.729	1.49	.127	.749	.255	50*	.170		.122
W52g	.970	.465	.229	.085	.084	.004	.720	1.400	.122	.700	.245	40*	.144	.145	.115
	.980	.510	.275	.155	.100	.006	.730	1.500	.127	.750	.255	50*	.178	.175	.125
W52h	.970	.370	.229	.215	.085	.004	.720	.850	.122	.425	.245	40*	.160	.144	.113
	.980	.390	.281	.235	.105	.006	.730	.870	.127	.435	.255	50*	.180	.176	.130
W52j	.970	.490	.229	.240	.085	.004	.720	.970	.122	.485	.245	40*	.150	.144	.113
	.980	.510	.281	.260	.105	.006	.730	1.030	.127	.515	.255	50*	.180	.176	.130
W52k	.970	.370	.229	.215	.085	.004	.720	.790	.122	.395	.245	40*	.150		.113
	.980	.390	.281	.235	.105	.006	.730	.810	.127	.405	.255	50*	.180		.130
W52m	.970	.465	.229	.085	.084	.003	.720			.700	.245	45*	.144		.115
	.980	.510	.275	.155	.110	.007	.730			MIN	.255	NOM	.178		.130
W52n	.970	.495	.229	.216	.084	.003	.720	.870	.123	.435	.246	45*	.144	.145	.115
	.980	.510	.275	.235	.110	.007	.730	MIN		MIN	.255	NOM	.178	.175	.130
W52p	.970	.465	.229	.216	.084	.003	.720			.435	.246	45*	.144		.115
	.980	.510	.275	.235	.110	.007	.730			MIN	.255	NOM	.178		.130
W52q	.975	.490	.250	.120			.725	1.450			.250	45*	.190		.120
W52r		.480	.248	.218	.106	.004	.718				.240		.150		.122
		.520	.287	.222	.130	.008	.730				.256		.181		.130
W52a	.963	.386	.256	.216	.086	.004	.719	1.03				45*	.162		.122
	.985	.385	.276	.232	.110		.730	1.09					.182		.130
W52c	.384	.385	.285	.216	.100	.004	.725	.787	.129	.393	.249	45*	.161	.185	.114
	MAX	MAX	MAX	.232		.005		.811	MAX	.405			.179	MAX	.125
W52u	.592	.511	.275	.216	.094	.004	.725	1.063	.082	.631	.250	45*	.102	.149	.114
	MAX	MAX	MAX	.232		.006		1.141	.067	.670			.125	.173	.125
W52v	.967	.500	.260	.220	.116	.004	.719	1.138	.118	.569	.242	40*	.152	.100	.118
	.983	MAX	.275	.230	.136	.006	.730	MAX	.134	MAX	.258	50*	.171		.134

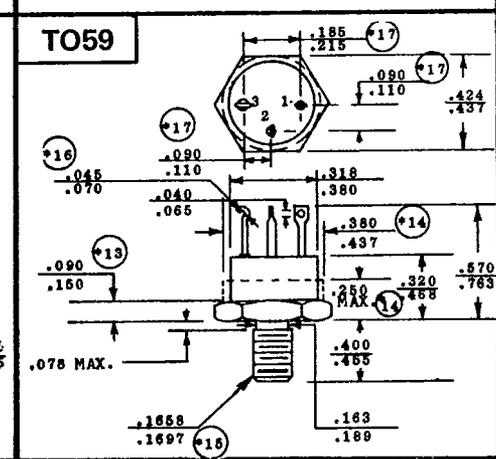
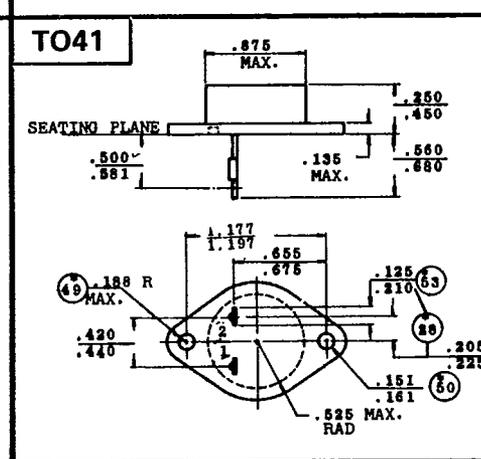
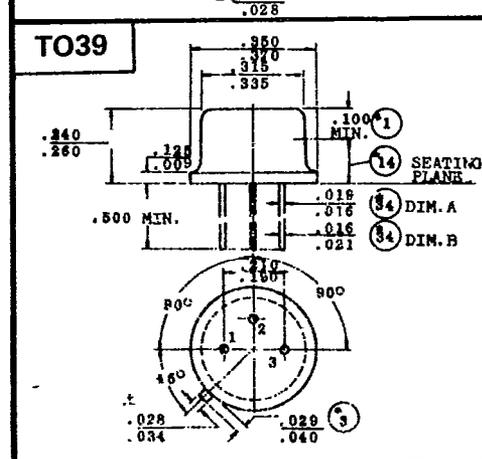
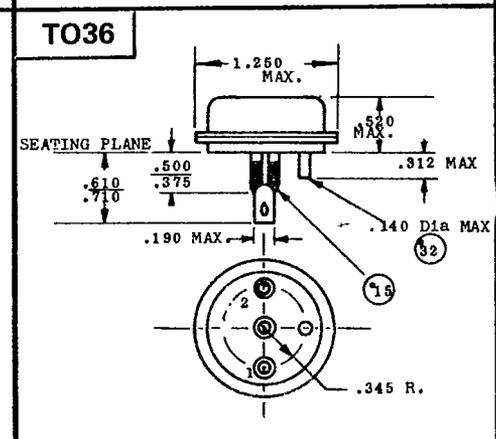
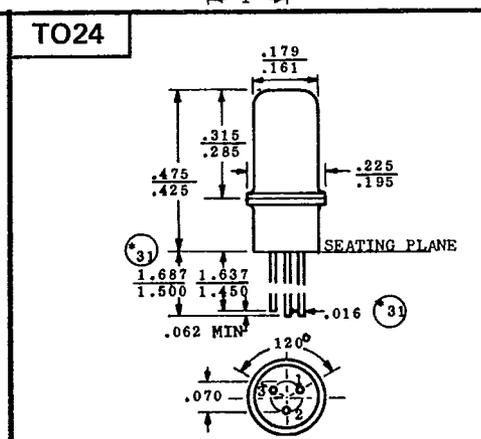
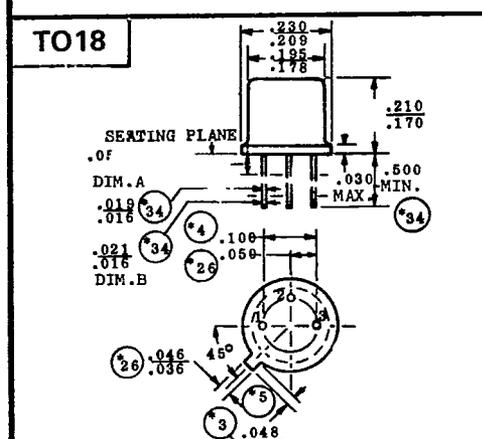
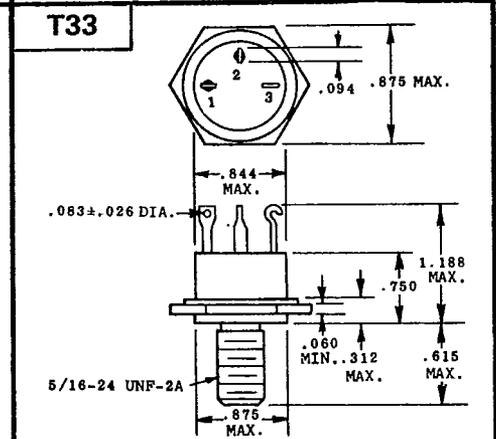
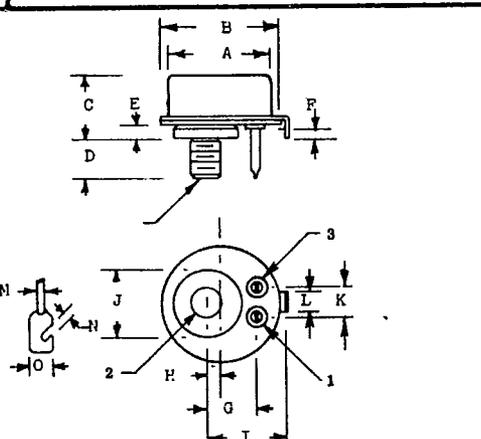
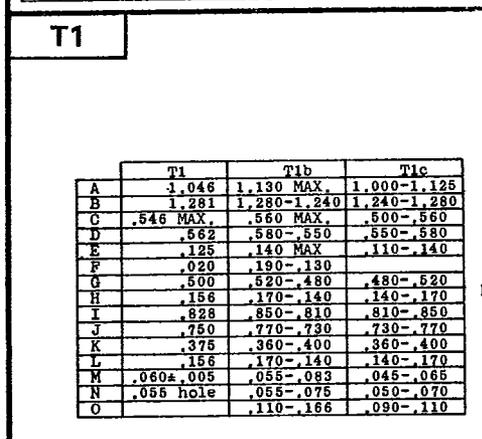
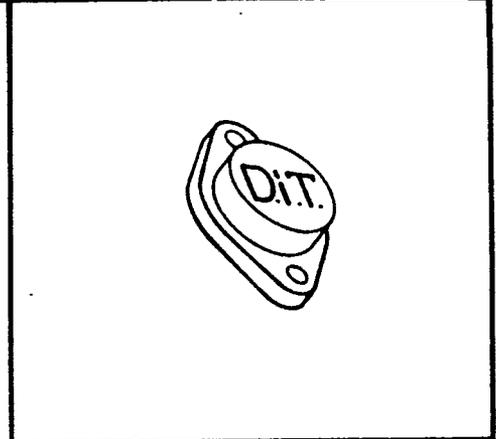
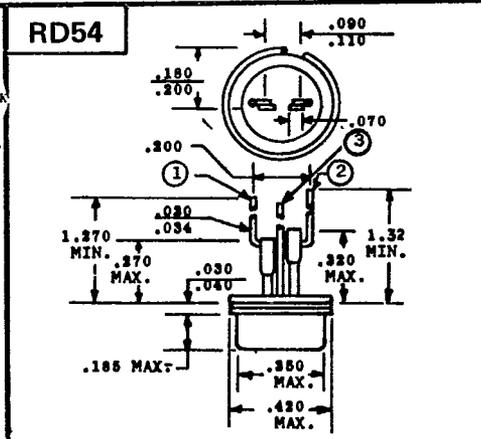
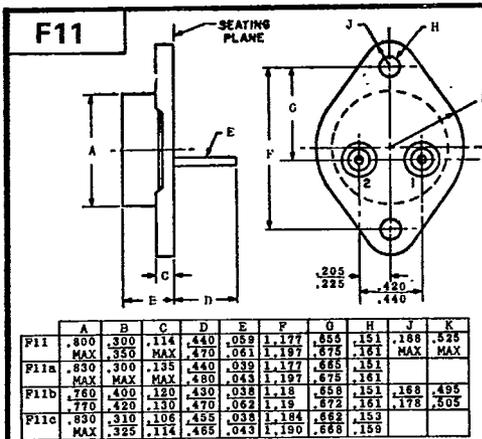
Torque on screw min 0.6 Nm (6 kg cm)
max 0.75 Nm (7.5 kg cm)

Recommended screw: raised cheese-head 4 40 UNC/2A

Heatsink compound must be applied sparingly and evenly

PROBLEM HARD COPY

DIODE TRANSISTOR CO INC TRANSISTOR & RECTIFIER OUTLINES



14

