2N6905 SERIES

Siliconix incorporated

T-27-27

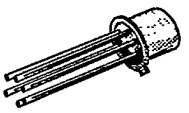
N-Channel JFET Pairs

The 2N6905 Series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and drift over temperature specifications. It is targeted for use in a wide range of precision instrumentation applications. The 2N6905 Series has a wide selection of both offset and drift ranges with the prime device, the 2N6905, featuring 5 mV offset and 10 µV/°C drift. The three devices allow designers to make important cost/benefit decisions. This series is available in a TO-71 hermetically sealed package and is available with military screening. (See Section 1.)

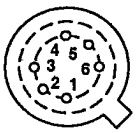
For additional design information please see performance curves NNR, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
2N6905	-35	2	-5	5
2N6906	-35	2	-5	10
2N6907	-35	2	-5	25

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- High-Gain, See 2N5911 Series
- SO-8, See SST404 Series
- Chips, Order 2N690XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-35	V
Gate-Source Voltage		V_{GS}	-35	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.6	mW/°C
	Total		5	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

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ELECTRICAL CHARACTERISTICS[1]

PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	LIMITS 2N6905 MIN	2N6905 MAX	2N6906 MIN	2N6906 MAX	2N6907 MIN	2N6907 MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-1.5	-0.2	-3	-0.2	-3	-0.2	-3	V
Saturation Drain[3] Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-2		-15		-15		-15	pA
		T_A = 125°C	-1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	-2		-5		-5		-5	pA
		T_A = 125°C	-0.8		-5		-5		-5	nA
Drain-Source On-Resistance[4]	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		4		20		20		20	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3		3	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 10 Hz	10		15		15		15	$nV/\sqrt{Hz}$
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 200 µA			5		10		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 200 µA, T = -55 to 25°C			10		25		25	µV/°C
		T = 25 to 125°C			10		25		50	µV/°C
Saturation Drain Current Ratio[4]	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.97							
Transconductance Ratio[4]	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 0.2 mA, f = 1 kHz	0.97							
Differential Output Conductance[4]	$\lvert g_{os1}-g_{os2}\rvert$		0.1							µS
Differential Gate Current[4]	$\lvert I_{G1}-I_{G2}\rvert$	V_{DG} = 15 V, I_D = 0.2 mA, T_A = 25°C	1							pA
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	102	95		95		95		dB

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

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