

N-channel vertical D-MOS transistor

2N7002

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits, with applications in relay, high-speed and line transformer drivers.

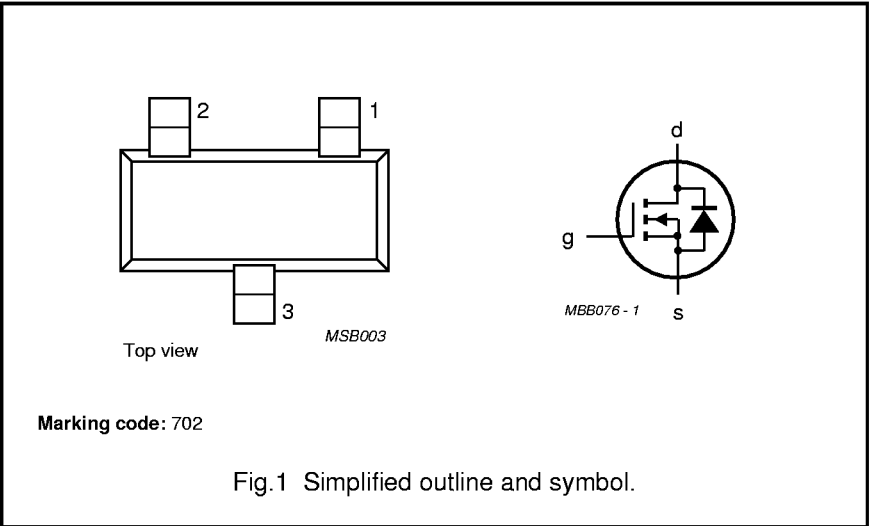
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	180	mA
$R_{DS(on)}$	drain-source on-resistance	$I_D = 500\text{ mA}$ $V_{GS} = 10\text{ V}$	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ $V_{GS} = V_{DS}$	3	V

PIN CONFIGURATION



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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	180	mA
I_{DM}	drain current	peak value	–	800	mA
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$ (note 1) (note 2)	– –	300 250	mW mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Notes

1. Mounted on a ceramic substrate measuring $10 \times 8 \times 0.7$ mm.
2. Mounted on a printed circuit board.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R_{thj-a}	from junction to ambient	note 1 note 2	430 500	K/W K/W

Notes

1. Mounted on a ceramic substrate measuring $10 \times 8 \times 0.7$ mm.
2. Mounted on a printed circuit board.

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CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$ $V_{GS} = 0$	60	90	–	V
I_{DSS}	drain-source leakage current	$V_{DS} = 48\text{ V}$ $V_{GS} = 0$	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$V_{DS} = 0$ $\pm V_{GS} = 15\text{ V}$	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ $V_{GS} = V_{DS}$	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 500\text{ mA}$ $V_{GS} = 10\text{ V}$	–	3.5	5	Ω
		$I_D = 75\text{ mA}$ $V_{GS} = 4.5\text{ V}$	–	–	5.3	Ω
$ Y_{fs} $	transfer admittance	$I_D = 200\text{ mA}$ $V_{DS} = 10\text{ V}$	100	200	–	mS
C_{iss}	input capacitance	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	–	25	40	pF
C_{oss}	output capacitance	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	–	22	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 200\text{ mA}$ $V_{DD} = 50\text{ V}$ $V_{GS} = 0\text{ to }10\text{ V}$	–	–	10	ns
t_{off}	turn-off time	$I_D = 200\text{ mA}$ $V_{DD} = 50\text{ V}$ $V_{GS} = 0\text{ to }10\text{ V}$	–	–	15	ns

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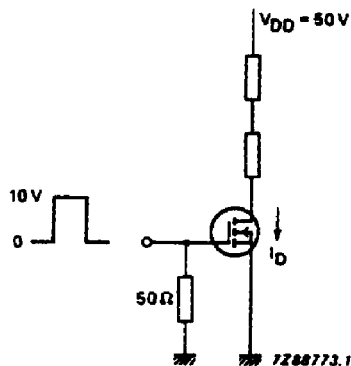


Fig.2 Switching time test circuit.

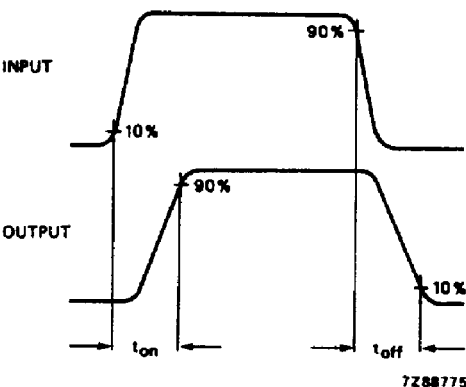
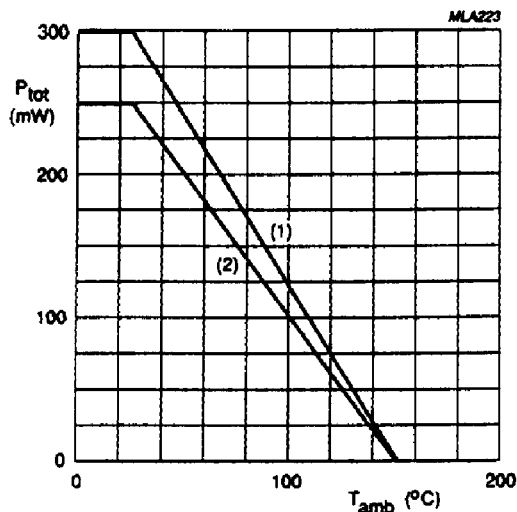


Fig.3 Input and output waveforms.



- (1) On ceramic substrate.
- (2) On printed circuit board.

Fig.4 Power derating curve.

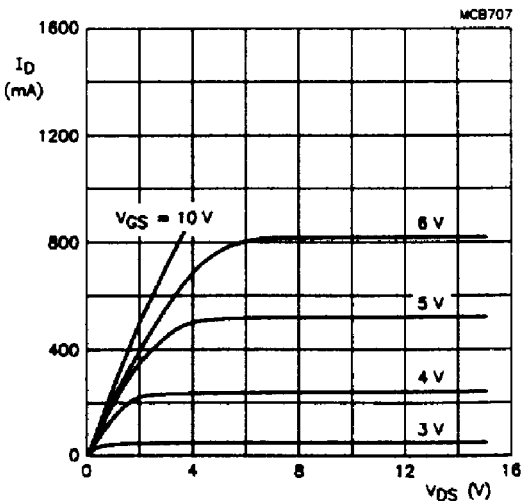


Fig.5 Typical output characteristics; T_J = 25 °C.

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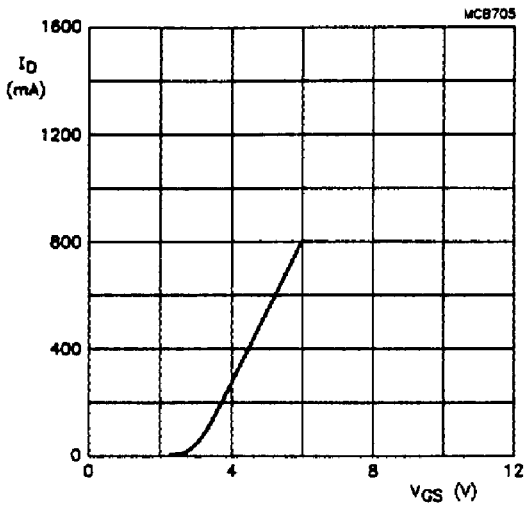


Fig.6 Typical transfer characteristic; $V_{DS} = 10\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$.

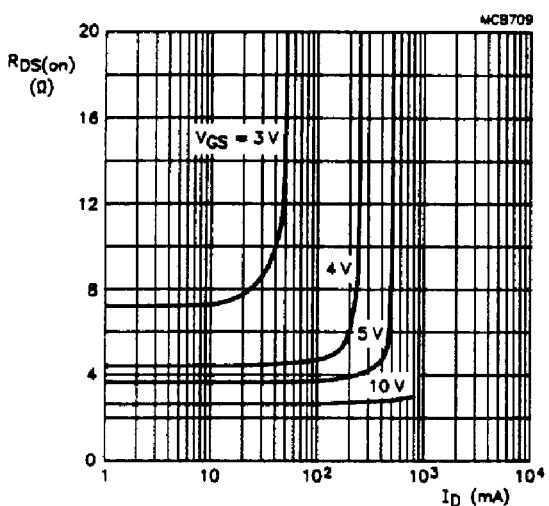


Fig.7 Typical on-resistance as a function of drain current; $T_j = 25\text{ }^\circ\text{C}$.

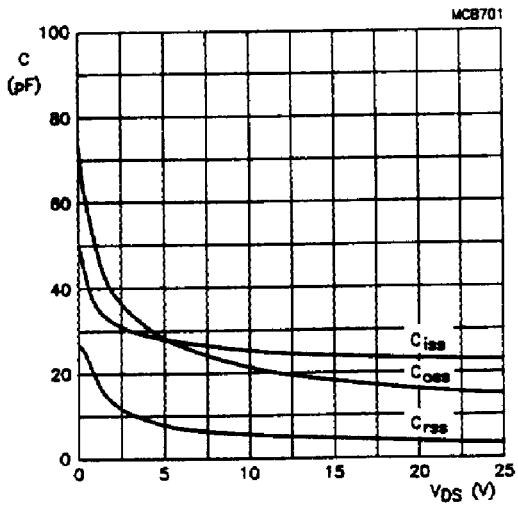


Fig.8 Typical capacitances as a function of drain-source voltage; $V_{GS} = 0$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^\circ\text{C}$.

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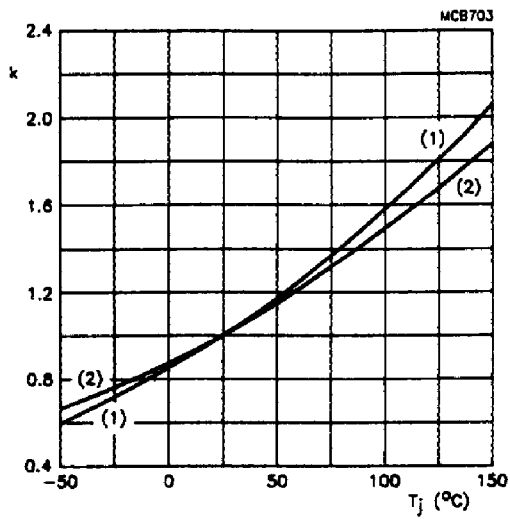


Fig.9 Temperature coefficient of drain-source on-resistance;

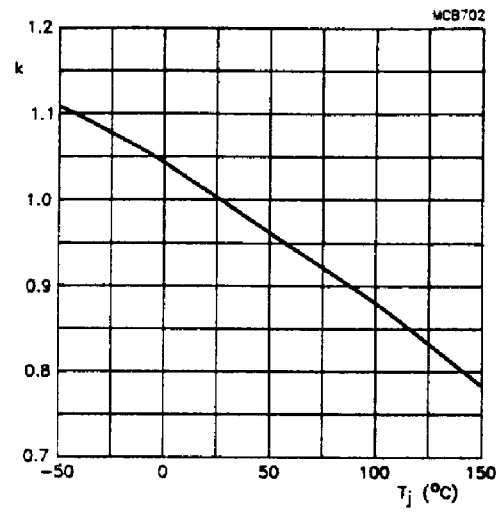


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25^\circ\text{C}}$$

typical $V_{GS(th)}$ at 1 mA.

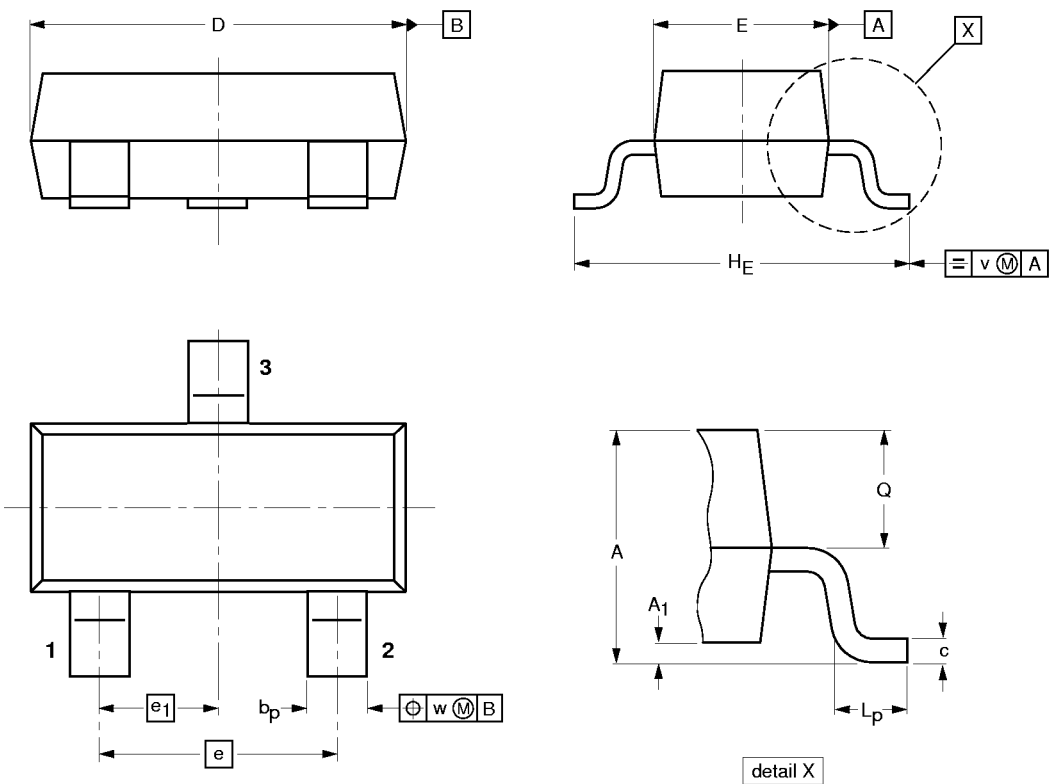
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PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28