**2SK1961**

N-Channel Junction Silicon FET

**High-Frequency Low-Noise
Amp Applications**
Applications

- High-frequency low-noise amp applications.

Features

- Adoption of FBET process
- Large $|y_{fs}|$
- Small C_{iss}
- Very low noise figure

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

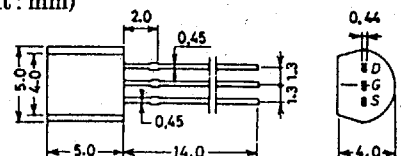
			unit
Drain to Source Voltage	V_{DSX}	15	V
Gate to Drain Voltage	V_{GDS}	-15	V
Gate Current	I_G	10	mA
Drain Current	I_D	100	mA
Allowable Power Dissipation	P_D	500	mW
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics at $T_a = 25^\circ\text{C}$

			min	typ	max	unit
G-D Breakdown Voltage	$V_{(BR)GDS}$	$I_G = -10\mu\text{A}, V_{DS} = 0$	-15			V
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = -10\text{V}, V_{DS} = 0$			-1.0	nA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 5\text{V}, I_D = 100\mu\text{A}$	-1.2	-2.6	-4.5	V
Drain Current	I_{DSS}	$V_{DS} = 5\text{V}, V_{GS} = 0$	40※		75※	mA
Forward Transfer Admittance	$ y_{fs} (1)$	$V_{DS} = 5\text{V}, I_D = 10\text{mA}, f = 1\text{kHz}$	15	19		mS
	$ y_{fs} (2)$	$V_{DS} = 5\text{V}, V_{GS} = 0, f = 1\text{kHz}$	24	32		mS
Input Capacitance	C_{iss}	$V_{DS} = 5\text{V}, V_{GS} = 0, f = 1\text{MHz}$		5.5		pF
Reverse Transfer Capacitance	C_{rss}	$V_{DS} = 5\text{V}, V_{GS} = 0, f = 1\text{MHz}$		1.6		pF
Noise Figure	NF	$V_{DS} = 5\text{V}, R_g = 1\text{k}\Omega, I_D = 5\text{mA}, f = 1\text{kHz}$		1.3		dB
Static Drain to Source on State Resistance	$R_{DS(on)}$	$I_D = 10\text{mA}, V_{GS} = 0$		24		Ω

 ※ : The 2SK1961 is classified by I_{DSS} as follows (unit : mA)

40	Y3	52	48	Y4	63	57	Y5	75
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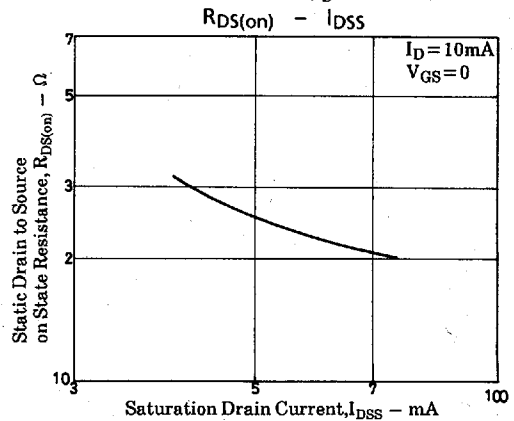
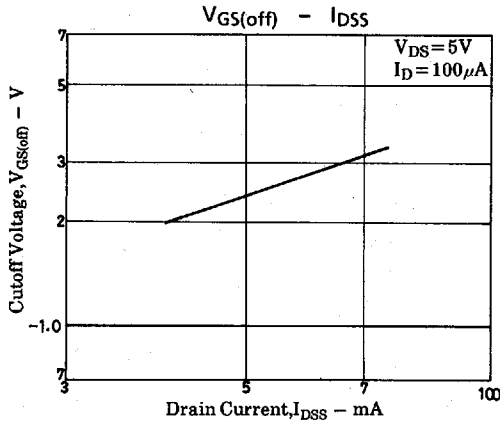
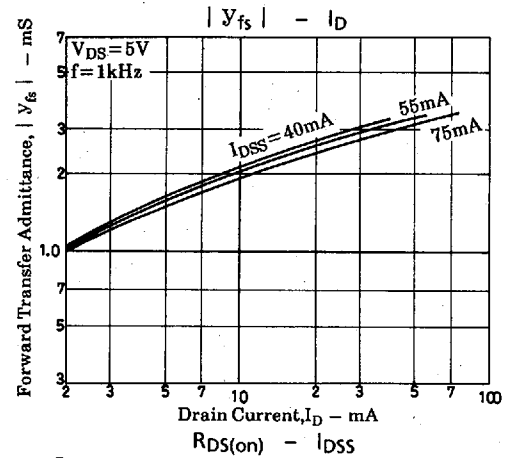
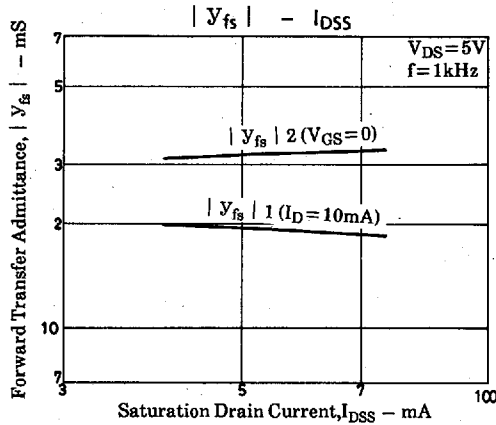
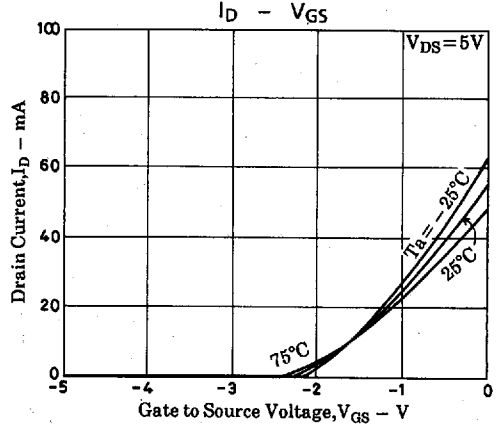
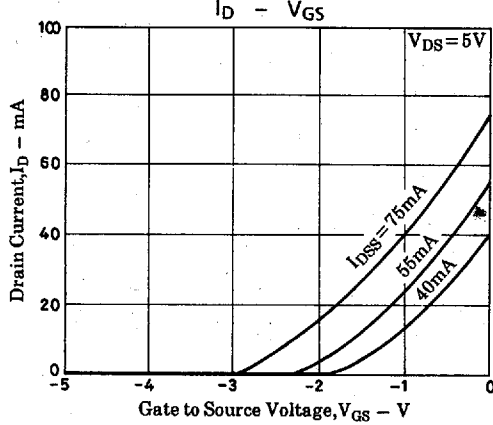
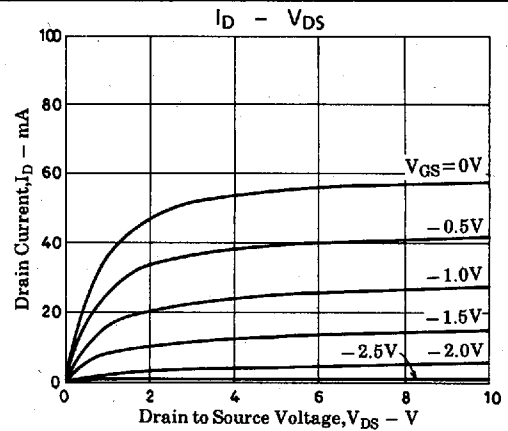
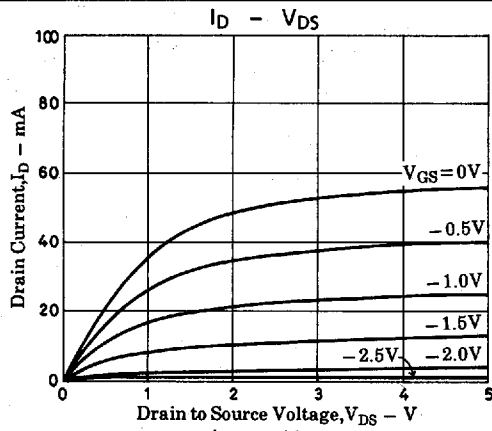
Case Outline 2019A
 (unit : mm)

 JEDEC: TO-92
 EIAJ: SC-43
 SANYO: NP

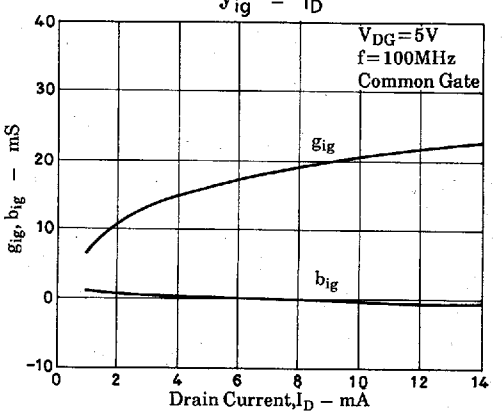
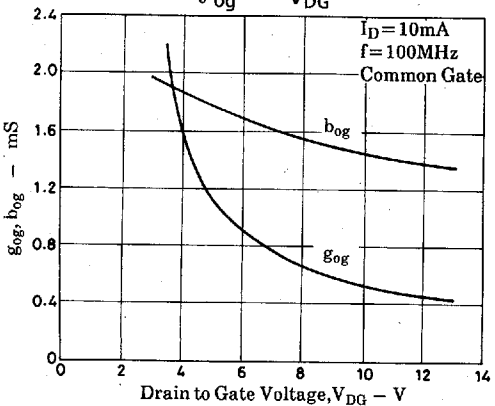
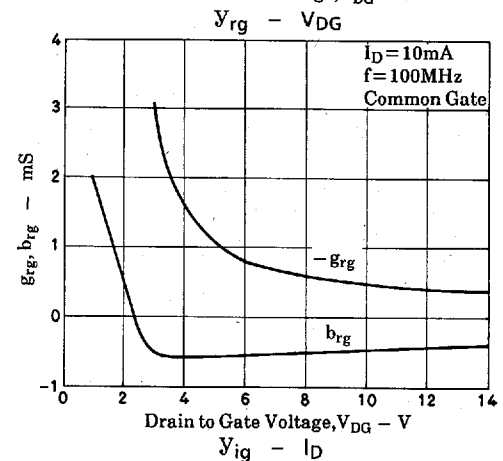
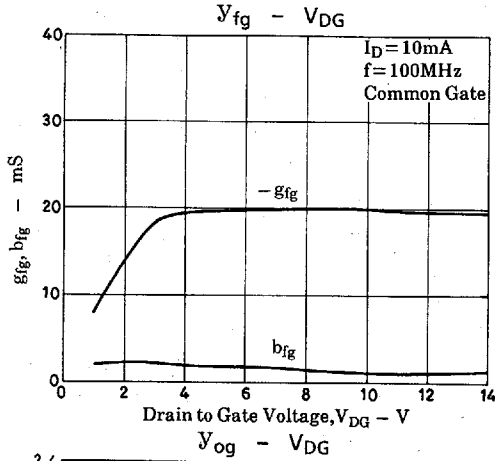
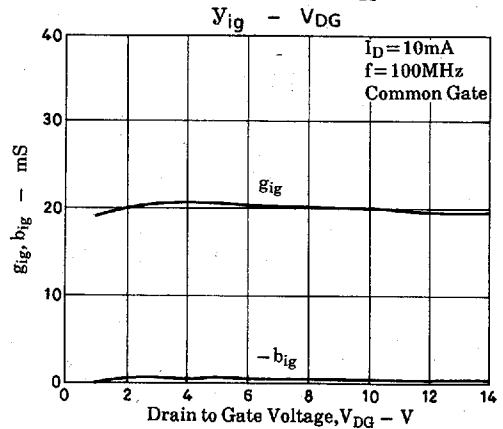
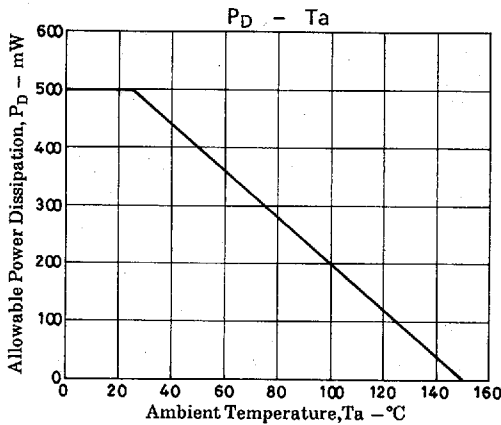
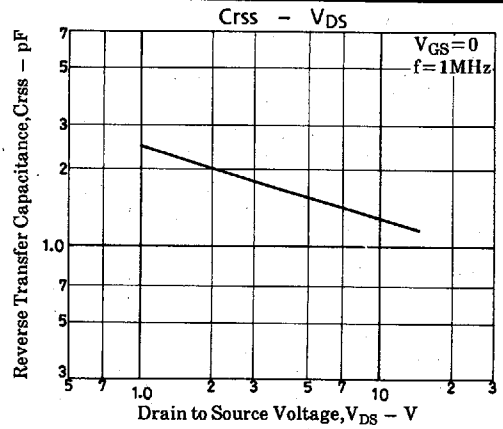
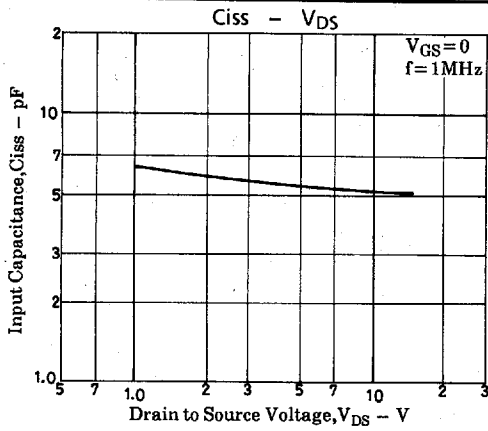
 D: Drain
 G: Gate
 S: Source

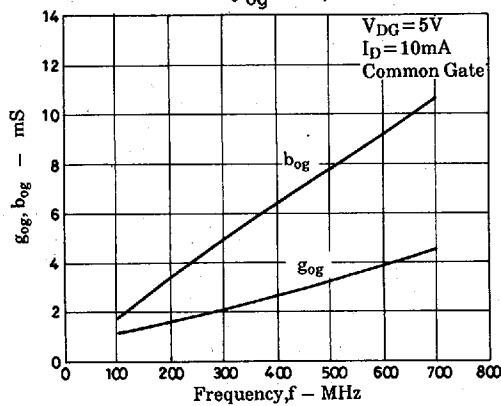
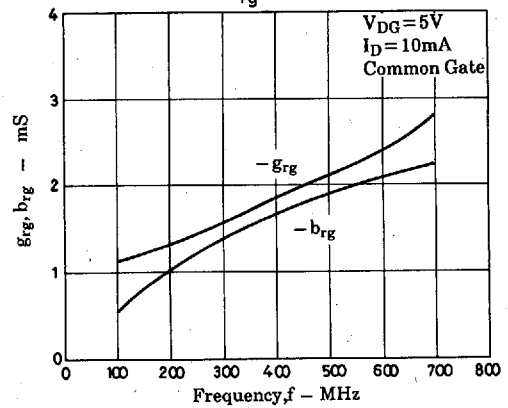
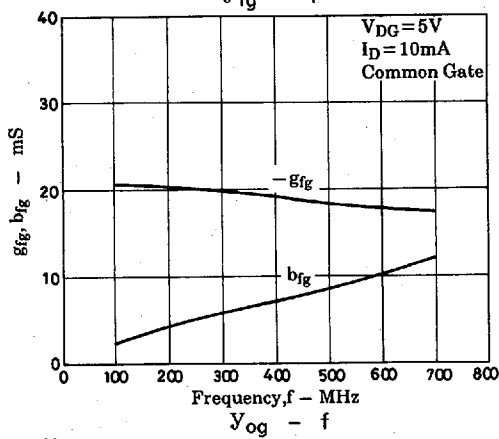
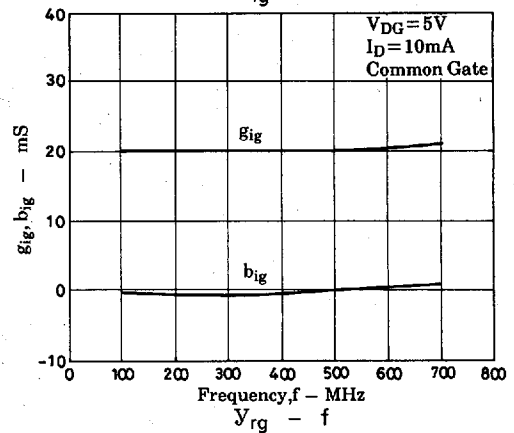
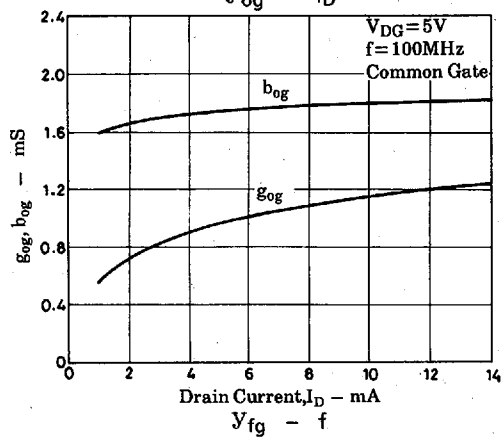
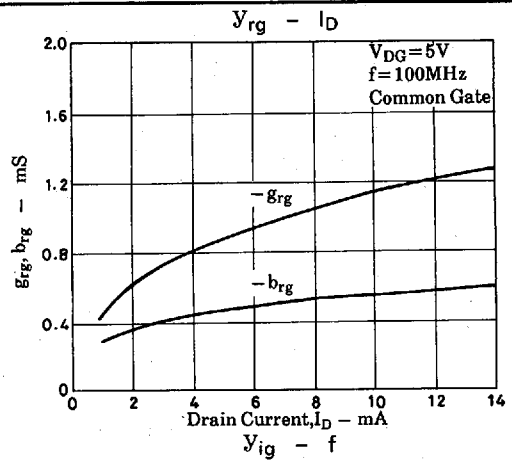
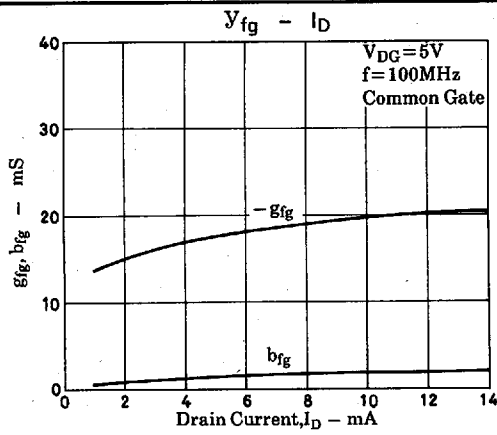
Specifications and information herein are subject to change without notice.

SANYO Electric Co., Ltd. Semiconductor Business Headquarters

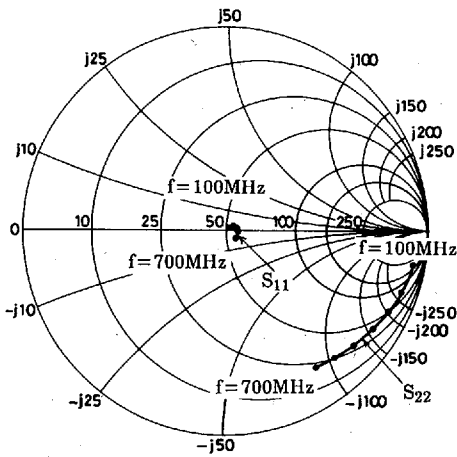
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN



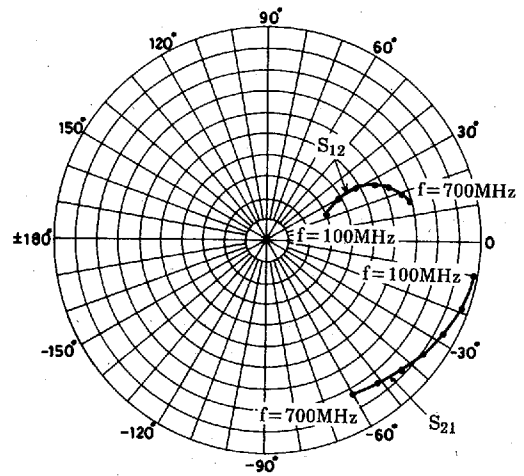




S Parameter Frequency Characteristic

(Common Gate) ($V_{DG}=5V, I_D=10mA$)

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(Common Gate) ($V_{DG}=5V, I_D=10mA$)

S Parameter (Common Gate)

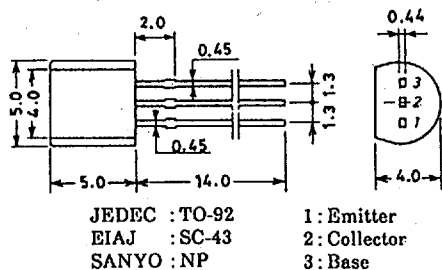
 $V_{DG}=5V, I_D=10mA, Z_0=50\Omega$

Freq (MHz)	$ S_{11} $	$\angle S_{11}$	$ S_{21} $	$\angle S_{21}$	$ S_{12} $	$\angle S_{12}$	$ S_{22} $	$\angle S_{22}$
100	0.024	54.7	0.985	-9.7	0.059	21.9	0.942	-9.0
200	0.038	48.5	0.963	-18.8	0.078	30.1	0.918	-17.3
300	0.054	32.4	0.932	-27.3	0.097	30.2	0.896	-25.4
400	0.055	20.5	0.903	-35.4	0.113	27.3	0.870	-33.0
500	0.060	1.8	0.875	-43.6	0.124	23.4	0.847	-40.5
600	0.055	-19.1	0.849	-51.4	0.132	19.0	0.826	-48.2
700	0.053	-41.6	0.826	-60.1	0.137	15.0	0.811	-56.0

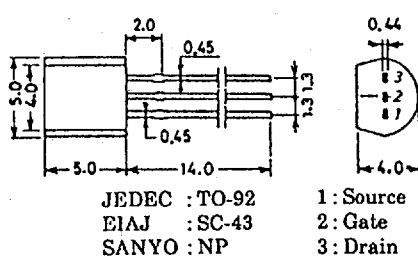
CASE OUTLINES OF LEAD FORMED SMALL SIGNAL TRANSISTORS

- All of Sanyo lead formed small signal transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

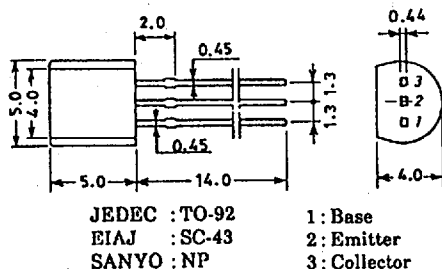
Case Outline 2003A/2003B (unit : mm)



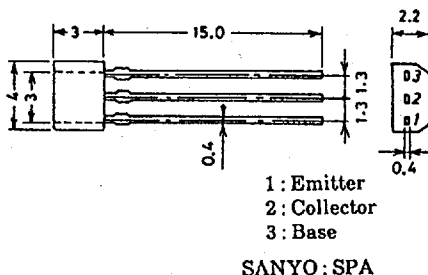
Case Outline 2019A/2019B (unit : mm)



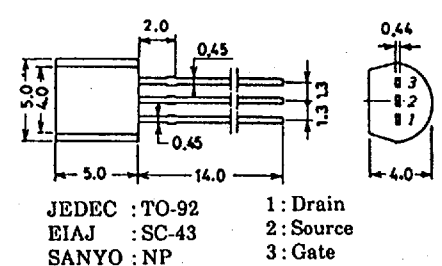
Case Outline 2004A (unit : mm)



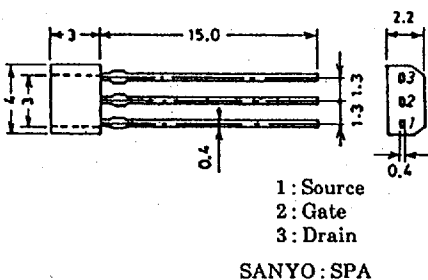
Case Outline 2033 (unit : mm)



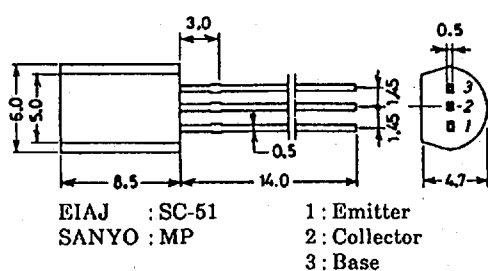
Case Outline 2005A (unit : mm)



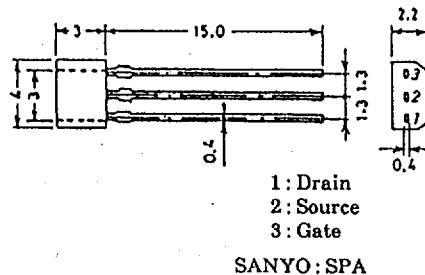
Case Outline 2034/2034A (unit : mm)



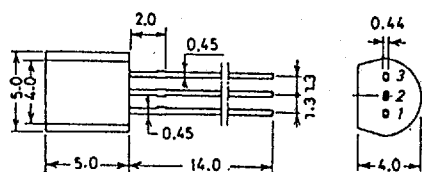
Case Outline 2006A (unit : mm)



Case Outline 2040 (unit : mm)



Case Outline 2061 (unit : mm)



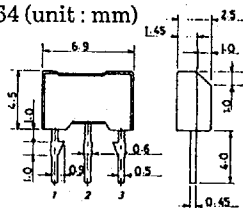
JEDEC : TO-92

EIAJ : SC-43

SANYO : NP

- 1: Emitter
- 2: Base
- 3: Collector

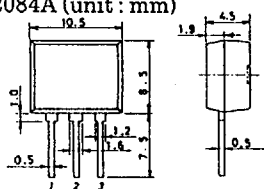
Case Outline 2064 (unit : mm)



- 1: Emitter
- 2: Collector
- 3: Base

SANYO : NMP

Case Outline 2084A (unit : mm)



- 1: Emitter
- 2: Collector
- 3: Base

SANYO : FLIP