2SK2553(L), 2SK2553(S)

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

ADE-208-357H (Z)
9th. Edition
Feb. 1999

Application

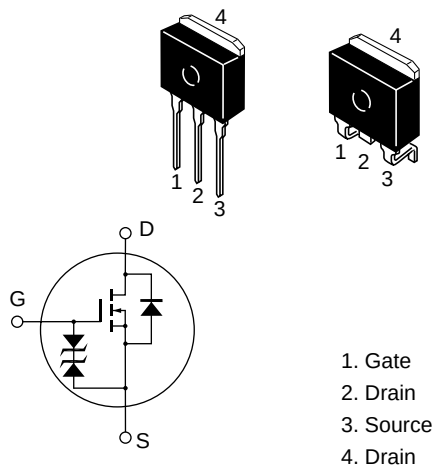
High speed power switching

Features

- Low on-resistance
- $R_{DS(on)}$ = 7 mΩ typ.
- High speed switching
- 4 V gate drive device can be driven from 5 V source

Outline

LDPAK



1. Gate
2. Drain
3. Source
4. Drain

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$ Note 1	200	A
Body to drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP} Note 3	45	A
Avalanche energy	E_{AR} Note 3	174	mJ
Channel dissipation	Pch Note 2	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes 1. PW ≤ 10 μs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

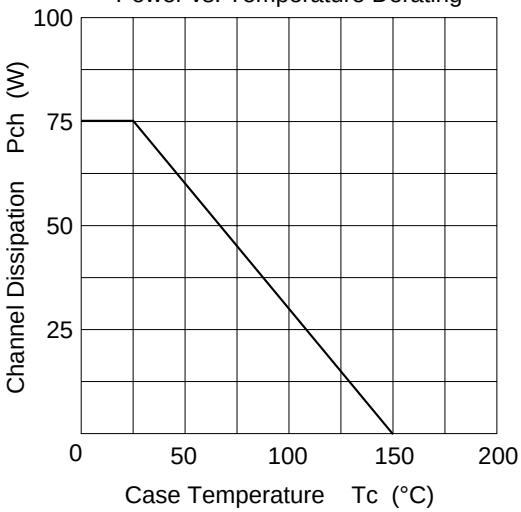
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	7	10	mΩ	I_D = 25 A V_{GS} = 10 V Note 1
		—	10	16	mΩ	I_D = 25 A V_{GS} = 4 V Note 1
Forward transfer admittance	$\|y_{fs}\|$	35	55	—	S	I_D = 25 A V_{DS} = 10 V Note 1
Input capacitance	Ciss	—	3550	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1760	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	500	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	35	—	ns	I_D = 25 A
Rise time	t_r	—	230	—	ns	V_{GS} = 10 V
Turn-off delay time	$t_{d(off)}$	—	470	—	ns	R_L = 1.2 Ω
Fall time	t_f	—	360	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.85	—	V	I_F = 50 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	135	—	ns	I_F = 50 A, V_{GS} = 0 di_F / dt = 50 A / µs

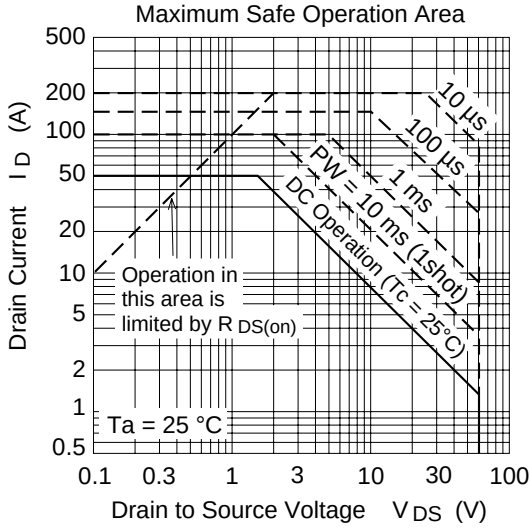
Note 1. Pulse Test

See characteristic curves of 2SK2529.

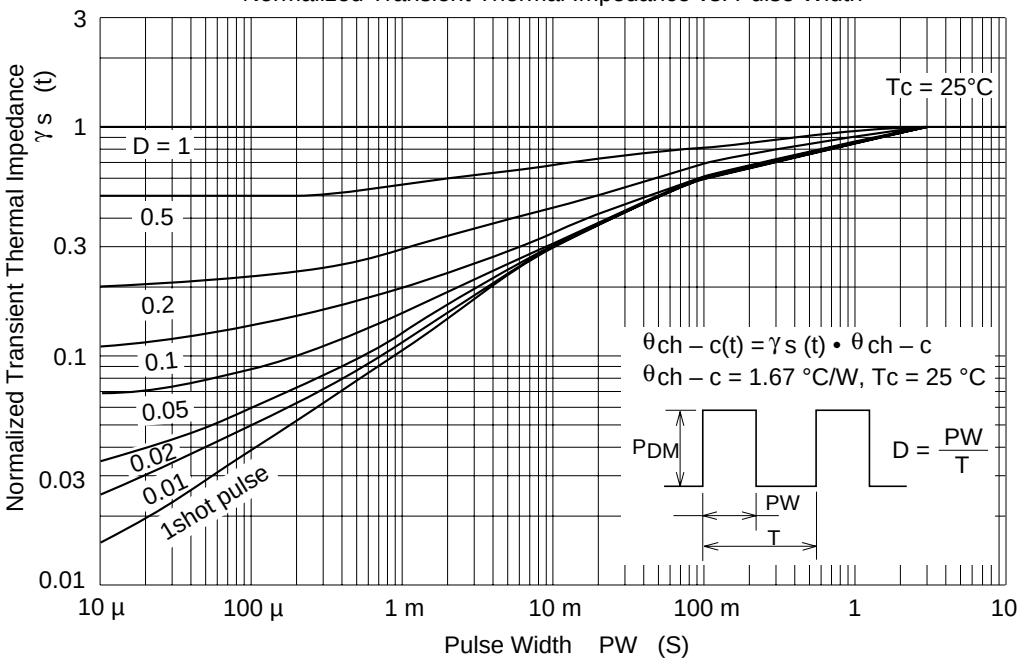
Power vs. Temperature Derating



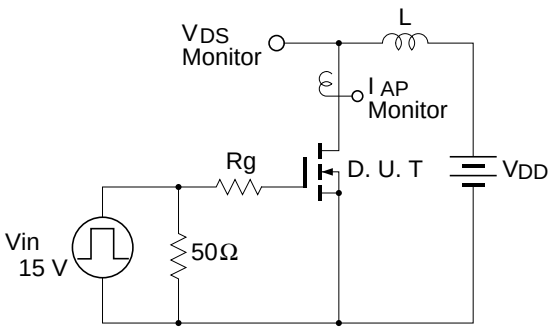
Maximum Safe Operation Area



Normalized Transient Thermal Impedance vs. Pulse Width

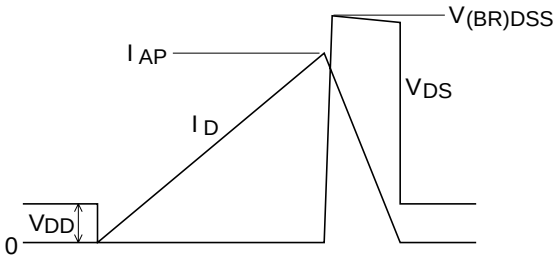


Avalanche Test Circuit

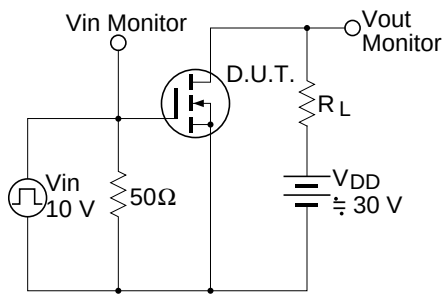


Avalanche Waveform

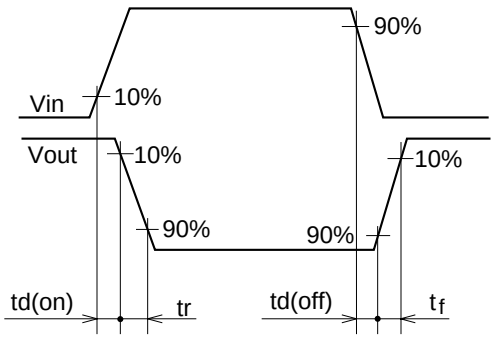
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



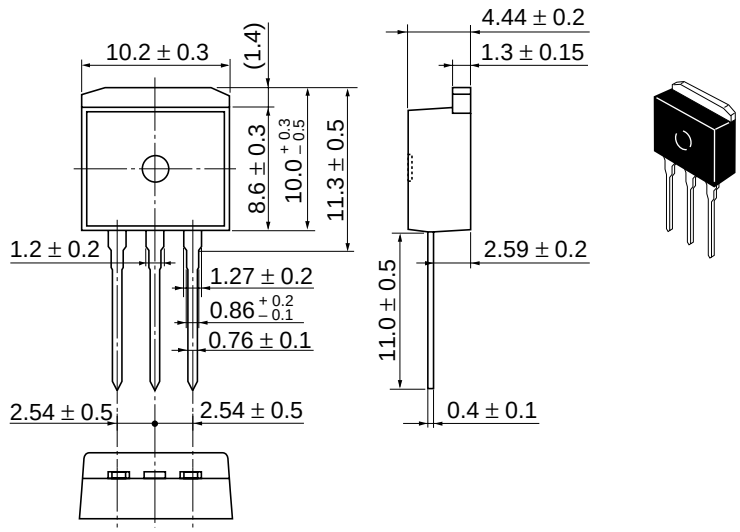
Waveform



Package Dimensions

As of January, 2001

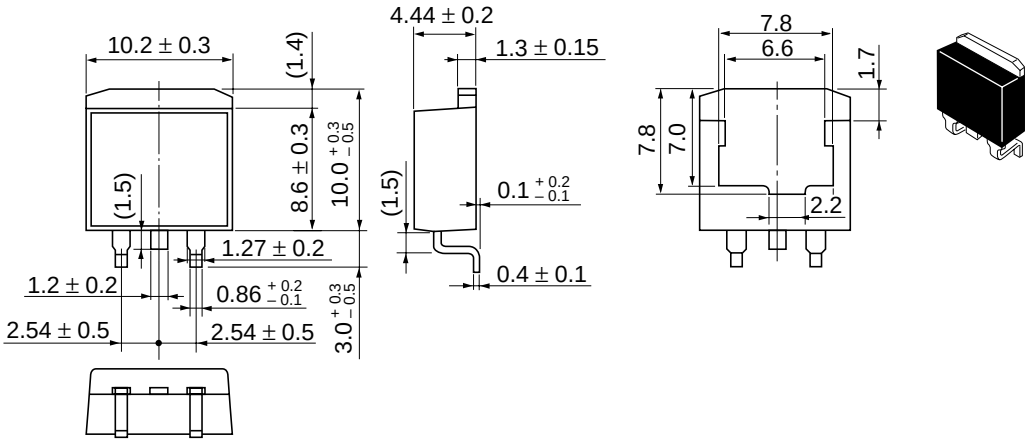
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
EIAJ	—
Mass (reference value)	1.4 g

As of January, 2001

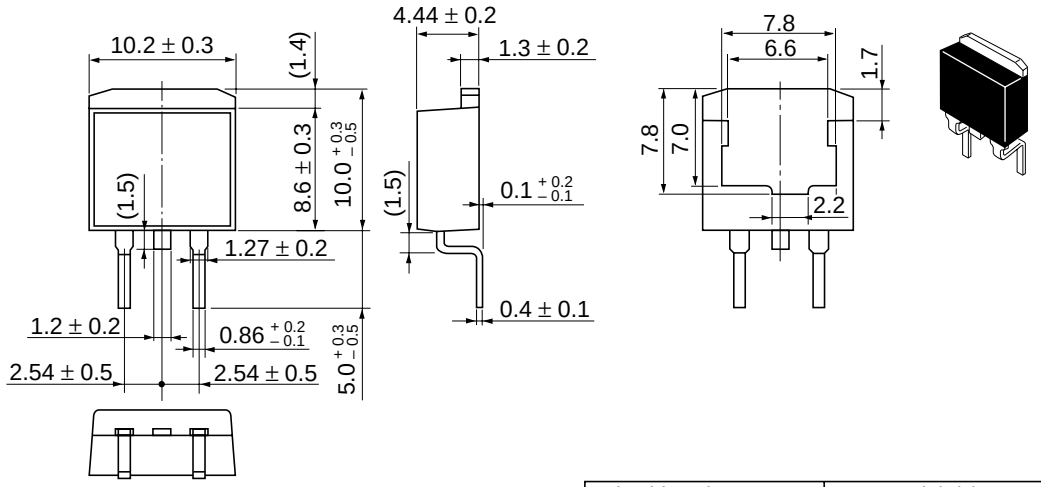
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
EIAJ	—
Mass (reference value)	1.3 g

As of January, 2001

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	1.35 g

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