

# 2SK3134(L), 2SK3134(S)

Silicon N Channel MOS FET  
High Speed Power Switching

## HITACHI

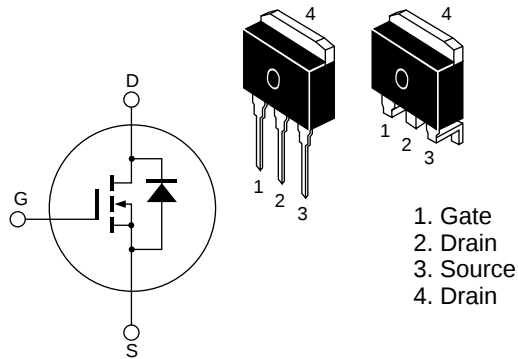
ADE-208-721B (Z)  
3rd. Edition  
Feb. 1999

### Features

- Low on-resistance  
 $R_{DS(on)} = 4m\Omega$  typ.
- Low drive current
- 4V gate drive device can be driven from 5V source

### Outline

LDBPAK



Absolute Maximum Ratings (Ta = 25°C)

| Item                                   | Symbol                           | Ratings     | Unit |
|----------------------------------------|----------------------------------|-------------|------|
| Drain to source voltage                | $V_{DSS}$                        | 30          | V    |
| Gate to source voltage                 | $V_{GSS}$                        | ±20         | V    |
| Drain current                          | $I_D$                            | 75          | A    |
| Drain peak current                     | $I_{D(pulse)}$ <sup>Note 1</sup> | 300         | A    |
| Body-drain diode reverse drain current | $I_{DR}$                         | 75          | A    |
| Avalanche current                      | $I_{AP}$ <sup>Note 3</sup>       | 35          | A    |
| Avalanche energy                       | $E_{AR}$ <sup>Note 3</sup>       | 122         | mJ   |
| Channel dissipation                    | $P_{ch}$ <sup>Note 2</sup>       | 100         | W    |
| Channel temperature                    | Tch                              | 150         | °C   |
| Storage temperature                    | Tstg                             | −55 to +150 | °C   |

Note: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$   
2. Value at Tc = 25°C  
3. Value at Tch = 25°C, Rg  $\geq 50\Omega$

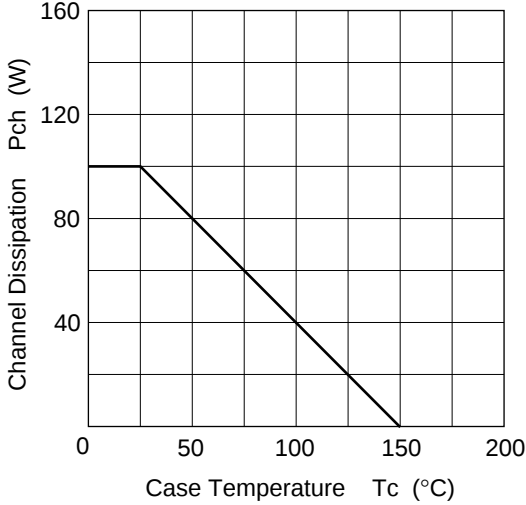
**Electrical Characteristics** (Ta = 25°C)

| Item                                       | Symbol        | Min | Typ  | Max       | Unit             | Test Conditions                                                         |
|--------------------------------------------|---------------|-----|------|-----------|------------------|-------------------------------------------------------------------------|
| Drain to source breakdown voltage          | $V_{(BR)DSS}$ | 30  | —    | —         | V                | $I_D = 10\text{mA}$ , $V_{GS} = 0$                                      |
| Gate to source leak current                | $I_{GSS}$     | —   | —    | $\pm 0.1$ | $\mu\text{A}$    | $V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0$                                |
| Zero gate voltage drain current            | $I_{DSS}$     | —   | —    | 10        | $\mu\text{A}$    | $V_{DS} = 30\text{V}$ , $V_{GS} = 0$                                    |
| Gate to source cutoff voltage              | $V_{GS(off)}$ | 1.0 | —    | 2.5       | V                | $I_D = 1\text{mA}$ , $V_{DS} = 10\text{V}$ <sup>Note 1</sup>            |
| Static drain to source on state resistance | $R_{DS(on)}$  | —   | 4.0  | 5.0       | $\text{m}\Omega$ | $I_D = 40\text{A}$ , $V_{GS} = 10\text{V}$ <sup>Note 1</sup>            |
|                                            |               | —   | 5.5  | 8.5       | $\text{m}\Omega$ | $I_D = 40\text{A}$ , $V_{GS} = 4\text{V}$ <sup>Note 1</sup>             |
| Forward transfer admittance                | $ y_{fs} $    | 50  | 80   | —         | S                | $I_D = 40\text{A}$ , $V_{DS} = 10\text{V}$ <sup>Note 1</sup>            |
| Input capacitance                          | $C_{iss}$     | —   | 6800 | —         | pF               | $V_{DS} = 10\text{V}$                                                   |
| Output capacitance                         | $C_{oss}$     | —   | 1550 | —         | pF               | $V_{GS} = 0$                                                            |
| Reverse transfer capacitance               | $C_{rss}$     | —   | 500  | —         | pF               | $f = 1\text{MHz}$                                                       |
| Total gate charge                          | $Q_g$         | —   | 130  | —         | nc               | $V_{DD} = 10\text{V}$                                                   |
| Gate to source charge                      | $Q_{gs}$      | —   | 16   | —         | nc               | $V_{GS} = 10\text{V}$                                                   |
| Gate to drain charge                       | $Q_{gd}$      | —   | 30   | —         | nc               | $I_D = 75\text{A}$                                                      |
| Turn-on delay time                         | $t_{d(on)}$   | —   | 50   | —         | ns               | $V_{GS} = 10\text{V}$ , $I_D = 40\text{A}$                              |
| Rise time                                  | $t_r$         | —   | 370  | —         | ns               | $R_L = 0.25\Omega$                                                      |
| Turn-off delay time                        | $t_{d(off)}$  | —   | 550  | —         | ns               |                                                                         |
| Fall time                                  | $t_f$         | —   | 380  | —         | ns               |                                                                         |
| Body-drain diode forward voltage           | $V_{DF}$      | —   | 1.05 | —         | V                | $I_F = 75\text{A}$ , $V_{GS} = 0$                                       |
| Body-drain diode reverse recovery time     | $t_{rr}$      | —   | 80   | —         | ns               | $I_F = 75\text{A}$ , $V_{GS} = 0$<br>$di_F/dt = 50\text{A}/\mu\text{s}$ |

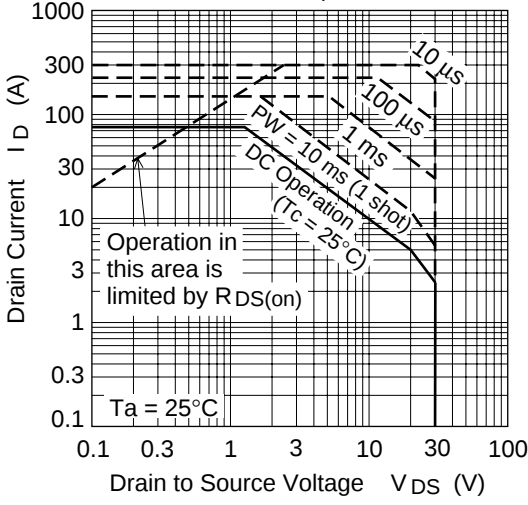
Note: 1. Pulse test

Main Characteristics

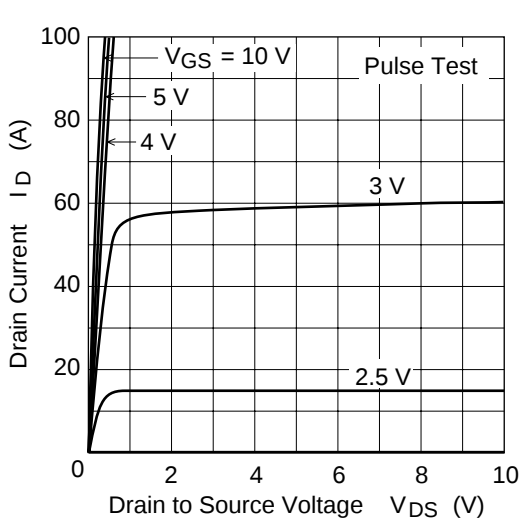
Power vs. Temperature Derating



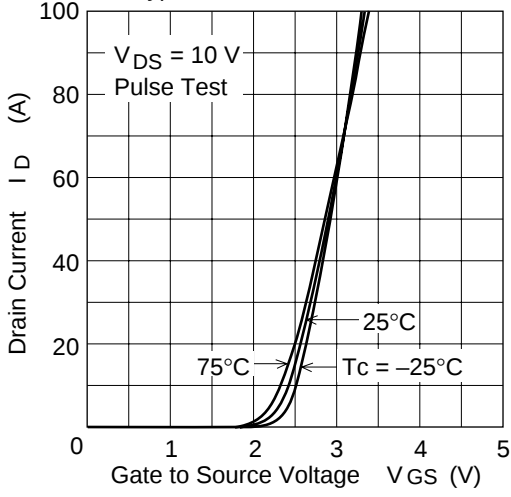
Maximum Safe Operation Area

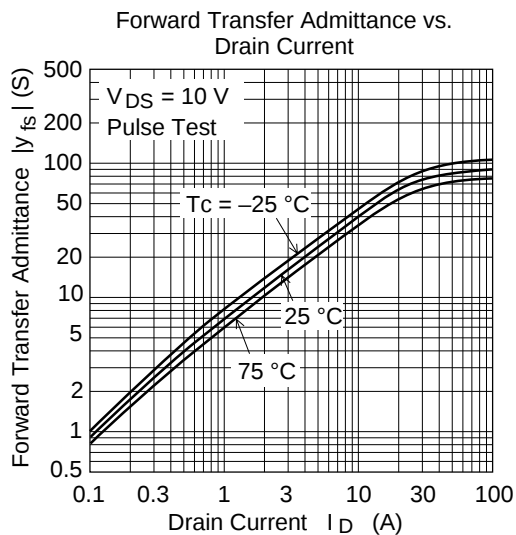
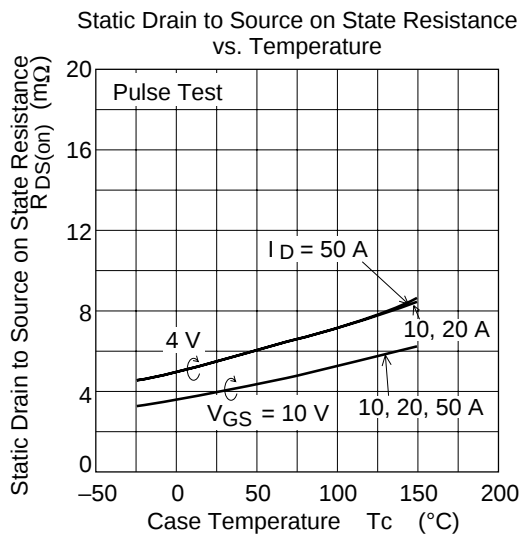
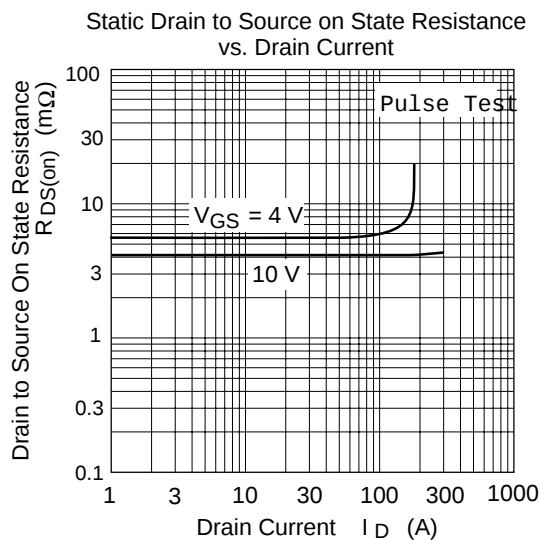
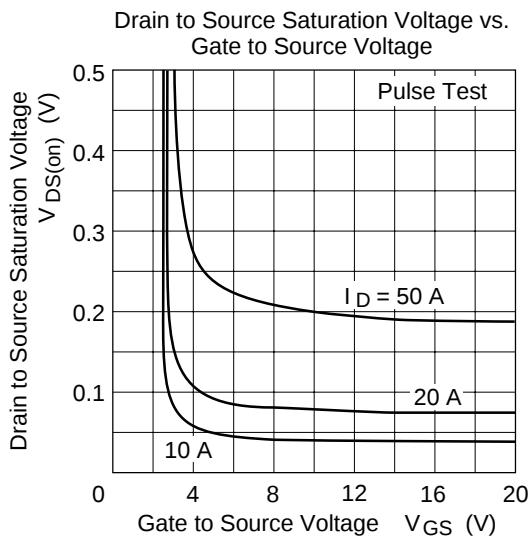


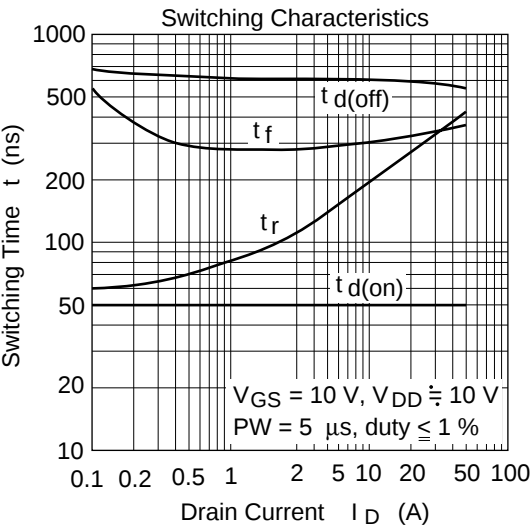
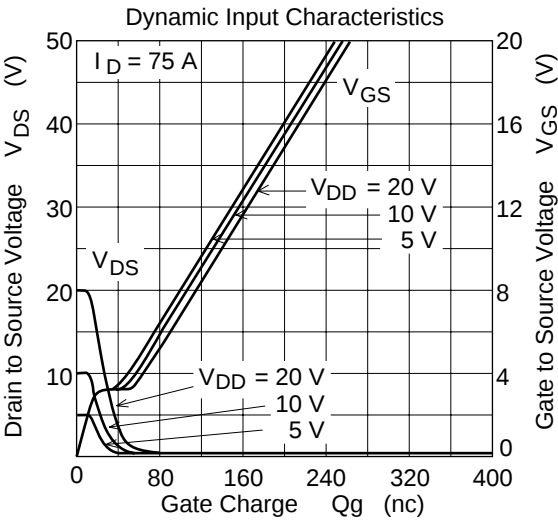
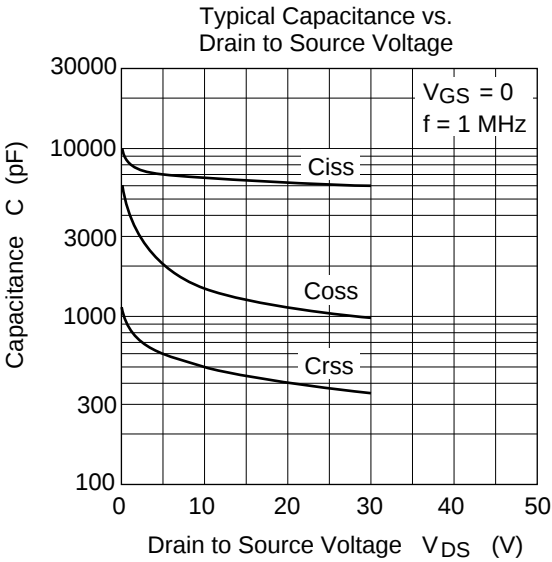
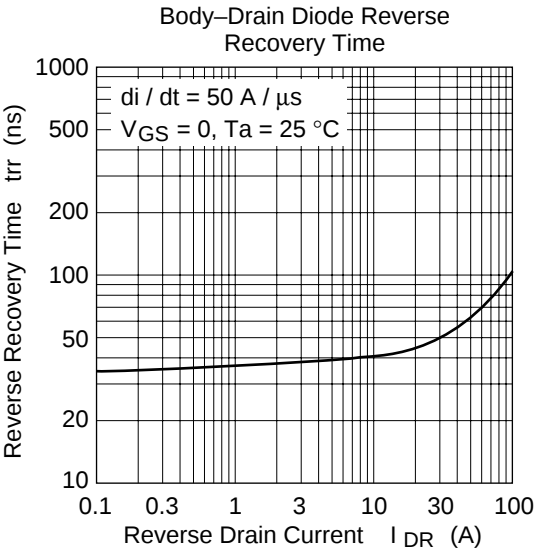
Typical Output Characteristics

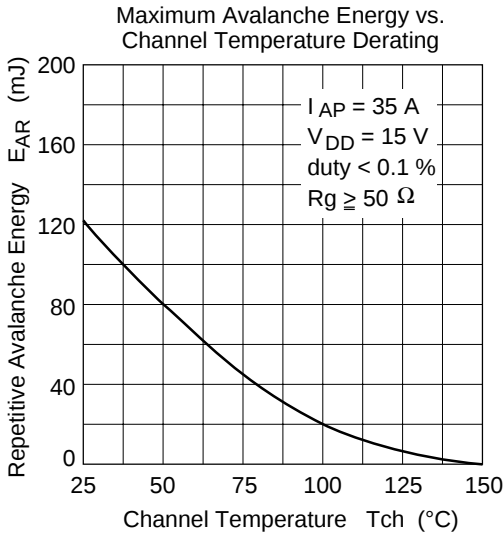
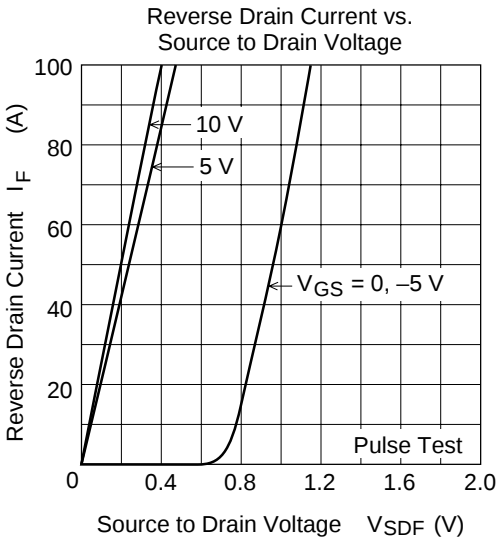


Typical Transfer Characteristics

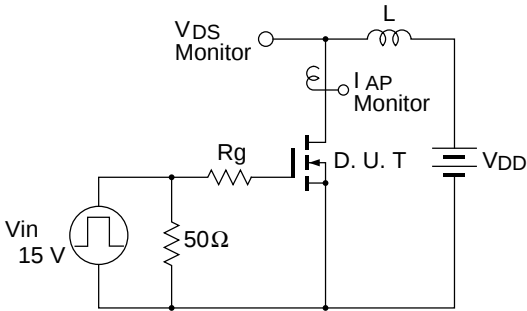






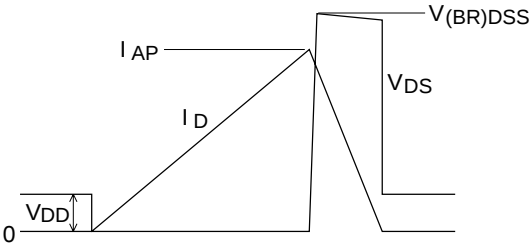


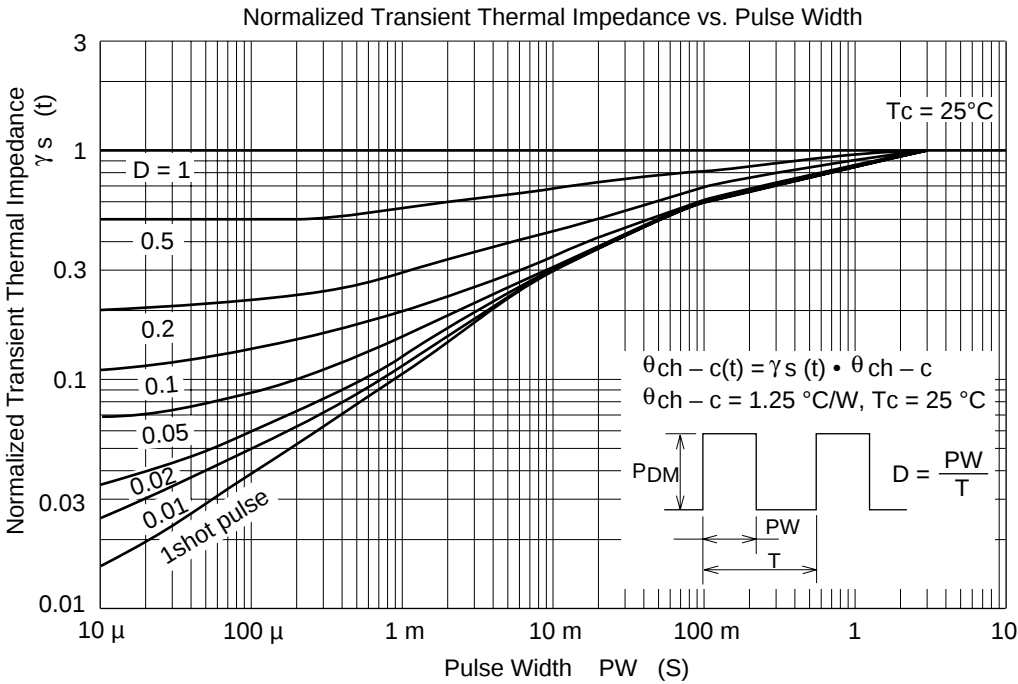
Avalanche Test Circuit



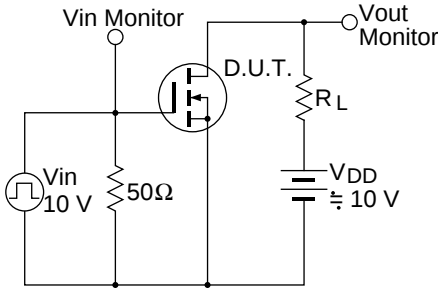
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

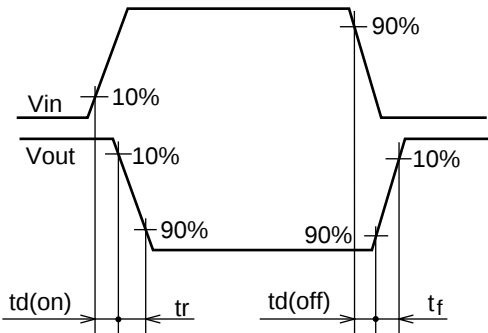




Switching Time Test Circuit

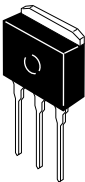
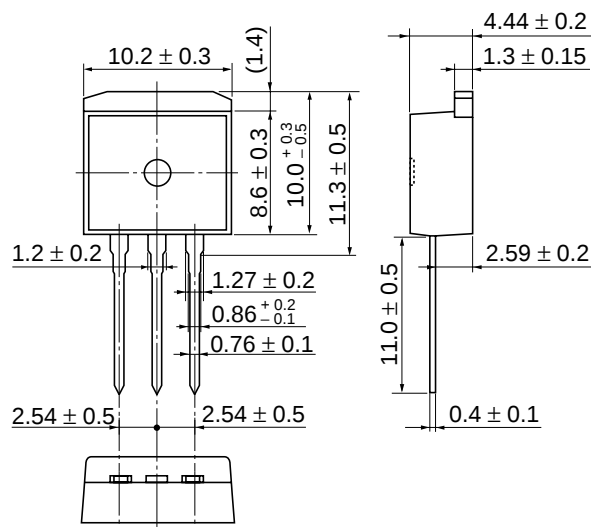


Waveform



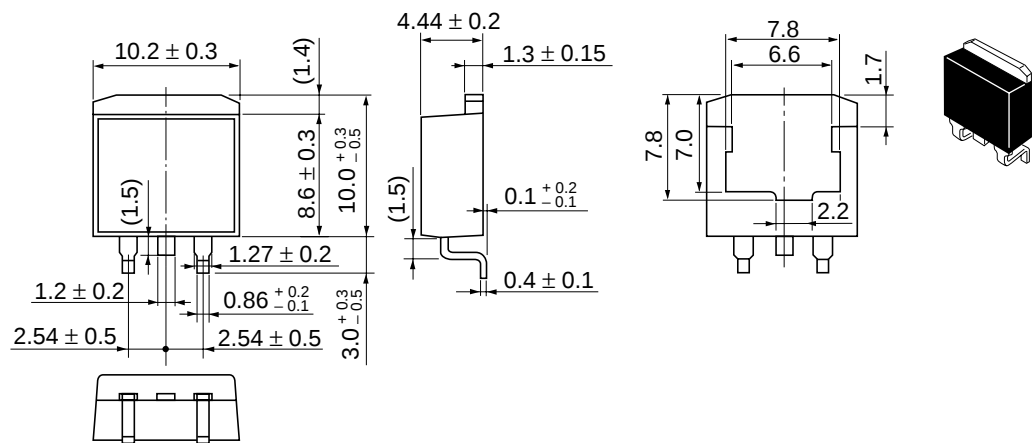
Package Dimensions

As of January, 2001  
Unit: mm



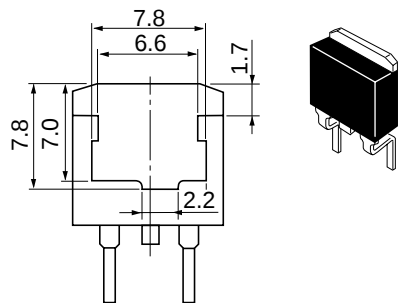
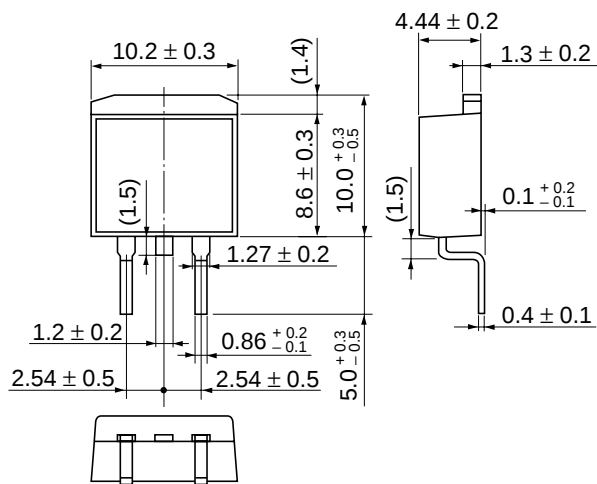
|                        |           |
|------------------------|-----------|
| Hitachi Code           | LDPAK (L) |
| JEDEC                  | —         |
| EIAJ                   | —         |
| Mass (reference value) | 1.4 g     |

As of January, 2001  
Unit: mm



|                        |               |
|------------------------|---------------|
| Hitachi Code           | LDBAK (S)-(1) |
| JEDEC                  | —             |
| EIAJ                   | —             |
| Mass (reference value) | 1.3 g         |

As of January, 2001  
Unit: mm



|                        |               |
|------------------------|---------------|
| Hitachi Code           | LDBAK (S)-(2) |
| JEDEC                  | —             |
| EIAJ                   | —             |
| Mass (reference value) | 1.35 g        |

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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

|     |              |                                                                                               |
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## For further information write to:

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|--------------------------------------|-----------------------------|
| Hitachi Semiconductor (America) Inc. | Hitachi Europe GmbH         |
| 179 East Tasman Drive,               | Electronic Components Group |
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| Fax: <1> (408) 433-0223              | Germany                     |
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| Fax: <44> (1628) 585160           |

|                                                                        |
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| Singapore 049318                                                       |
| Tel: <65>-538-6533/538-8577                                            |
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