



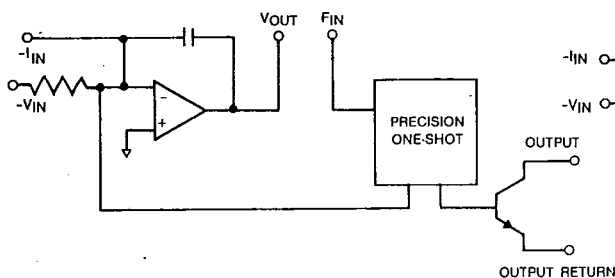
MODELS 3815, 3816, AND 3817 LOW COST, GENERAL PURPOSE V/F/V CONVERTERS

These are self-contained voltage-to-frequency converters, requiring no external components. Compared to typical V/F conversion systems assembled from monolithic V/F functions and additional components, they provide much better performance, with the ease and reliability of working with a single unit...often at lower cost and in less overall space.

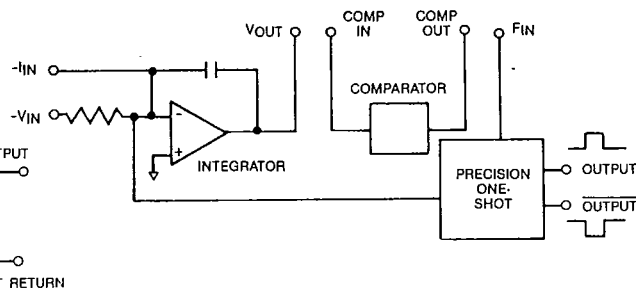
- V/F and F/V operating modes
- Single-supply operation (V/F mode)
- Max. non-linearities down to 0.005%
- Three full-scale frequency ranges:
10 KHz - Model 3815
25 KHz - Model 3816
100 KHz - Model 3817
- Open collector, CMOS/TTL-compatible outputs (10 KHz, 25 KHz)
- Complementary CMOS output (100 KHz)
- Standard 14-pin hybrid package

BLOCK DIAGRAMS

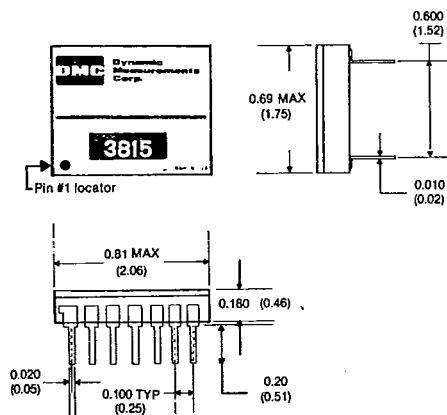
MODELS 3815 AND 3816



MODEL 3817



MECHANICAL DATA



PIN ASSIGNMENTS

MODELS 3815 & 3816			
PIN	FUNCTION	PIN	FUNCTION
1	NC	1	NC
2	-VS	2	-VS
3	IIN	3	IIN
4	VIN	4	VIN
5	VOUT	5	VOUT
6	FIN	6	COMP IN
7	NC	7	NC
8	OUTPUT	8	OUTPUT
9	OUTPUT RETURN	9	OUTPUT
10	NC	10	FIN
11	NC	11	COMP OUT
12	COMMON	12	COMMON
13	NC	13	NC
14	+VS	14	+VS

Dimensions are in Inches (cm) and tolerances are ± 0.01 (0.025), unless otherwise specified.

Dynamic Measurements Corp.

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PERFORMANCE SPECIFICATIONS

(At +25 °C, unless otherwise specified.)

PARAMETER GROUP	ITEM	SPECIFICATION						UNITS			
		MODELS 3815 AND 3816			MODEL 3817						
		MIN	TYP	MAX	MIN	TYP	MAX				
ANALOG INPUTS (V/I OPERATION)	Range Configuration	0 to -10	Single-Ended		0 to -10	Single-Ended		VDC			
	Full-Scale Voltage ¹	-9.5	-10	-10.5	-9.5	-10	-10.5	VDC			
	Full-Scale Current	126	133	140	126	133	140	uA			
	Overrange	+ 10%			+ 5%			Kohm			
	Input Impedance	70	75		70	75					
	Overvoltage Protection (without damage)			± V _S			± V _S				
DIGITAL INPUTS (F/V OPERATION)	Levels										
	Logic "1"	0.6	0.65	0.7	12V (CMOS-Compatible)			VDC			
	Logic "0"	-0.1	0	0.3	12V (CMOS-Compatible)			VDC			
	Pulse Width										
	3815	10	25	30				uSec			
	3816	5	12	15				uSec			
SCALING AND OUTPUT	3817				1	2.5	3	uSec			
	Polarity	Positive			Positive						
	Full-Scale Frequency										
	3815		10					KHz			
	3816		25			100		KHz			
	3817							KHz			
	Non-Linearity										
	3815		0.003%	0.005%							
	3816		0.005%	0.01%							
	3817					0.005%	0.015%				
	Output Pulse										
	3815	40	50	60				uSec			
	3816	15	20	30				uSec			
	3817				4	5	6	uSec			
	Transfer Characteristic										
	F _{OUT} vs. V _{IN} : 3815	10 x (V _{IN} /10V)			100 x (V _{IN} /10V)			KHz			
	3816	25 x (V _{IN} /10V)						KHz			
	3817							KHz			
	F _{OUT} vs. I _{IN} : 3815	10 x (I _{IN} /133uA)			100 x (I _{IN} /133uA)			KHz			
	3816	25 x (I _{IN} /133uA)						KHz			
	3817							KHz			
	Polarity	Negative			Complementary						
	Levels	Open Collector			12V (CMOS-Compatible)						
STABILITY	Gain TC (0 °C to 70 °C)		60	100		40	200	ppm/ °C			
	Offset TC (0 °C to 70 °C) ²		30	50		20	50	uV/ °C			
	PSRR: 3815, 3816		15	30				ppm/%			
	3817					0.005	0.01	%/%			
	Warm-Up Time (to 0.01%)		2			2		Minutes			
POWER REQUIREMENTS	Single-Supply Operation										
	+ V _S	14.5	15	25	14.5	15	20	VDC			
	+ I _S : 3815		7.9	10				mA			
	3816		8.2	10				mA			
	3817					10	14	mA			
	Dual Supply Operation										
	+ V _S	14.5	15	17	14.5	15	17	VDC			
	+ I _S		6.4	7.5		8.1	10	mA			
ENVIRONMENTAL	- V _S	-13	-15	-17	-13	-15	-17	VDC			
	- I _S		3	4		2.5	4	mA			
	Operating Temp. Range	0		+ 70	0		+ 70	°C			
	Storage Temp. Range	-25		+ 85	-25		+ 85	°C			

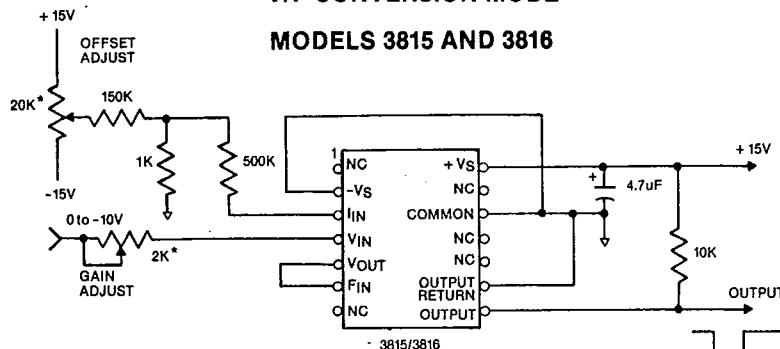
NOTES: 1. Specified with 1K resistor in series with V_{IN}. Trimmable to -10V.

2. Lower offset TC available in dual supply version. Please consult DMC.

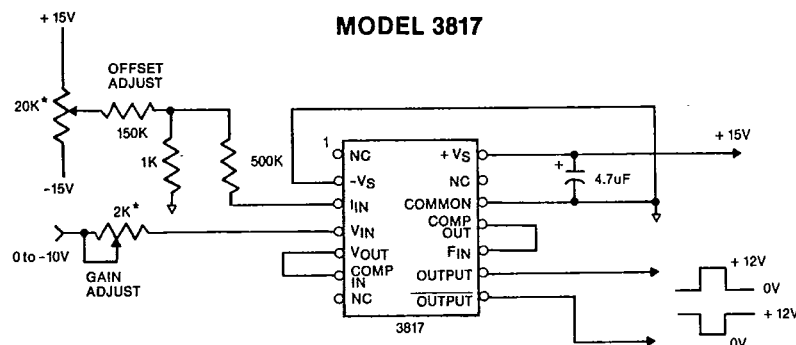
APPLICATION TECHNIQUES

V/I CONVERSION MODE

MODELS 3815 AND 3816

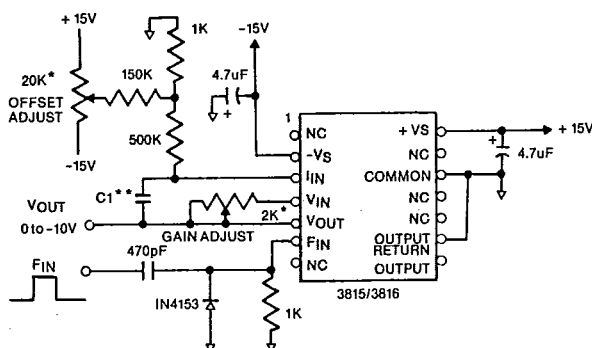


MODEL 3817

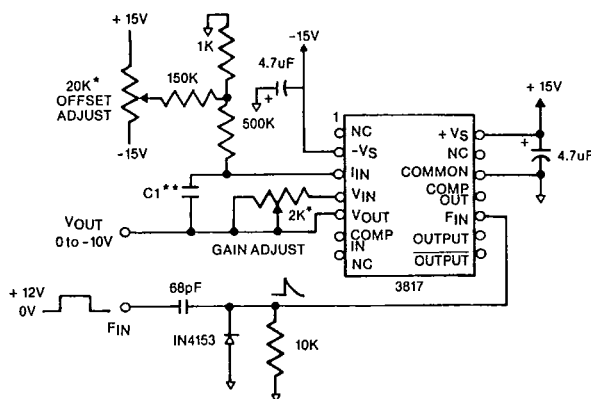


F/I CONVERSION MODE

MODELS 3815 AND 3816



MODEL 3817



* Stable, low TC 10T Potentiometer

* Capacitor C1 determines the amount of ripple and noise seen at the output. As step response and bandwidth are also a function of C1, care should be taken to calculate the value of C1 for the maximum amount of ripple that can be tolerated. This will ensure the best step response and bandwidth for the value of C. The formulas given below will give the worst case ripple (low frequency) for the selected value of C1. The graphs shown in Figures 1 and 2 may also be used to aid in the selection of C1.

10KHz Model 3815—

$$V_{\text{Ripple}} = \frac{14.5 \times 10^{-9}}{C + 0.027\mu\text{F}}$$

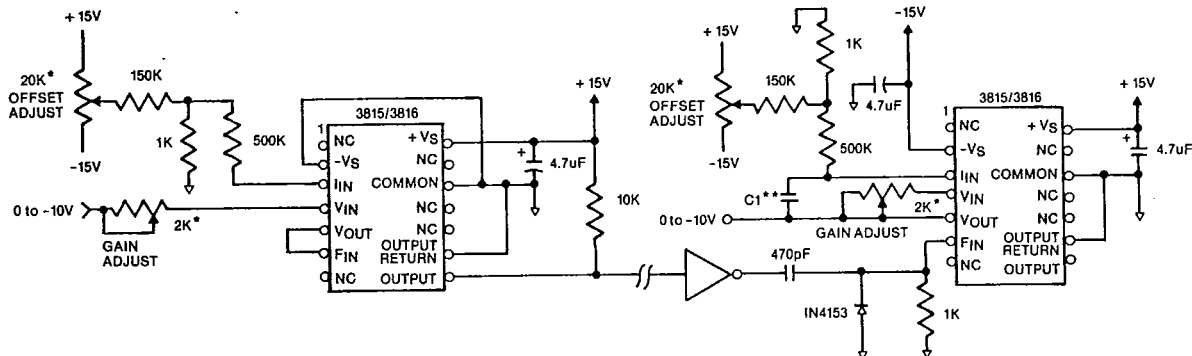
25KHz Model 3816

$$V_{\text{Ripple}} = \frac{7 \times 10^{-9}}{C + 0.015\mu\text{F}}$$

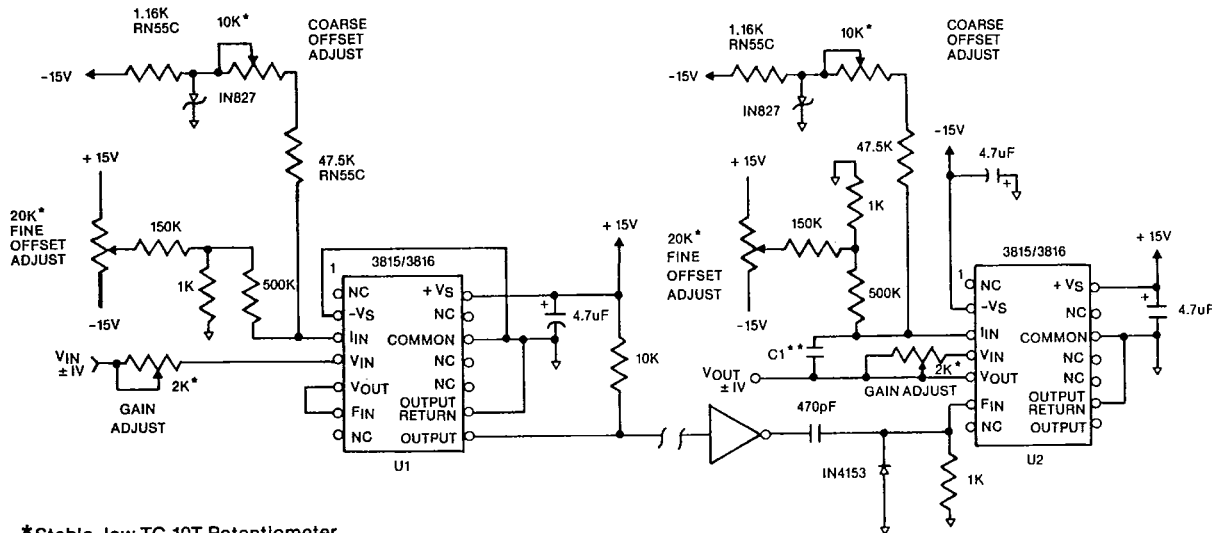
100KHz Model 3817

$$V_{\text{Ripple}} = \frac{1.4 \times 10^{-9}}{C1 + 0.0068\mu\text{F}}$$

0 TO -10V INPUT V/F - F/V LINK (UTILIZING MODEL 3815 OR 3816)



$\pm 1V$ INPUT V/F - F/V LINK (UTILIZING MODEL 3815 OR 3816)



* Stable, low TC 10T Potentiometer

** Capacitor C1 is determined by using the formula shown for F/V conversion and the graphs shown in Figures 1, 2 and 3.

OPERATION

U1 is trimmed for a symmetrical change about 9KHz (MODEL 3815) or 22.5KHz (MODEL 3816) by using the Fine and Coarse Offset Adjustments to calibrate the center frequency. The Gain Adjust is used to center the frequency swing about the center frequency when $\pm 1V$ is applied. When $\pm 1V$ is applied to the transmitter (U1), the Gain Adjust of U2 is used to adjust for a 2V change in output voltage. Next the Coarse and Fine Offset Adjustments of U2 are used to center the 2V swing about 0. This gives a $\pm 1V$ output of the receiver (U2) when $\pm 1V$ is applied to the transmitter (U1).

FIGURE 1

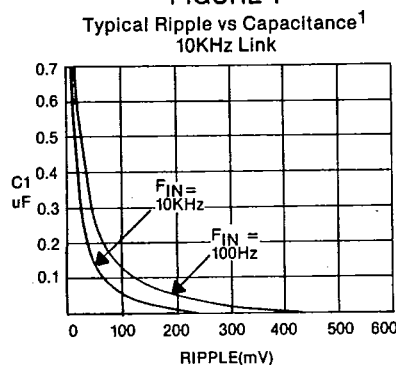


FIGURE 2

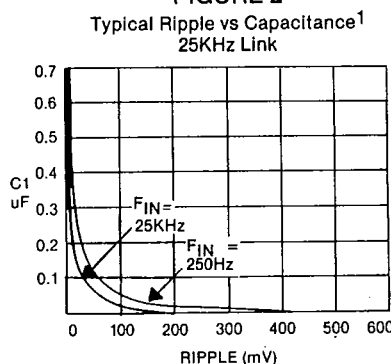
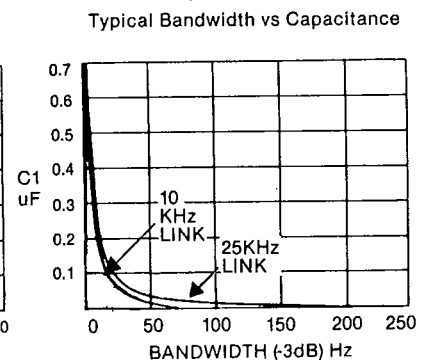
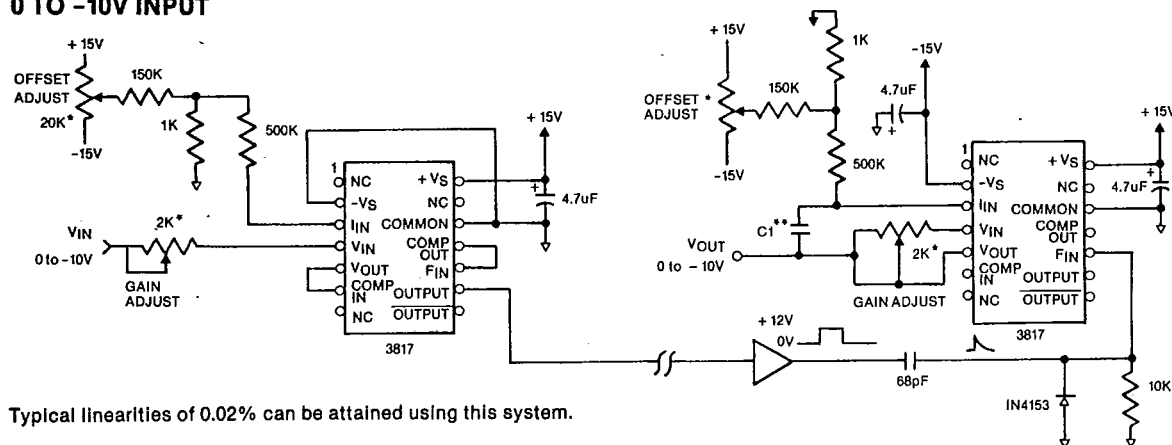


FIGURE 3



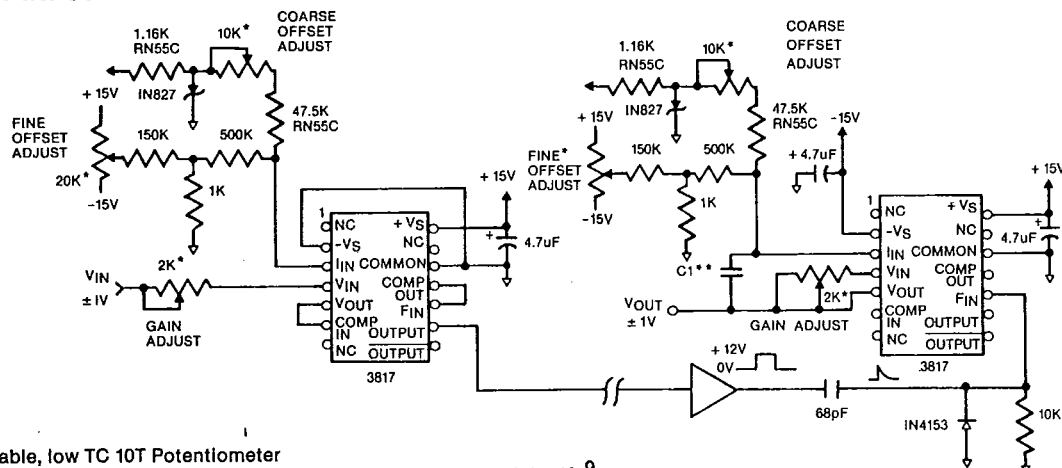
¹ The range of ripple for a given value of capacitor is determined by the input frequency. The largest amount of ripple is seen at low frequencies while the least amount is seen at the Full Scale frequency (10KHz or 25KHz).

**100KHz V/F - F/V LINK
0 TO -10V INPUT**



Typical linearities of 0.02% can be attained using this system.

**100KHz V/F - F/V LINK
± 1V INPUT**



*Stable, low TC 10T Potentiometer

**Capacitor C1 is determined using the formula $V_{\text{Ripple}} = \frac{1.4 \times 10^{-9}}{C1 + 0.0068\mu\text{F}}$ and the graphs shown in Figures 4 and 5.

FIGURE 4
Typical Ripple vs Capacitance¹
100Khz Link

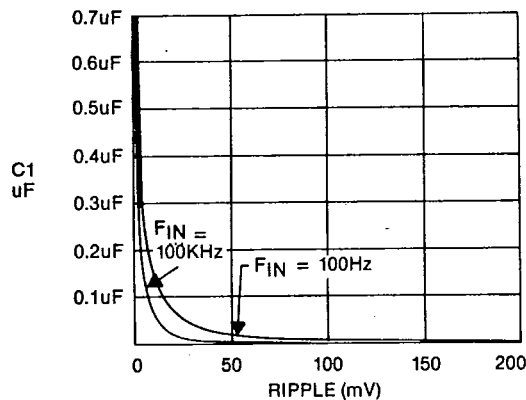
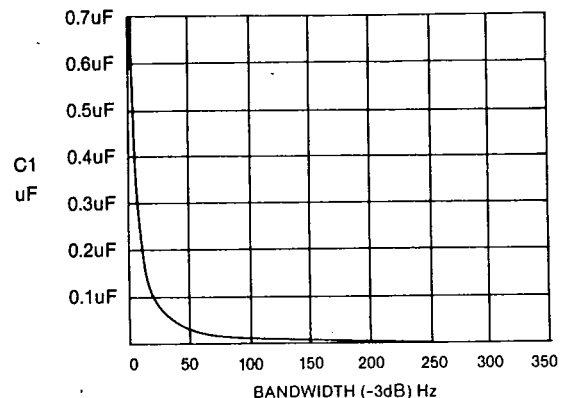


FIGURE 5
Typical Bandwidth vs Capacitance



¹ The range of ripple for a given value capacitor is determined by the input frequency. The largest amount of ripple is seen at low frequencies, while the least is seen at 100KHz.