HITACHI

3SK233

Silicon N Channel Dual Gate MOS FET
UHF TV Tuner RF Amplifier

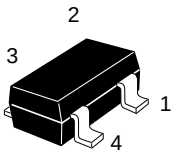
Feature

- Low voltage operation.
- Superior cross modulation characteristics.

Table 1 Absolute Maximum Ratings
(Ta = 25°C)

Item	Symbol	Rating	Unit
Drain to source voltage	V_{DS}	12	V
Gate 1 to source voltage	V_{G1S}	±10	V
Gate 2 to source voltage	V_{G2S}	±10	V
Drain current	I_D	35	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	125	°C
Storage temperature	Tstg	–55 to +125	°C

MPAK-4



1. Source
2. Gate 1
3. Gate 2
4. Drain

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Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test condition
Drain to source breakdown voltage	$V_{(BR)DSX}$	12	—	—	V	I_D = 200 µA, V_{G1S} = –5 V, V_{G2S} = –5 V
Gate 1 to source breakdown voltage	$V_{(BR)G1SS}$	±10	—	—	V	I_{G1} = ±10 µA, V_{G2S} = V_{DS} = 0
Gate 2 to source breakdown voltage	$V_{(BR)G2SS}$	±10	—	—	V	I_{G2} = ±10 µA, V_{G1S} = V_{DS} = 0
Gate 1 cutoff current	I_{G1SS}	—	—	±100	nA	V_{G1S} = ±8 V, V_{G2S} = V_{DS} = 0
Gate 2 cutoff current	I_{G2SS}	—	—	±100	nA	V_{G2S} = ±8 V, V_{G1S} = V_{DS} = 0
Drain current	I_{DSS}	0	—	2	mA	V_{DS} = 6 V, V_{G1S} = 0, V_{G2S} = 3 V
Gate 1 to source cutoff voltage	$V_{G1S(off)}$	–0.7	—	+0.7	V	V_{DS} = 10 V, V_{G2S} = 3 V, I_D = 100 µA
Gate 2 to source cutoff voltage	$V_{G2S(off)}$	–0.1	—	+0.8	V	V_{DS} = 10 V, V_{G1S} = 3 V, I_D = 100 µA
Forward transfer admittance	$\|y_{fs}\|$	14	—	—	mS	V_{DS} = 6 V, V_{G2S} = 3 V, I_D = 10 mA, f = 1 kHz
Input capacitance	Ciss	0.9	1.25	1.8	pF	V_{DS} = 6 V, V_{G2S} = 3 V, I_D = 10 mA, f = 1 MHz
Output capacitance	Coss	0.4	0.7	1.2	pF	
Reverse transfer capacitance	Crss	—	0.015	0.03	pF	
Power gain	PG	16	19.4	—	dB	V_{DS} = 4 V, V_{G2S} = 3 V, I_D = 10 mA, f = 900 MHz
Noise figure	NF	—	2.8	4	dB	

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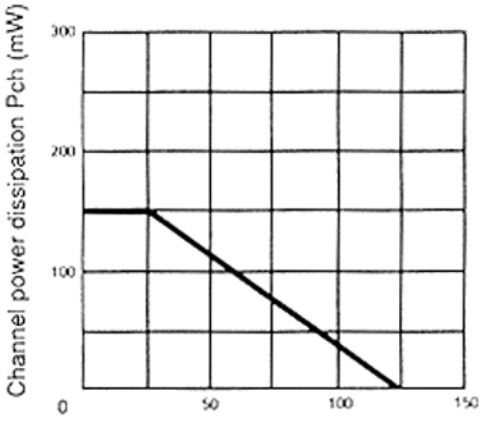
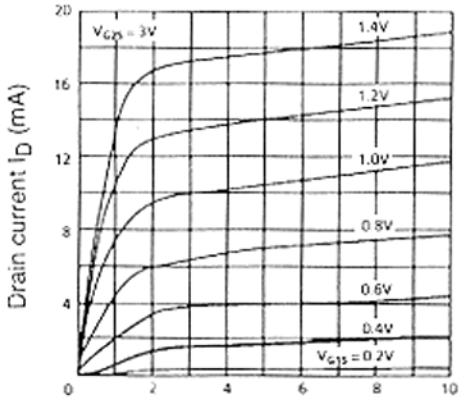
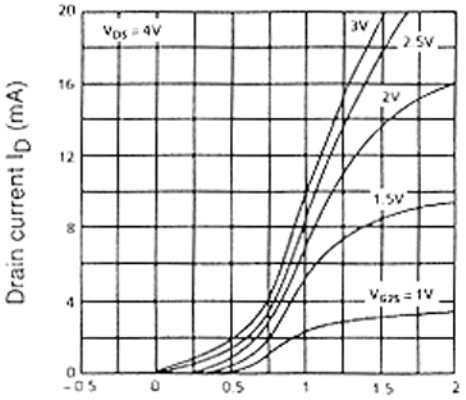
Maximum channel power dissipation curve



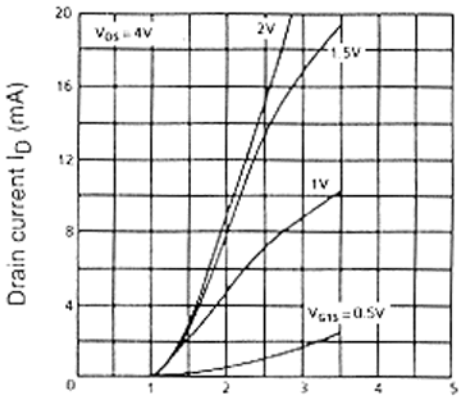
Typical output characteristics



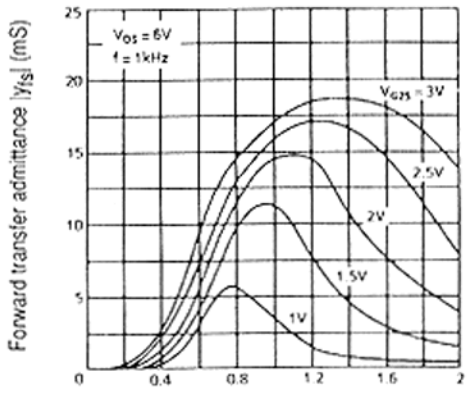
Drain current vs. gate 1 to source voltage



Drain current vs. gate 2 to source voltage

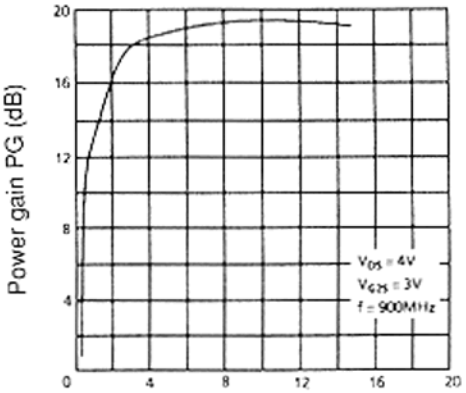


Forward transfer admittance vs. gate 1 to source voltage



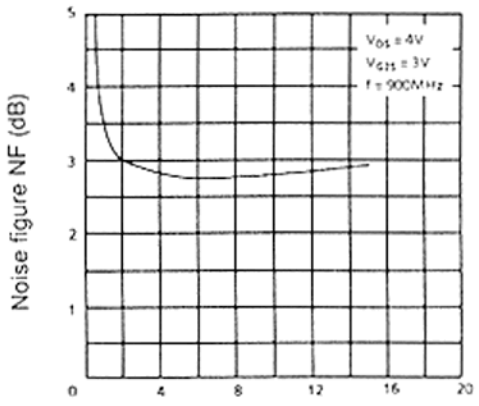
Gate 1 to source voltage V_{G1S} (V)

Power gain vs. drain current

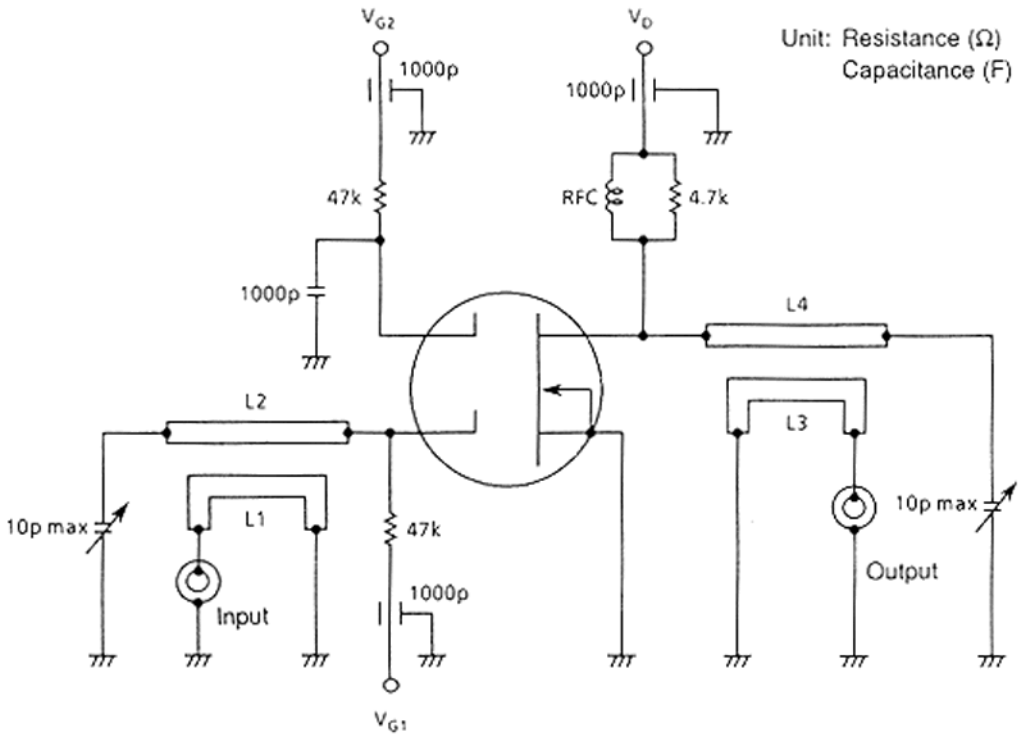


Drain current I_D (mA)

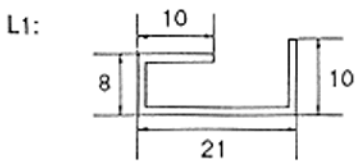
Noise figure vs. drain current

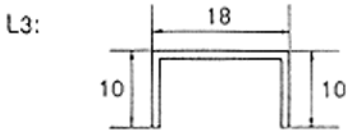


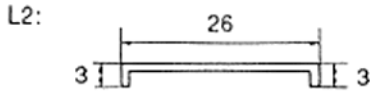
Drain current I_D (mA)

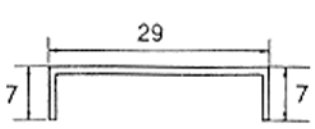


RFC: 4 turn, 6 mm inside dia (ϕ1 mm enameled copper wire)









Unit: mm

L1 to L4: ϕ1 mm copper wire

Figure 1 900 MHz Power Gain, Noise Figure Test Circuit