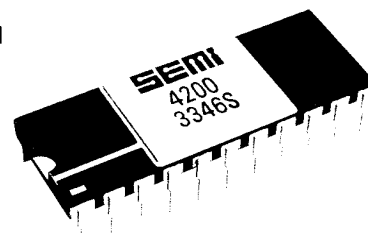


# SEMI 4200 150NSEC, STATIC, TTL IN/OUT, 4096x1 N-MOS RAM

## FEATURES

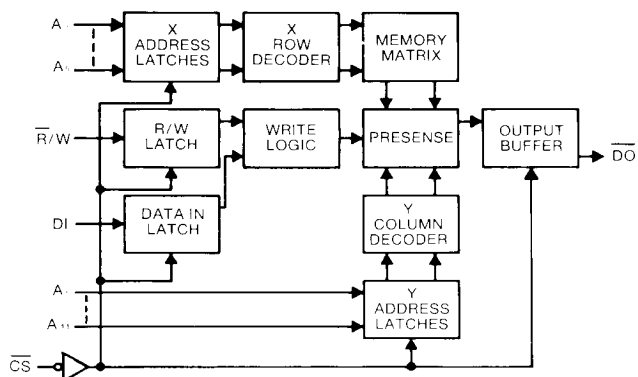
- Completely Static
- Access Time as low as 150 nsec max
- Cycle Time as low as 300 nsec max
- Typical Operating Power Under 450 mw.
- Typical Standby Power Under 35 mw.
- Data Retention with Low  $V_{DD}$
- Pin and Voltage Compatible with Standard 22 Pin 4K Dynamic Rams
- TTL Compatible Three-State Outputs
- Fully Decoded
- Active Low Chip Select

## GENERAL DESCRIPTION



The SEMI 4200 is an N-Channel MOS Random Access Memory, organized as 4096 words by one bit. It uses a fully static memory cell which eliminates the need for any refresh or charge pump circuitry. All inputs can be driven by standard TTL devices and the three-state data output can directly drive one TTL load of any type. The Chip Select input provides for simple memory expansion and low system power, by putting unselected devices into a high output impedance and low power state. For additional power savings  $V_{DD}$  can be reduced significantly, thus allowing data to be retained economically under battery power.

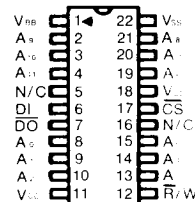
## BLOCK DIAGRAM



## PIN CONFIGURATION

$A_N$	Address Inputs
$\overline{DI}$	Data Input
$\overline{DO}$	Data Output
$\overline{CS}$	Chip Select Input
$\overline{R/W}$	Read/Write Input
N/C	No Internal Connection
$V_{SS}$	Ground
$V_{BB}$	Supply Voltage (-5V)
$V_{CC}$	Supply Voltage (+5V)
$V_{DD}$	Supply Voltage (+12V)

### TOP VIEW



# EMM SEMI 4200 150NSEC, STATIC, TTL IN/OUT, 4096x1 N-MOS RAM

## RECOMMENDED OPERATING CONDITIONS $T_{AMB}$ 0°C to 70°C

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	$V_{DD}$	11.4	12.0	12.6	V <sub>dc</sub>
Output Reference Voltage	$V_{CC}$	4.75	5.0	5.25	V <sub>dc</sub>
Substrate Voltage	$V_{BB}$	4.5	—	—5.5	V <sub>dc</sub>
Input High Level	$V_{IH}$	2.4	—	5.25	V <sub>dc</sub>
Input Low Level	$V_{IL}$	—0.1	—	0.7	V <sub>dc</sub>
Chip Select High Level	$V_{CH}$	8	12	15	V <sub>dc</sub>
Chip Select Low Level	$V_{CL}$	—1	—	0.5	V <sub>dc</sub>

## DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

CHARACTERISTICS	SYMBOL	4200A		4200B		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
Input Current	$I_{IN}$	—20	20	—20	20	—A	$V_{IN}$ 0.7V or 5V
Chip Select Input Current	$I_{CS}$	—20	20	—20	20	—A	$V_{CS}$ 0.5V or 12V
Output "Low" Voltage	$V_{OL}$	—	0.5	—	0.5	V <sub>dc</sub>	$I_{OL}$ 2.0mA Fig. 5
Output "High" Voltage	$V_{OH}$	2.7	$V_{CC}$	2.7	$V_{CC}$	V <sub>dc</sub>	$I_{OH}$ 500 —A Fig. 5
Output Current (Unselected)	$I_{OO}$	—20	20	—20	20	—A	$V_{OL}$ 2.7V, $V_{CS}$ 12V
Supply Current (Selected and Averaged Over One Cycle)	$I_{DD}$	—	50	—	55	mA	$T_{AMB}$ 25°C
		4200A	4200B				$V_{DD}$ 12V
$T_{CSW}$ 200		150					$V_{CC}$ 5V
$T_C$ 350		300					$V_{BB}$ 5V
For Other Conditions See Figure 3							$V_{CS}$ 12V
Supply Current (Unselected)	$T_{AMB}$ 25°C $I_{DD}$	—	5	—	5	mA	$V_{DD}$ 12V
	$T_{AMB}$ 70°C $I_{DD}$	—	15	—	15	mA	$V_{CC}$ 5V
Substrate Current	$I_{BB}$	—3	—	—3	—	mA	$V_{BB}$ —5V
Reference Supply Current	$I_{CC}$	—	100	—	100	—A	$V_{CS}$ 12V
Standby Current At Reduced Voltages	$T_{AMB}$ 25°C $I_{DDS}$	—	2	—	2	mA	$V_{CS}$ 4V to 15V
	$T_{AMB}$ 70°C $I_{DDS}$	—	6	—	6	mA	$V_{DD}$ 4V $V_{BB}$ —4V $V_{CC}$ 0V

## READ CYCLE — AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	4200A		4200B		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
Chip Select Read Pulse Width	$T_{CSR}$	200	—	150	—	ns	FULL OPERATING VOLTAGE AND TEMPERATURE RANGE
Chip Select Rise and Fall Time*	$T_{CR}, T_{CF}$	—	100	—	100	ns	
Set Up Time	$T_P$	0	—	0	—	ns	
Access Time	$T_A$	—	200	—	150	ns	
Cycle Time, $T_{CR} = T_{CF}$ 10ns	$T_C$	350	—	300	—	ns	
Data Hold Time	$T_H$	100	—	100	—	ns	
Output Recovery Time	$T_{OR}$	10	—	10	—	ns	
Read Recovery Time	$T_{CRR}$	125	—	125	—	ns	

## WRITE CYCLE — AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	4200A		4200B		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
Chip Select Write Pulse Width	$T_{CSW}$	200	—	150	—	ns	FULL OPERATING VOLTAGE AND TEMPERATURE RANGE
Chip Select Rise and Fall Time*	$T_{CR}, T_{CF}$	—	100	—	100	ns	
Set Up Time	$T_P$	0	—	0	—	ns	
Cycle Time, $T_{CR} = T_{CF}$ 10ns	$T_C$	350	—	300	—	ns	
Data Hold Time	$T_H$	100	—	100	—	ns	
Write Recovery Time	$T_{CWR}$	125	—	125	—	ns	

\*Typical Chip Select Rise and Fall Time ( $T_{CR}$  and  $T_{CF}$ ) is 10 ns For Read and Write Cycle

## CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Capacitance (Except Chip Select)	$C_{IN}$	—	4	6	pF	$V_{IN}$ 2.4V
Input Capacitance Chip Select	$C_{CS}$	—	6	10	pF	$V_{CS}$ 12V or 0V
Output Capacitance	$C_O$	—	6	8	pF	$V_O$ 2.7V $V_{CS}$ 12V



**ABSOLUTE MAXIMUM RATINGS** (See Note 1) (Referenced to GND)

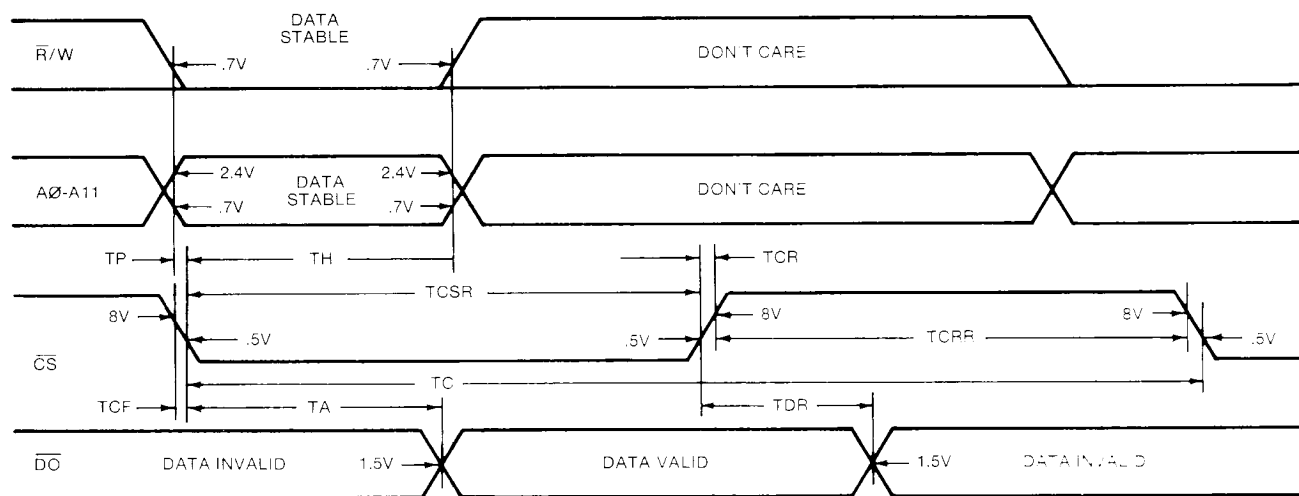
RATING	SYMBOL	VALUE	UNIT
Supply Voltages	$V_{DD}$	-1.5 to +18	Vdc
	$V_{CC}$	.5 to +7	Vdc
	$V_{BB}$	-1.5 to +18	Vdc
Input & Output Voltages (Except Chip Select)	$V_I, V_O$	$V_{BB}$ to +15	Vdc
Chip Select Input Voltage	$V_{CS}$	$V_{BB}$ to +15	Vdc
Power Dissipation	$P_D$	1.6 (Note 2)	W
Operating Ambient Temperature Range	$T_{AMB}$	0 to +70	°C
Storage Temperature Range		-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

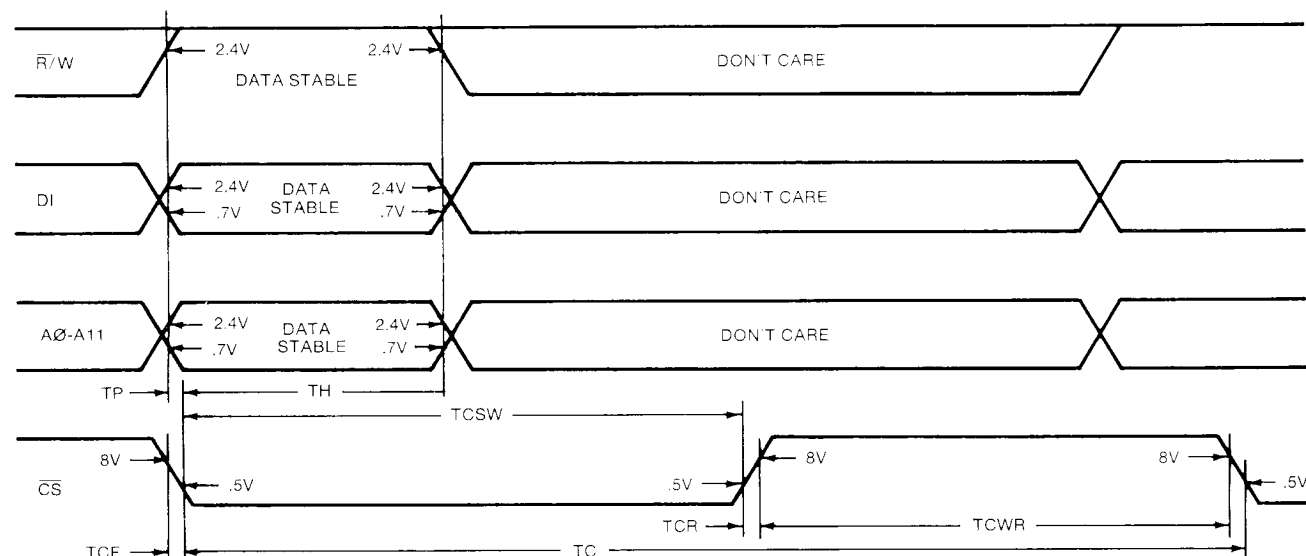
**NOTE 1:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

**NOTE 2:** At 25°C ambient. Derate 13.5mw/°C.

**Figure 1 — READ CYCLE**



**Figure 2 — WRITE CYCLE**



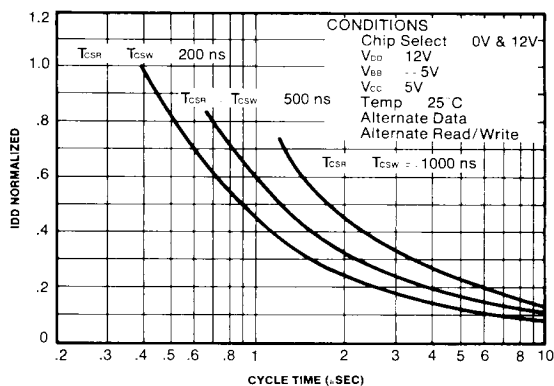


Figure 3. OPERATING  $I_{DD}$  AS A FUNCTION OF CYCLE TIME

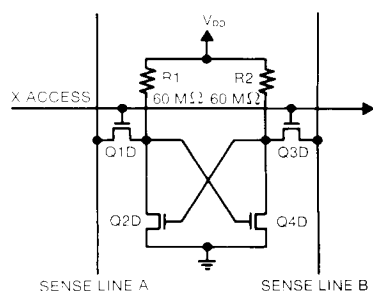
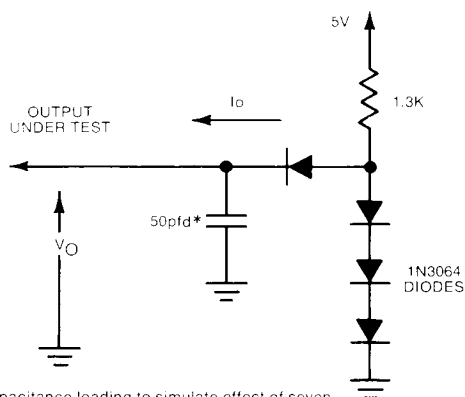


Figure 4. MEMORY CELL



\*Capacitance loading to simulate effect of seven additional outputs plus one TTL input

Figure 5. OUTPUT TEST LOAD

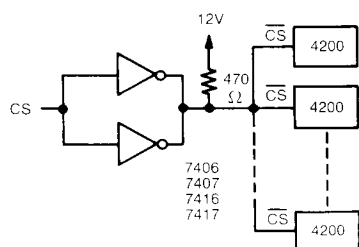


Figure 6. TYPICAL CHIP SELECT DRIVER

## FUNCTIONAL DESCRIPTION

EMM/SEMI 4200 is a 4096 bit static RAM with memory cells organized in an array of 64 rows by 64 columns (4096 words x 1 bit). Each memory cell is addressed by simultaneously decoding the X addresses ( $A_0$  through  $A_5$ ) for the rows and the Y addresses ( $A_6$  through  $A_{11}$ ) for the columns. Data is written or read on separate input ( $\overline{DI}$ ) and output ( $\overline{DO}$ ) pins. Logic level 1 is represented by a high state on pin  $\overline{DI}$  but is represented on  $\overline{DO}$  by a low state. The operation of the memory is controlled by chip select ( $\overline{CS}$ ) and read/write ( $\overline{R/W}$ ).

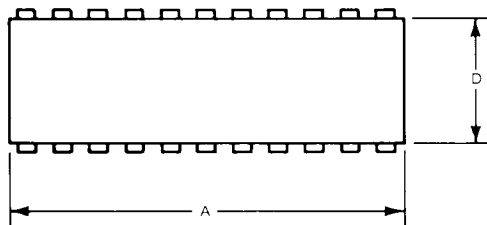
When  $\overline{CS}$  is high, all pins are in an inoperative high impedance state, and power is supplied only to the memory elements. When  $\overline{CS}$  is low, the memory is enabled for reading or writing.

The negative going edge of  $\overline{CS}$  begins timing for a read cycle. Data on  $\overline{R/W}$  and address pins ( $A_N$ ) must be stable for time  $T_H$ .  $\overline{R/W}$  and  $A_N$  will then have been latched into D type flip flops and no longer need to be held stable. Output data will be presented on  $\overline{DO}$  within time  $T_A$  and will remain until time  $T_{DR}$  after  $\overline{CS}$  goes high. Data will then be invalid. After time  $T_C$  another read or write cycle can be initiated.

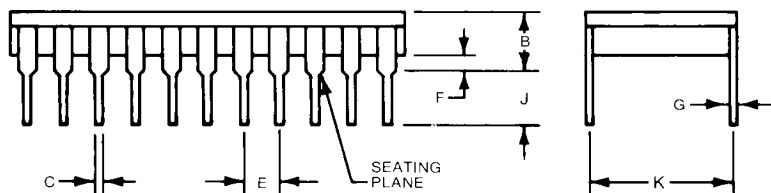
The negative going edge of  $\overline{CS}$  also begins timing for a write cycle.  $\overline{R/W}$ ,  $A_N$  and  $\overline{DI}$  must be held stable for time  $T_H$ . These inputs will then have been latched and  $\overline{DI}$  will be entered within time  $T_{CSW}$ . Another read or write cycle can be initiated after time  $T_C$ .

The memory cells (because they are cross coupled high impedance static cells) will retain data down to  $V_{DD} = 4V$ ,  $V_{BB} = -4V$ .

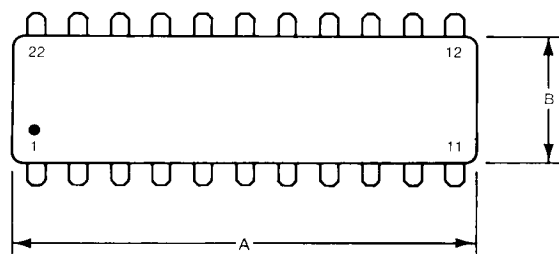
# CERAMIC PACKAGE DIMENSIONS



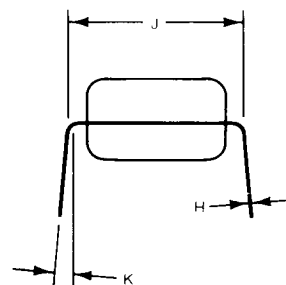
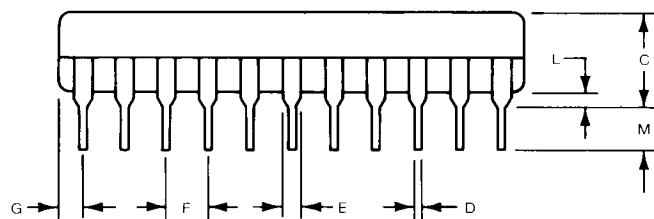
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.1	27.8	1.065	1.095
B	—	3.56	—	0.140
C	0.38	0.53	0.015	0.023
D	8.64	10.8	0.340	0.425
E	2.29	2.79	0.090	0.110
F	0.64	1.65	0.025	0.065
G	0.20	0.30	0.008	0.012
J	2.54	3.81	0.100	0.150
K	10.2 REF		0.4 REF	



# PLASTIC PACKAGE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.4	29.72	1.000	1.17
B	8.64	9.14	.340	.360
C	4.32	5.08	.170	.200
D	.36	.56	.014	.022
E	.76	1.52	.030	.060
F	2.41	2.67	.095	.105
G	1.02	2.03	.040	.080
H	.20	.31	.008	.012
J	9.65	10.16	.380	.400
K	0	15	0	15
L	.51	1.02	.020	.040
M	2.54	3.56	.100	.140



## ORDERING INFORMATION

Part Number	Access	Speed Cycle	Package	Temperature Range
4200ACC	200	350	Ceramic	0°C to -70°C
4200ACP	200	350	Plastic	0°C to -70°C
4200BCC	150	300	Ceramic	0°C to -70°C
4200BCP	150	300	Plastic	0°C to -70°C

### WARNING:

#### MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or in conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

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