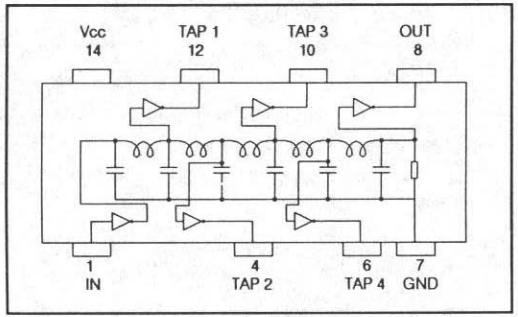
- ❒ **Schottky TTL buffered**
- ❒ **5 equally spaced taps**
- ❒ **14 pin package**
- ❒ **Low profile**
- ❒ **TTL compatible**
- ❒ **Auto insert or surface mount package styles**

DUAL - IN - LINE PACKAGE (TOP VIEW)



description

The 42A series of Digital Delay Modules are Schottky TTL buffered delay lines providing precise delay times and direct compatibility with TTL. Five equally spaced fixed delay taps are mounted in a low profile 14 pin dual-in-line package. Internal termination of the delay line and compensation for propagation delays and thermal drift are incorporated in the design so that no additional external components are required. These modules are particularly suitable for high density board designs. The 42S series is the surface mount version which may be vapour-phased at temperatures below 218C for durations of up to 2 minutes.

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{cc} 7V
Input voltage 5.5V
Min. pulse width as % of total delay 80%
Input pulse repetition rate PRR . . . . . 3 x pulse width min.
Operating free-air temperature range . . . . . 0C to 70C
Storage temperature range . . . . . –55C to 125C
Temperature coefficient of delay . . . . . ±300ppm/C
Lead temperature 1.5mm from case for 10 seconds 300C

drive capabilities

Logic 0 output . . . . . 10 TTL loads per tap max.
20 TTL loads per unit max.
Logic 1 output . . . . . 20 TTL loads per unit max.

electrical specifications over operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} High-level output voltage	V_{IH} =2V, I_{OH} =–1mA V_{CC} =4.75V	2.7	3.4		V
V_{OL} Low-level output voltage	V_{CC} =4.75V I_{OL}=20mA,V_{IL} =0.8V			0.5	V
I_{IH} High-level input current	V_{CC}=5.25V,V_{IH}=2.7V			50	μA
I_{IL} Low-level input current	V_{CC}=5.25V, V_{IL}=0.5V			–2	mA
Icc Supply current outputs high	V_{CC}=5.25V			24	mA
Icc Supply current outputs low	V_{CC}=5.25V			54	mA

delay characteristics Vcc = 5V, Ta = 25C, no load at taps, input test pulse width 100% of total delay, input rise time 3ns

delay tolerance from input to tap ±2ns or ±5% whichever is greater

42A SERIES 5 Tap 14 Pin DIP
Package style C with pins 2, 3, 5, 9, 11 and 13 missing

PART No. (1)	TOTAL DELAY (ns) ±5% (2)	TAP TO TAP DELAY (ns)	OUTPUT RISE TIME (ns)
42A - 5250	25	5 ± 2	3
42A - 5500	50	10 ± 2	3
42A - 5101	100	20 ± 2	3
42A - 5151	150	30 ± 3	4
42A - 5201	200	40 ± 4	4
42A - 5251	250	50 ± 5	4
42A - 5301	300	60 ± 6	4
42A - 5351	350	70 ± 7	4
42A - 5401	400	80 ± 8	4
42A - 5451	450	90 ± 9	4
42A - 5501	500	100 ± 10	4

(1) Surface mount part numbers start with 42S
Package style D with pins 2, 3, 5, 9, 11 and 13 missing
(2) or ±2ns whichever is greater

Note: Delays measured at 1.5V on leading edge, Rise Time measured from 0.7V to 2.4V.