1. APPLICATION

This data sheet applies to the conforming product specifications of the 68-pin, two-piece S-RAM card of the JEIDA 4.1 / PCMCIA 2.0 Memory Card Guidelines.

2. FUNDAMENTAL CIRCUITS

2.1 CIRCUIT CONFIGURATION

CMOS SRAM + Primary Lithium Battery (replaceable) + Secondary Battery (fixed type/charging type)

2.2 MEMORY CAPACITY

ITEM	MEMORY CAPACITY	MEMORY DEVICE CONFIGURATION
4-SR-64	64 KW x 8 bit or 32 KW x 16 bit (64 Kbyte)	256 Kbit SRAM x 2
4-SR-128	128 KW x 8 bit or 64 KW x 16 bit (128 Kbyte)	256 Kbit SRAM x 4
4-SR-256	256 KW x 8 bit or 128 KW x 16 bit (256 Kbyte)	1 Mbit SRAM x 2
4-SR-512	512 KW x 8 bit or 256 KW x 16 bit (512 Kbyte)	1 Mbit SRAM x 4
4-SR-1M	1 MW x 8 bit or 512 KW x 16 bit (1 Mbyte)	1 Mbit SRAM x 8
4-SR-2M	2 MW x 8 bit or 1 MW x 16 bit (2 Mbyte)	1 Mbit SRAM x 16

Attribute memory is an option available on SRAM memory cards. (see page 46 for attribute memory specification).

2.3 SUPPLY VOLTAGE

5V ± 5%

2.4 INPUT/OUTPUT SIGNAL LEVEL

TTL Logic Level

2.5 MEMORY BACKUP FUNCTIONS

* Primary battery/ secondary battery are internal and have memory support functions for DATA in the SRAM area.
* Primary battery has a replacement structure and battery life is as written below.
(The secondary battery functions as a "backup" during primary battery replacement.)

ITEM	MEMORY CAPACITY	MEMORY BACKUP TIME
4-SR-64	64 Kbyte	5 Years
4-SR-128	128 Kbyte	4 Years
4-SR-256	256 Kbyte	2 Years
4-SR-512	512 Kbyte	2 Years
4-SR-1M	1 Mbyte	1 Years
4-SR-2M	2 Mbyte	1 Year

Standards: Tstg = 25°C

Lithium Primary Battery : CR2325 (FDK TYPE 3V/175mAH) and similar products

Secondary Battery : AL920 (Seiko, Charging Type) and similar products

3. CIRCUIT CONFIGURATION AND LOGIC

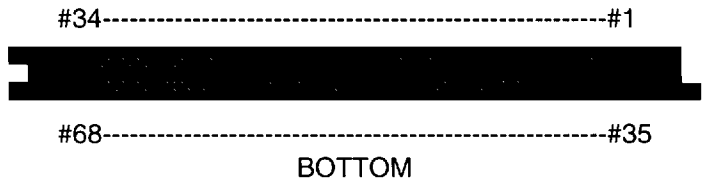
3.1 PIN ARRANGEMENT

PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL	PIN #	SIGNAL
1	GND	11	A9	21	A12	31	D1	41	D15	51	Vcc	61	*REG
2	D3	12	A8	22	A7	32	D2	42	CE2	52	NC	62	BVD2
3	D4	13	A13	23	A6	33	WP	43	NC	53	NC	63	BVD1
4	D5	14	A14	24	A5	34	GND	44	NC	54	NC	64	D8
5	D6	15	WE/PGM	25	A4	35	GND	45	NC	55	NC	65	D9
6	D7	16	NC	26	A3	36	*CD1	46	A17	56	NC	66	D10
7	CE1	17	Vcc	27	A2	37	D11	47	A18	57	NC	67	*CD2
8	A10	18	NC	28	A1	38	D12	48	A19	58	RESET	68	GND
9	*OE	19	A16	29	A0	39	D13	49	A20	59	*WAIT		
10	A11	20	A15	30	D0	40	D14	50	NC	60	NC		

3.2 PIN DESCRIPTION

PIN #	PIN DESCRIPTION
A0~A20	ADDRESS INPUT
D0~D15	DATA INPUT/OUTPUT
CE1,CE2	CARD ENABLE
*REG	REGISTER SELECT
*OE	OUTPUT ENABLE
WE/PGM	WRITE ENABLE/PROGRAM
*CD1,CD2	CARD DETECT
WP	WRITE PROTECT
RESET	RESET
*WAIT	WAIT
BVD1,BVD2	BATTERY VOLTAGE DETECT
Vcc	POWER SUPPLY (+5V)
GND	GROUND
NC	NO CONNECTION

3.3 PIN DIAGRAM

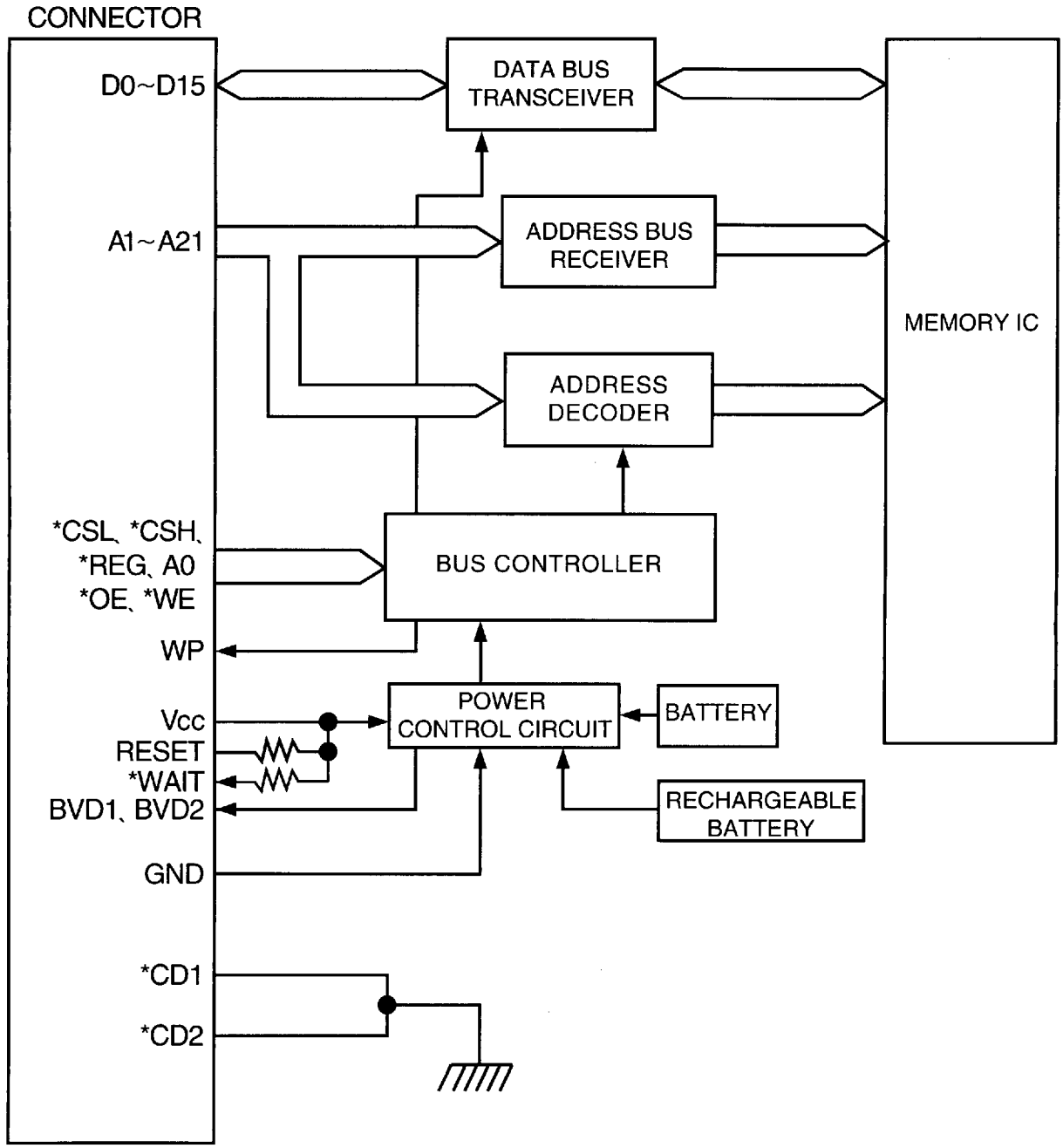


This PIN arrangement conforms with the standards set by JEIDA/ PCMCIA.

NOTES:

1. *64 Kbyte....#19, 46, 47, 48, 49 are not connected.
2. *128 Kbyte....#46, 47, 48, 49 are not connected.
3. *256 Kbyte....#47, 48, 49 are not connected.
4. *512 Kbyte....#48, 49 are not connected.
5. *1 Mbyte....#49 is not connected.

3.4 BLOCK DIAGRAM



3.5 FUNCTION TABLES

READ MODE

MODE	*REG	CE2	CE1	A0	*OE	WE	WP	D15-D8	D7-D0
STANDBY MODE	X	H	H	X	X	X	OFF/ON	HIGH-Z	HIGH-Z
BYTE ACCESS (8 BIT)	H	H	L	L	L	H	OFF/ON	HIGH-Z	EVEN-BYTE
	H	H	L	H	L	H	OFF/ON	HIGH-Z	ODD-BYTE
WORD ACCESS (16 BIT)	H	L	L	X	L	H	OFF/ON	ODD-BYTE	EVEN-BYTE
ODD-BYTE ADDRESS ACCESS (ONLY)	H	L	H	X	L	H	OFF/ON	ODD-BYTE	HIGH-Z

WRITE MODE

MODE	*REG	CE2	CE1	A0	*OE	WE	WP	D15-D8	D7-D0
STANDBY MODE	X	H	H	X	X	X	OFF/ON	X	X
BYTE ACCESS (8 BIT)	H	H	L	L	H	L	OFF	X	EVEN-BYTE
	H	H	L	H	H	L	OFF	X	ODD-BYTE
WORD ACCESS (16 BIT)	H	L	L	X	H	L	OFF	ODD-BYTE	EVEN-BYTE
ODD-BYTE ADDRESS ACCESS (ONLY)	H	L	H	X	H	L	OFF	ODD-BYTE	X

*H: High level, L: Low level, X: Don't Care, Not Valid: Not Valid

NOTES:

1. BVD1, BVD2 have the following functions for detect output of internal battery voltage. Also, output goes to low level during alarm.
2. BVD1: When battery voltage cannot assure SRAM data retention (detection voltage = 2.37Vtyp).
3. BVD2: When battery voltage cannot assure SRAM data retention immediately (detection voltage = 2.65Vtyp).
4. The WP signal is output in high level (Protected) when enabled and output in low level (Not Protected) when the switch is disabled.

4. ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SIGNAL	RATING	UNIT
POWER SUPPLY	Vcc	-0.5~+6.0	V
INPUT VOLTAGE	Vin	-0.5~Vcc +0.5	V
OUTPUT VOLTAGE	Vout	-0.5~Vcc +0.5	V
OPERATION TEMPERATURE	Topr	0~+60	°C
STORAGE TEMPERATURE	Tstg	-20~+70	°C
DATA RETENTION TEMPERATURE	Tdr	0~+70	°C

5. RECOMMENDED OPERATING CONDITIONS

DESCRIPTION	SIGNAL	RATING		UNIT
		MIN	MAX	
POWER SUPPLY VOLTAGE	Vcc	4.75	5.25	V
INPUT VOLTAGE HIGH	Vih	2.4		V
INPUT VOLTAGE LOW	Vil		0.8	V
OPERATION TEMPERATURE	Topr	0	+55	°C
DATA RETENTION TEMPERATURE	Tdr	0	+55	°C

6. ELECTRICAL CHARACTERISTICS

6.1 DC CHARACTERISTICS (WITHIN OPERATION PARAMETERS)

ITEM	SIGNAL	RATING		UNIT	CONDITIONS
		MIN	MAX		
INPUT LEAK CURRENT	Ili	-10	10	µA	Vin= 0~Vcc, excluding *CE, *REG, *WE
		-32	10	µA	Vin= 0~Vcc, Inputting *CE, *REG, *WE
OUTPUT LEAK CURRENT	Ili/o	-10	10	µA	excluding BVD1, BVD2, Vout=0~Vcc, CE=Vih, *OE=Vih, *WE=Vil
STANDBY CURRENT	Isb		100	µA	CE=Vih, Separate Input=Vih or Vil
OPERATING CURRENT	Icc		80	mA	CE=Vil, Separate Input=Vih or Vil, Iout=0 mA
INPUT VOLTAGE "H" LEVEL	Vih	2.4		V	
INPUT VOLTAGE "L" LEVEL	Vil		0.8	V	
OUTPUT VOLTAGE "H" LEVEL	Voh	2.4		V	Ioh=-4.0mA (Output BVD1, BVD2), Ioh=-1.0 mA (Output separately)
OUTPUT VOLTAGE "L" LEVEL	Vol		0.4	V	Iol=5.0mA (Ouput BVD1, BVD2) Iol=5.02.1mA (Output separately)

NOTE:

1. CE = CE1, CE2

6.2 AC CHARACTERISTICS (WITHIN OPERATION PARAMETERS)

READ TIMING SPECIFICATIONS

DESCRIPTION	SIGNAL	RATING		UNIT
		MIN	MAX	
READ CYCLE TIME	$t_c(R)$	200		ns
ADDRESS ACCESS TIME[4]	$t_a(A)$		200	ns
DATA VALID FROM ADD CHANGE[4]	$t_v(A)$	0		ns
CARD ENABLE ACCESS TIME	$t_a(CE)$		200	ns
OUTPUT ENABLE ACCESS TIME	$t_a(OE)$		100	ns
ADDRESS HOLD TIME	$t_h(A)$	20		ns
OUTPUT ENABLE TIME FROM *CE	$t_{en}(CE)$	5		ns
OUTPUT ENABLE TIME FROM *OE	$t_{en}(OE)$	5		ns
OUTPUT DISABLE TIME FROM *CE	$t_{dis}(CE)$		90	ns
OUTPUT DISABLE TIME FROM *OE	$t_{dis}(OE)$		90	ns

NOTES:

1. These timings are specified only when -WAIT is asserted within the cycle.
2. These timings are specified for hosts and cards which support the -WAIT signal.
3. 600 nsec cycle timings apply for 3.3 volt reduced operating voltage.
4. The -REG signal timing is identical to address signal timing.

WRITE TIMING SPECIFICATIONS

DESCRIPTION	SIGNAL	RATING		UNIT
		MIN	MAX	
WRITE CYCLE TIME	t_cW	200		ns
WRITE PULSE WIDTH	t_w(WE)	120		ns
ADDRESS SETUP TIME[3]	t_{su}(A)	20		ns
ADDRESS SETUP TIME FOR WE[3]	t_{su}(A-WEH)	140		ns
CARD ENABLE SETUP TIME FOR WE	t_{su}(CE-WEH)	140		ns
DATA SETUP TIME FOR WE	t_{su}(D-WEH)	60		ns
DATA HOLD TIME	t_h(D)	30		ns
WRITE RECOVER TIME	t_{rec}(WE)	30		ns
OUTPUT DISABLE TIME FROM WE	t_{dis}(WE)		90	ns
OUTPUT DISABLE TIME FROM OE	t_{dis}(OE)		90	ns
OUTPUT ENABLE TIME FROM WE	t_{en}(WE)	5		ns
OUTPUT ENABLE TIME FROM OE	t_{en}(OE)	5		ns
OUTPUT ENABLE SETUP FROM WE	t_{su}(OE-WE)	10		ns
OUTPUT ENABLE HOLD FROM WE	t_h(OE-WE)	10		ns
CARD ENABLE SETUP TIME[1]	t_{su}(CE)	0		ns
CARD ENABLE HOLD TIME[1]	t_h(CE)	20		ns
WAIT VALID FROM WE[1]	t_v(WT-WE)		35	ns
WAIT PULSE WIDTH[2]	t_w(WT)		12	µs
WE HIGH FROM WAIT RELEASED[2]	t_v(WT)	0		ns

NOTES:

1. These timings are specified for hosts and cards which support the -WAIT signal.
2. These timings specified only when -WAIT is asserted within the cycle.
3. The -REG signal timing is identical to address signal timing.
4. 600 nsec cycle times apply for 3.3 volt reduced operating speed.

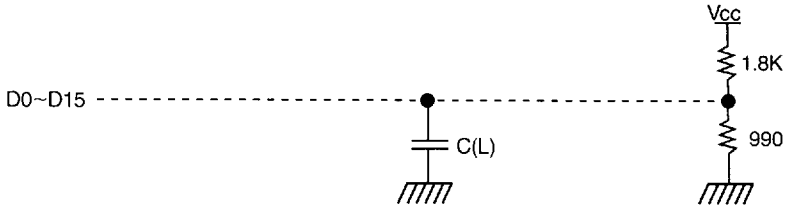
6.3 TERMINAL CAPACITANCE

ITEM	CONDITIONS	SIGNAL	MIN	MAX	UNIT
INPUT TERMINAL	f=1MHz	C IN		35	pF
OUTPUT TERMINAL	T opr=25°C	C OUT		35	pF
INPUT/OUTPUT TERMINAL	V i/o = OV	C I/O		45	pF

6.4 AC CHARACTERISTIC MEASUREMENT CONDITIONS

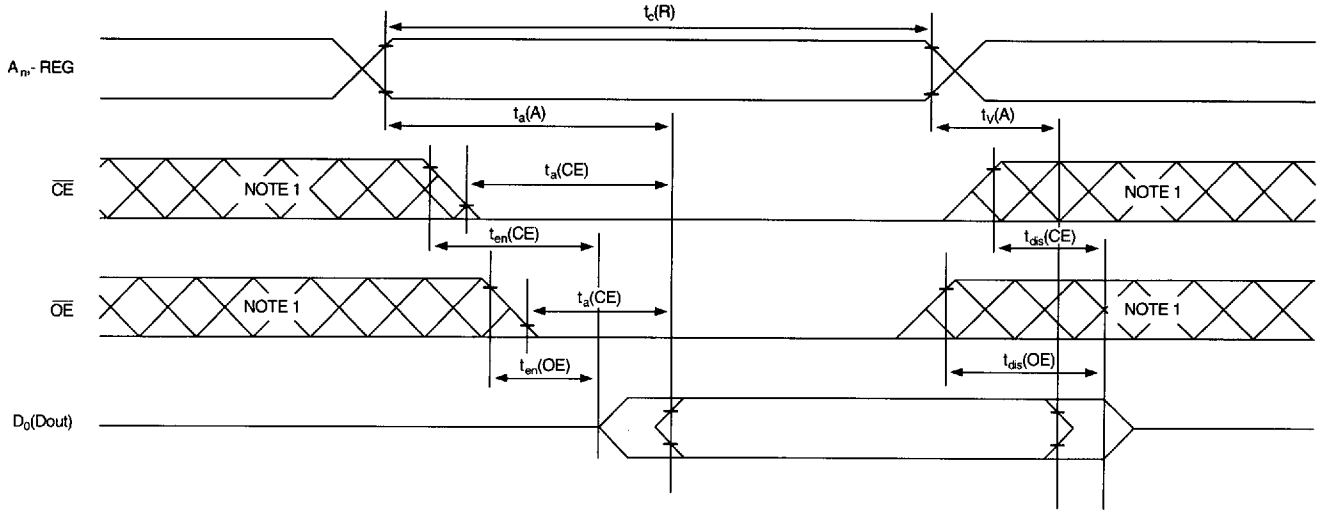
INPUT VOLTAGE	:V IH = 2.4V, V IL = 0.6V
INPUT PULSE TERMINAL RISE/FALL	:tr,tf = 5~10ns (0.8V~2.2V)
TIMING MEASUREMENT VOLTAGE	:Input Vi (H) = 2.2V, Vi (L) = 0.8V
	Output Vo (H) = 2.2V, Vo(L) = 0.8V
OUTPUT LOAD	:ITTL + 100pF

Output load for measurement of:< T clz, T olz, T chz, T ohz, T wlz, T whz >



7. MEMORY TIMING DIAGRAMS

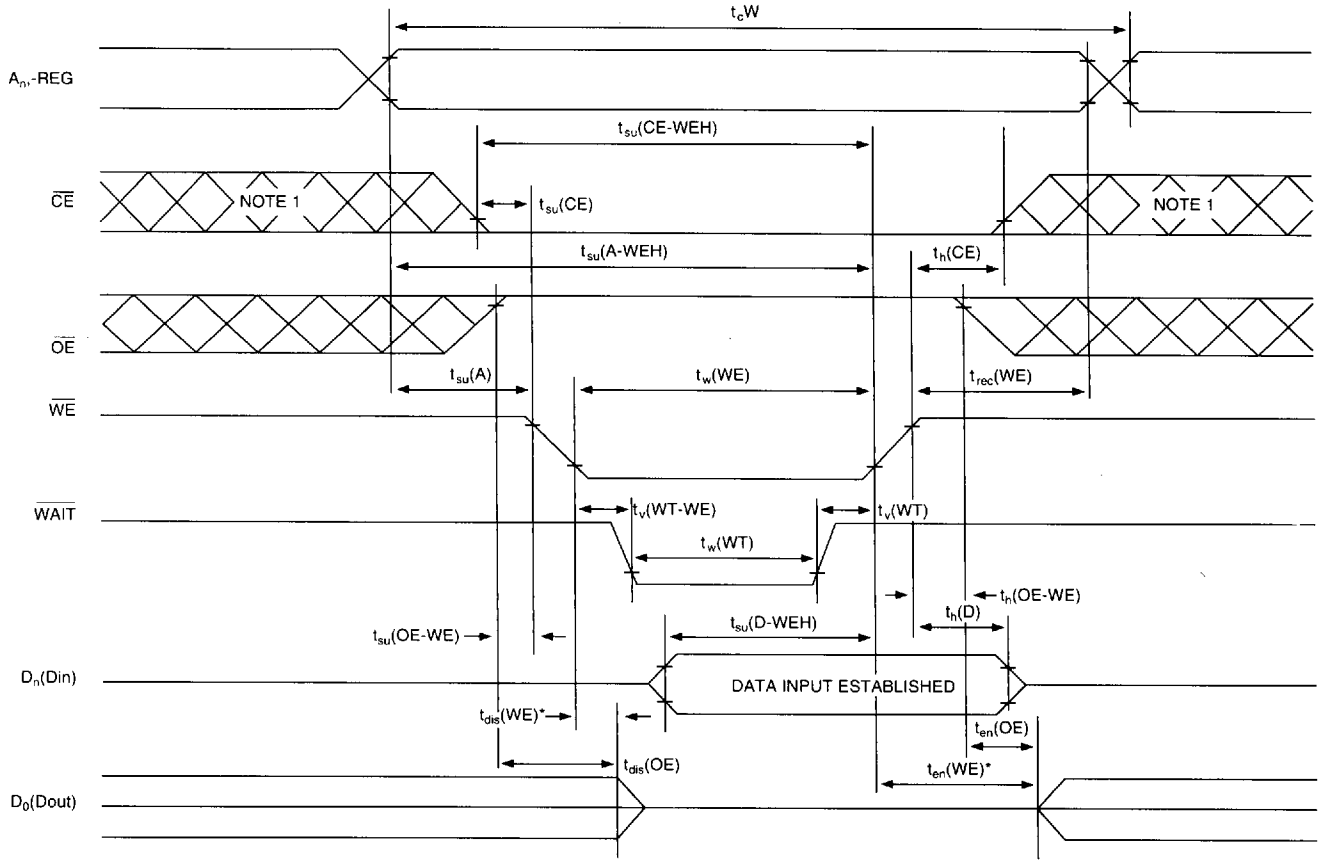
7.1 READ TIMING SPECIFICATIONS



NOTE:

1. The hatched portion may be either high or low.

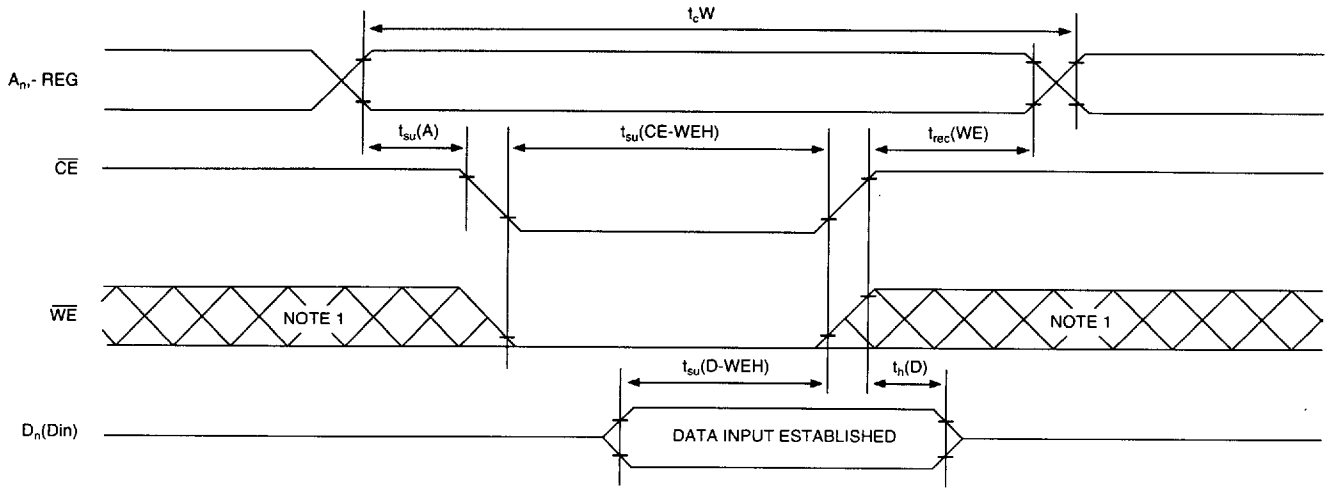
7.2 WRITE TIMING SPECIFICATIONS (WE CONTROL)



NOTE:

1. The hatched portion may be either high or low.

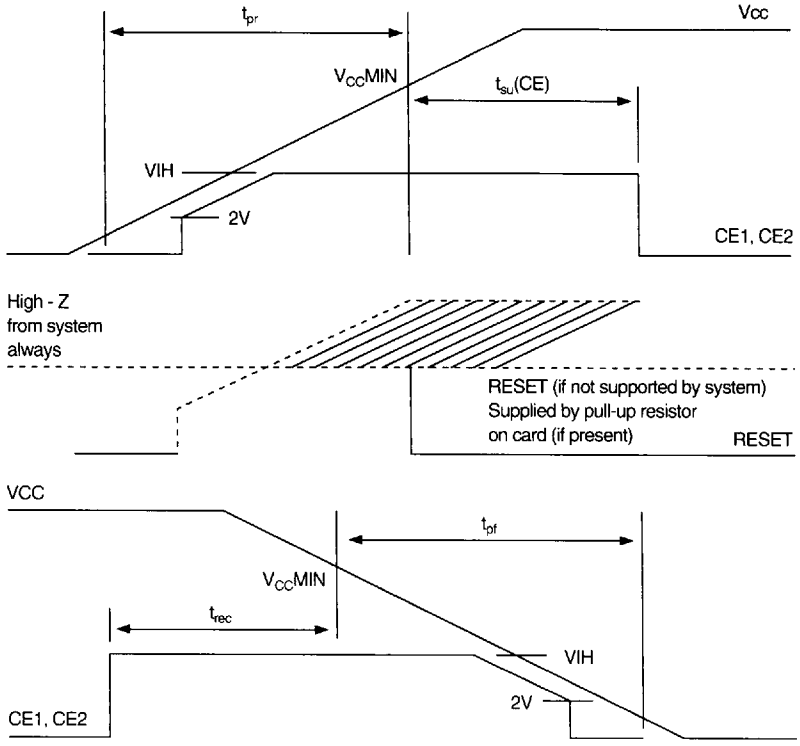
7.3 WRITE TIMING SPECIFICATIONS (CE CONTROL)



NOTE:

1. The hatched portion may be either high or low.

7.5 POWER SEQUENCE



ITEM	SIGNAL	MIN	STANDARD	MAX
POWER SOURCE DETECT (RISING)	Vin(H)	4.2V	4.3V	4.4V
POWER SOURCE DETECT (FALLING)	Vin(L)	4.1V	4.2V	4.3V
BATTERY BACKUP RECOVERY TIME	*1 Tbr	1.6ms		
DATA RETAIN SETUP TIME	*2 T dr(su)			0.5 ms
BATTERY BACKUP SETUP TIME	*3 T bs	10µs		
DATA RETAIN SETUP TIME (POWER FALL)	*4 T dr(sf)	0ns		

NOTES:

*1. Time standby state is retained after power has switched from Vbb to Vcc.

*2. Time until standby state is defined after power has switched from Vbb to Vcc.

*3. Time standby state is retained until power has switched from Vcc to Vbb.

*4. Time card is retained in standby state before power switches from Vcc to Vbb.

8. FUNCTIONS

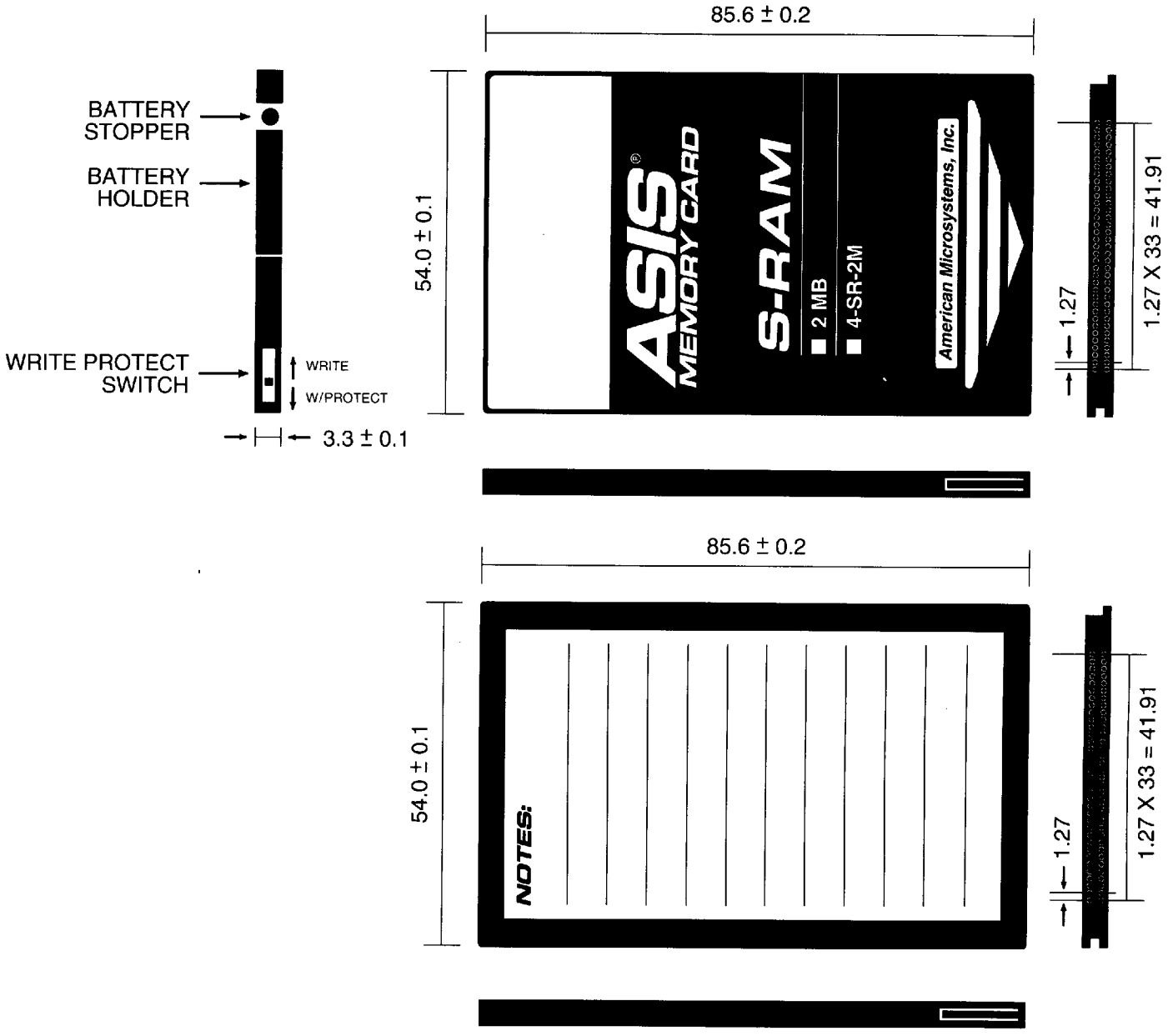
(1) Data crash prevention for battery consumption in the event of a card terminal short circuit.

(2) Data crash prevention during Power Rise/Fall.

(3) Data crash and latch locking prevention circuit to prevent a card from being inserted into or removed from equipment that may still have power running through it.

9. MECHANICAL CHARACTERISTICS

9.1 EXTERNAL DIMENSION



10. CARD INSPECTION

10.1 SPECIAL FEATURE TESTING

#	ITEM	TESTING PARAMETERS	TEST TEMP.	# INSPECTED
1	HIGH TEMP. OPERATION	Read/Write data retention battery conditions are +5.25V / +4.75V.	+55 °C	All
2	EXTERNAL EXAMINATION	Correct markings, correct labeling, no marks or scratches, WP switch is in WRITE position, battery stopper is in LOCK position.	Room Temperature	All

1. ATTRIBUTE MEMORY FUNCTION TABLES

ATTRIBUTE MEMORY (READ MODE)

MODE	*REG	CE2	CE1	A0	*OE	WE/PGM	WP	D15-D8	D7-D0
STANDBY MODE	X	H	H	X	X	X	OFF/ON	HIGH-Z	HIGH-Z
BYTE ACCESS (8 BIT)	L	H	L	L	L	H	OFF/ON	HIGH-Z	EVEN-BYTE
	L	H	L	H	L	H	OFF/ON	HIGH-Z	NOT VALID
ODD ADDRESS ACCESS (ONLY)	L	L	L	X	L	H	OFF/ON	NOT VALID	EVEN-BYTE
ODD-BYTE ACCESS (ONLY)	L	L	H	X	L	H	OFF/ON	NOT VALID	HIGH-Z

ATTRIBUTE MEMORY (WRITE MODE)

MODE	*REG	CE2	CE1	A0	*OE	WE/PGM	WP	D15-D8	D7-D0
STANDBY MODE	X	H	H	X	X	X	OFF/ON	NOT VALID	NOT VALID
BYTE ACCESS (8 BIT)	L	H	L	L	H	L	OFF	NOT VALID	EVEN-BYTE
	L	H	L	H	H	L	OFF/ON	NOT VALID	NOT VALID
WORD ACCESS (16 BIT)	L	L	L	X	H	L	OFF	NOT VALID	EVEN-BYTE
ODD-BYTE ADDRESS (ONLY)	L	L	H	X	H	L	OFF/ON	NOT VALID	NOT VALID

*H: High level, L: Low level, X: Don't Care, Not Valid: Not Valid

2. ATTRIBUTE MEMORY AC CHARACTERISTICS

(WITHIN OPERATION PARAMETERS)

ATTRIBUTE MEMORY READ TIMING SPECIFICATIONS

ITEM	SIGNAL	RATING		UNIT
		MIN	MAX	
READ CYCLE TIME	t_{cR}	300		ns
ADDRESS ACCESS TIME	$t_{a(A)}$		300	ns
CARD ENABLE ACCESS TIME	$t_{a(CE)}$		300	ns
OUTPUT ENABLE ACCESS TIME	$t_{a(OE)}$		150	ns
OUTPUT DISABLE TIME FROM *OE	$t_{dis(OE)}$		100	ns
DATA VALID FROM ADD CHANGE	$t_{v(A)}$	30		ns

ATTRIBUTE MEMORY WRITE TIMING SPECIFICATIONS

ITEM	SIGNAL	RATING		UNIT
		MIN	MAX	
WRITE CYCLE TIME	t_{cW}	10		ms
DATA SETUP TIME	t_{su}	200		ns
DATA HOLD TIME	$t_{h(D)}$	100		ns
WRITE PULSE WIDTH	$t_{w(WT)}$	300		ns
ADDRESS SETUP TIME	t_{su}	20		ns
ADDRESS HOLD TIME	$t_{h(D)}$	200		ns
CARD ENABLE SETUP TIME	$t_{su(CE)}$	10		ns
CARD ENABLE HOLD TIME	$t_{h(CE)}$	10		ns
OUTPUT ENABLE SETUP TIME	$t_{su(OE)}$	10		ns
OUTPUT ENABLE HOLD TIME	$t_{h(OE)}$	0		µs

NOTES:

1. Attribute memory space consists of 8K Byte X 8-Bit wide EEPROM.
2. The EEPROM attribute memory is an option available on SRAM, FLASH, and MASK ROM memory cards.

3. ATTRIBUTE MEMORY WRITE TIMING SPECIFICATIONS