T-73-65

5021 & 5025

DATA AND SPECIFICATIONS
DESCRIPTION AND INSTRUCTIONS

Optical Electronics Incorporated

HIGH SPEED ANALOG SAMPLE & HOLD MEMORIES

FEATURES

- BANDWIDTH: DC -100MHz
- SLEW RATE: 600V/μsec
- ACQUISITION: 30nsec Cx = 10pF
- OUTPUT: ±10V, ±30mA
- DROOP RATE: 1mV/μsec, Cx = 100pF
- TTL LOGIC COMMAND LINE

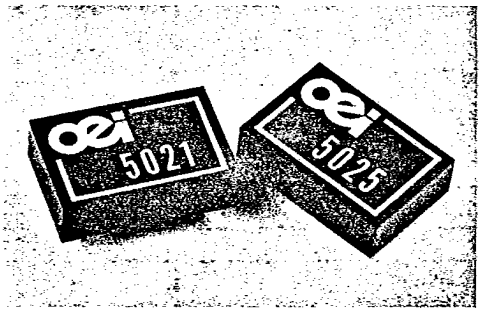
APPLICATIONS

- ANALOG DATA ACQUISITION
- WAVEFORM MEASUREMENT
- PULSE AMPLITUDE MODULATION
- ANALOG DELAY CIRCUIT

DESCRIPTION

The 5021 and the 5025 Sample and Hold Analog Memories are designed for versatility of application. Because their frequency response characteristics are determined by an external capacitor, they can essentially be tailored to any specific application requirements. Both devices provide an output voltage equal to the sampled input voltage at the time the input voltage has been sampled. Because of the very short acquisition times, particularly for the 5025, rapid sampling and thus steep input signal slopes can be accommodated. The major differences between the two devices can be found in the areas of tracking slewing rate and acquisition time. The slewing rate for the 5021 is an impressive 150V/μs with a charge capacitor of 0pF. The slewing rate for the 5025 exceeds at 600V/μs known industry standards, particularly at a bandwidth range of DC to 100MHz. The acquisition time for the 5025 is a mere 30ns when a charge capacitor of 10pF is used.

Both devices operate at unit gain and can, therefore, be used in numerous applications where no gain is required. Furthermore, both devices accept an input voltage of ±10 volts minimum and provide a load current of ±30mA min. This then makes them ideal as drivers.



As has been mentioned earlier, the frequency response of either device can be tailored by the externally applied charge capacitor Cx. Curves of slewing rate vs. capacitance and small signal bandwidth vs. capacitance are given in the section Typical Performance Curves. The droop of the devices is also dependent on the size of the sum of the internal and external charge capacitors. The larger the external capacitor is made, the smaller the droop rate becomes. However, slew rate and bandwidth are, of course, affected by the size of the capacitor, too. In most cases, it is advantageous to use the 5021 rather than enlarging Cx on the 5025. This also holds true when the maximum capacitive load exceeds 100pF considerably.

SPECIFICATIONS

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ELECTRICAL

Specifications at T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

MODEL		5021			5025			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ERROR								
Voltage Gain			.98			.98		V/V
Memory Leakage				10			10	nA
Command Feedthrough Capacitance				0.1			0.1	pF
Signal Feedthrough Capacitance							0.25	pF
Warm Up Time				10			10	min
RATED OUTPUT								
Voltage		±10			±10			V
Current		±30			±30			mA
Output Resistance				30			30	Ω
Temperature Drift				±400			±400	µV/°C
Load Capacitance				1000			1000	pF
DYNAMIC RESPONSE								
Tracking Mode	Cx = 0		100			100		MHz
Bandwidth	Cx = 10pF					10		MHz
	Cx = 100pF		10					MHz
	Cx = 1nF					1		MHz
	Cx = 100nF		30					KHz
Tracking Slew Rate	Cx = 0		150			600		V/µsec
	Cx = 10pF					400		V/µsec
	Cx = 100pF		15					V/µsec
	Cx = 1nF					10		V/µsec
	Cx = 100nF		0.15					V/µsec
Aperture Time				3			3	nsec
Aperture Jitter				300			300	psec
Aquisition Time	Cx = 10pF						30	nsec
	Cx = 100pF			1.0				µsec
	Cx = 1nF						2	µsec
	Cx = 100nF			100				µsec
Settling Time to 0.1%	Cx = 0			150				nsec
	Cx = 10pF						50	nsec
	Cx = 100pF			1.4				µsec
	Cx = 1nF						3	µsec
	Cx = 100nF			140				µsec
Non-Linearity	at 100Hz			0.3			0.1	%
	at 100KHz			0.3			0.3	%
INPUT								
Voltage Range		±10			±10			V
Signal Resistance				10			5	kΩ
Signal Bias Current				2			.1	mA
Command Voltage	Hold	2			2			V
	Sample			0.8			.08	V
Command Resistance		2			2			kΩ
Command Bias Current				3			3	mA
POWER SUPPLY								
Rated Voltage		±13	±15	±18	±13	±15	±18	V
Current Quiescent				±30			±90	mA
TEMPERATURE RANGE								
Specification		-55		+85	-55		+85	°C
Operating		-55		+100	-55		+100	°C
Storage		-65		+100	-65		+100	°C
Thermal Resistance				20			20	°C/W
*Quiescent Temperature Rise				18			54	°C

*Note: Quiescent Temperature Rise is temperature above ambient.

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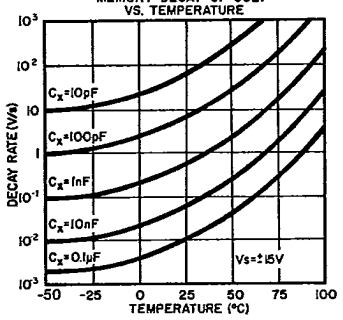
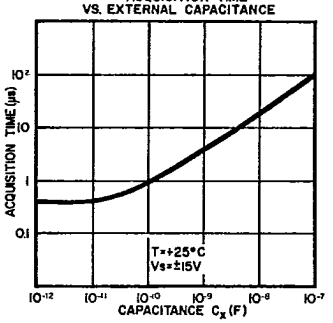
5021
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)

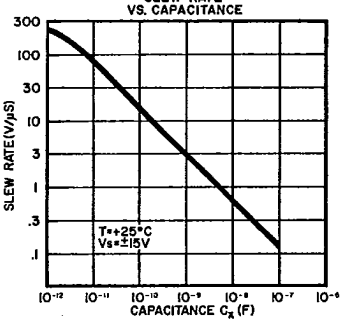
MEMORY DECAY OF 5021 VS. TEMPERATURE



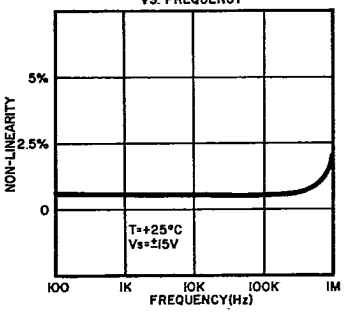
ACQUISITION TIME VS. EXTERNAL CAPACITANCE



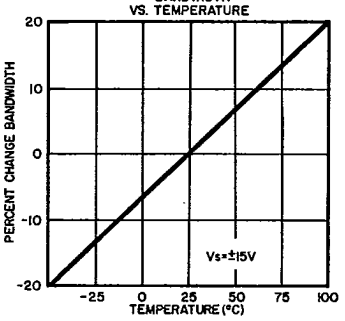
SLEW RATE VS. CAPACITANCE



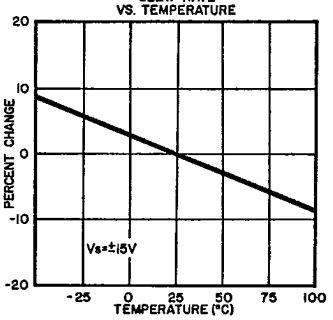
NON-LINEARITY VS. FREQUENCY



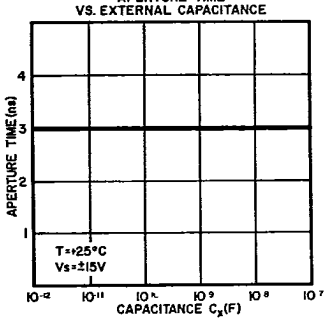
BANDWIDTH VS. TEMPERATURE



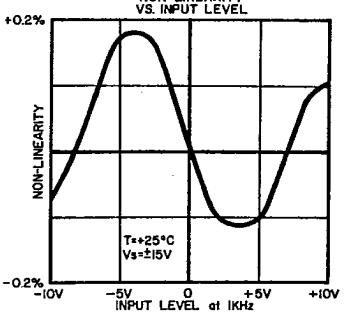
SLEW RATE VS. TEMPERATURE



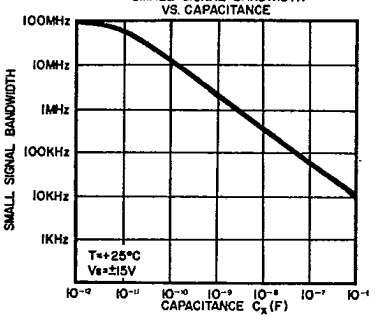
APERTURE TIME VS. EXTERNAL CAPACITANCE



NON-LINEARITY VS. INPUT LEVEL



SMALL SIGNAL BANDWIDTH VS. CAPACITANCE



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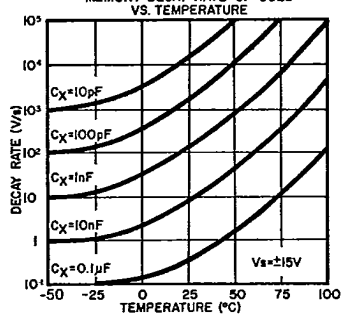
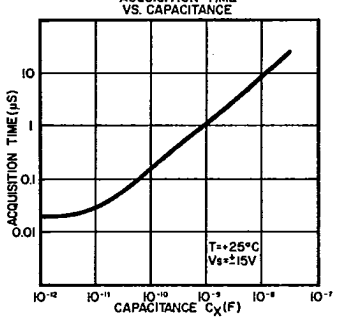
5025
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)

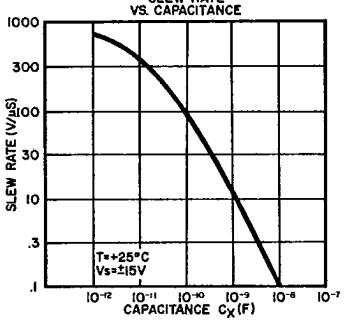
MEMORY DECAY RATE OF 5025 VS. TEMPERATURE



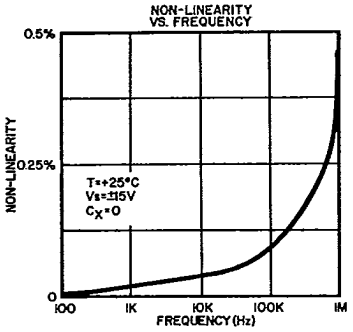
ACQUISITION TIME VS. CAPACITANCE



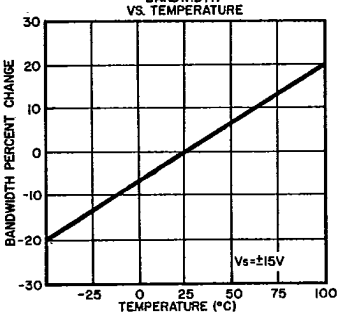
SLEW RATE VS. CAPACITANCE



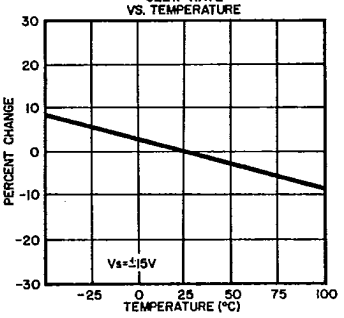
NON-LINEARITY VS. FREQUENCY



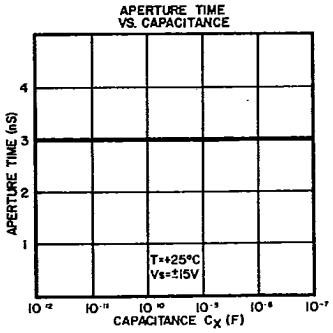
BANDWIDTH VS. TEMPERATURE



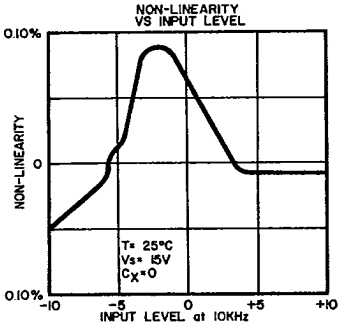
SLEW RATE VS. TEMPERATURE



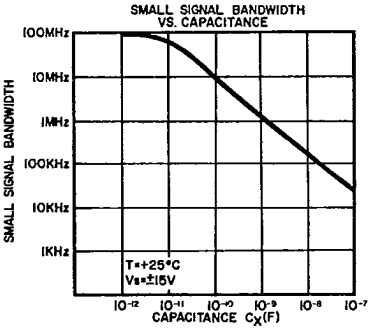
APERTURE TIME VS. CAPACITANCE



NON-LINEARITY VS INPUT LEVEL



SMALL SIGNAL BANDWIDTH VS. CAPACITANCE



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Clearly, the 5025 is slanted toward higher frequency applications. This becomes quite obvious when the acquisition times and, as shown above, the slew rate are considered. Where the acquisition time for the 5021 is guaranteed at 1μs for a Cx of 100pF, the 5025 is considerably faster, with an acquisition time of 30ns at a Cx of 10pF. Settling time, or the time to reach 0.1% of the intended value, is also much faster for the 5025 at 50ns (Cx=10pF) while the 5021 clocks in at 1.4μs with the Cx of 100pF.

In general, both devices will perform faster at smaller input voltage. This is interpreted to mean that with decreasing sample voltages, sampling rates can be imroved. Also, of course, the bandwidth increases with smaller charge capacitors.

The command signals for both devices i.e. the signals that operate the built-in semiconductor switch, are TTL compatible. Threshold condition is active high at voltages above +2.0 volts. Sampling is done at a logic low, or voltages below 0.8 volts. The devices present one TTL load.

FUNCTIONAL DESCRIPTION AND APPLICATIONS

The 5021 or the 5025 are semiconductor devices of hybrid construction. They both are pin for pin compatible. The 5025, however, exhibits parameters that make it applicable at higher frequency signals than its functional twin, the 5021.

Both devices are Sample and Hold Analog Memories with unity gain from input to output. As the block diagram in figure 1 show, they consist functionally of three distinct parts.

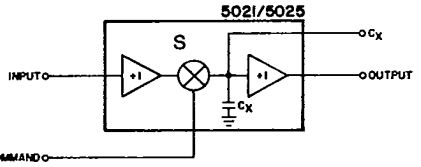

FIGURE 1: FUNCTIONAL BLOCK DIAGRAM

The signal to be sampled is applied to the front end buffer B1. The very fast input buffer provides a unity gain amplification to the signal and delivers a charge current, via the switch S, to the internal charge capacitor Cx, which can be altered by a capacitor connected to the device. Thus the devices can be tailored to nearly any desirable condition. The capacitor should be connected between pin 3 and analog common.

Switch S is a semiconductor device that, as noted before, is driven by typical TTL logic levels.

The voltage on the capacitor is sampled by an FET follower amplifier. This output amplifier also provides a unity gain. Thus, overall gain from input to output is unity. This output stage will provide a drive current of ±30m A, sufficient to allow elimination of driver buffers in many applications.

The devices are bipolar i.e. they allow application of voltages from -10 volts to +10 volts at the input for the sample and hold process.

The following description is applicable to both the 5021 and the 5025. However, it should be remembered that the 5025 should be used where speed and bandwidth considerations are most important, because it is the faster of the two devices.

Initially, it can be assumed that the command line is held at TTL logic high and the switch is open. Thus, the input voltage cannot reach the charge capacitor Cx. With the switch closed (command line logic low), the signal can, via the input buffer, reach the charge capacitor. When the capacitor has charged, the switch can be opened to retain that voltage on the capacitor and the output of the device then presents this value via the FET buffer. It must be remembered that, even though the output stage is designed for a ±30mA drive current, high current demand on the output influences the gain and it will drop below unity if the current exceeds specified values.

When designing with the 5021 or the 5025, the droop rate or memory decay must, of course, be taken into account. To decrease memory decay and at the same time increase the acquisition time of the device, Cx can be increased. As for all sample and hold applications, capacitors exhibiting low leakage and low dielectric absorption should be used for Cx. Typically, capacitors with polysterene, Teflon®, polycarbonate, polypropilene or MOS dielectric are best suited. To aid in the selection of values, typical performance curves are given, which show the influence of Cx on memory decay and aperture time in the section for typical performance curves. Values are given for both devices.

The power supply leads in the 5021 and the 5025 are internally decoupled. Therefore, no external bypass capacitors are needed. If other wideband devices are connected to the same power supply lines, use of a high capacitance, solid tantalum, bypass capacitor becomes a necessity. Values of 1 to 15μF are recommended. Positive and negative supply lines should be bypassed and connections should be made as closely as possible to the memory devices.

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MULTIPLEXED INPUT

Since these peak sense and hold memories are capable of such high speed operation, they are naturals to be teamed with other high speed devices. For instance, circuit complexity can be reduced if several different signals must be sampled, as shown in figure 2.

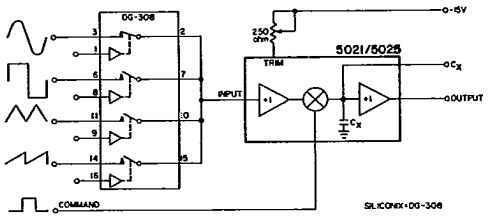


FIGURE 2: SAMPLE AND HOLD, MULTIPLEXED INPUTS

A multiplexer, or in this case, a quad analog switch, can be used and the output tied to the input of either the 5021 or 5025.

Quad SPST CMOS analog switches that can qualify are the DG308, produced by Siliconix or the H1201 from Harris. Typical turn on and turn off times are 130 nanosecond and 90 nanosecond for the Siliconix device and 185 nanosecond and 220 nanosecond for the Harris device. Of course, these high switching speeds may not be needed in a particular application. One of these devices will allow four signals to be accessed. Of course, they can be ganged if more than four signals need to be processed. Switches as well as the sample and hold memories can be controlled from a command center, consisting of discrete logic, a minicomputer, or microprocessor. Commands can be sent to the memory device to either sample or hold by operating the switch S. The sampled voltage, fed to the hold capacitor, is then routed to the output via the FET follower and presented to an oscilloscope, DVM, analog to digital converter, or other device. Trim adjustments allow accurate offset nulling. The choice of Cx is critical in any application where the full bandwidth of the device is needed. Also, of course, with increasing values of Cx, the acquisition time increases and the memory decay decreases, trade offs that must be considered when Cx is selected.

In this and all applications, a provision for trimming can be made. A 250 ohm potentiometer connected between the negative power supply rail and the trim pin will give the necessary trimming range. Trimming should be accomplished under dynamic operating conditions as experience shows that a trim under static conditions will not hold when a dynamic input is provided.

X1000 SAMPLE AND HOLD

In another typical combination of devices shown in Figure 3, an AH0605, produced by OEI, is combined with the sample and hold memory devices because of the AH0605's excellent speed and bandwidth capabilities. This combination can be used when the voltage to be sampled is too low to fit inside the specification limits of the 5021 or the 5025.

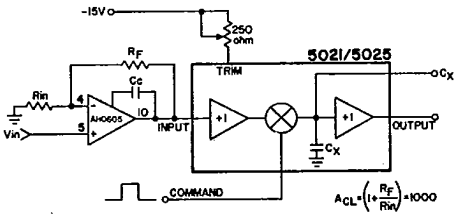


FIGURE 3: X1000 SAMPLE & HOLD

The circuit shown in figure 4 provides a gain of 1000 when the ratio of R_{in}/R_F = 999. Here, as in other applications, analog command and digital command common can be tied together. This should be done at one point only. Although not a necessity, it is helpful to bypass the power supply lines near the two devices. Cx can be increased if the acquisition time needs to be extended or the memory decay rate be improved. Refer to the last application of this series for an example of decay rate improvement without the attendant penalties of decreased bandwidth and longer acquisition times.

INTEGRATOR WITH RESET

Figure 4 shows the 5021 and the 5025 in an application with an integrator.

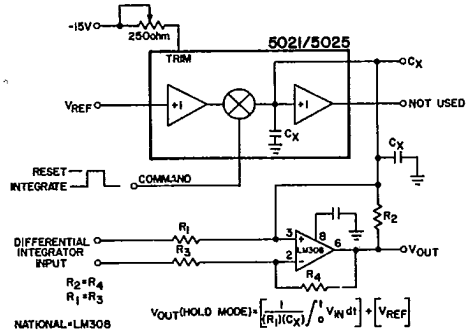


FIGURE 4: INTEGRATOR WITH PROGRAMMABLE RESET LEVEL

The integrator sets initial conditions, Cx is located at the summing node of the noninverting input of the integrator and only its charging function is used. In essence the 5021 or 5025 function as a charge control for Cx. Thus a signal can be sampled and its amplitude superimposed on the initial conditions set by the integrator. The circuit can also be used to set a given zero crossing to another i.e.: if there is a differential voltage between the sampled signal and the point where that sample should be further processed, the integrator can operate as a level adjuster.

FAST ACQUISITION, LOW DROOP

A very interesting circuit is presented in figure 5. This circuit allows the user to take full advantage of the rapid sampling capabilities of the 5021, or the even faster 5025, and still allows interface to devices with slower processing speeds, such as analog to digital (A/D) converters. This then makes possible use of slower and thus less expensive devices, rather than the faster and much more expensive flash converters.

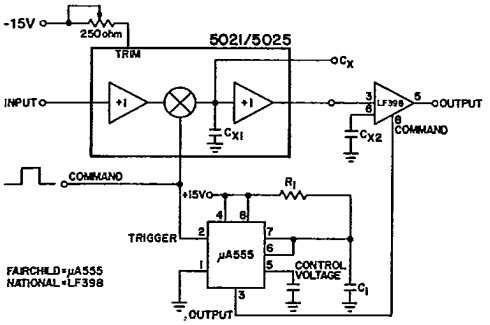


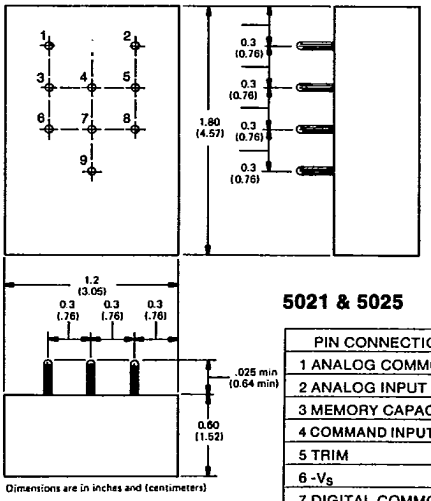
FIGURE 5: FAST ACQUISITION, LOW DROOP SAMPLE AND HOLD

As shown the circuit consists essentially of 5 parts. The 5021 or 5025, the first charge capacitor Cx_1, a timing device, the second charge capacitor. Cx_2, and a monolithic sample and hold device. In operation the OEI devices are set to work at or near the limits of their characteristics. Very rapid sample operations require small values of Cx_1 and thus will also result in relatively rapid decay of the voltage on this capacitor. To lengthen the overall droop rate the 5021/5025 is backed up with a slower sample and hold device which is outfitted with a larger Cx_2. This then increases the acquisition time and improves memory decay rates.

Improvements orders of magnitude are possible with this arrangement. Thus an A/D converter that could follow the two sample and hold devices can be much slower, the accuracy is maintained, and the very high speed of the data acquisition can still be taken advantage of. The A/D converter should however not exceed 8 bits of conversion because the error on the 5021/5025 can be around 2% and the sample and hold error of the slower device must still be added to this.

In operation the command to sample a very high speed, high bandwidth signal triggers the 555 as well. The 555 is connected as a monostable flip-flop with a time constant sufficiently large, to allow the charge capacitor of the slower sample and hold circuit to charge fully and thus complete the sampling process. Of course, if the 5021/5025 were controlled from a microprocessor, the sample and hold commands could be served by an interrupt routine, triggered by the comparator, but this circuit frees the μP from yet an additional chore and more software with the associated overhead.

MECHANICAL DESCRIPTION: The 5021 and 5025 use an epoxy encapsulant and are enclosed in glass-fiber-filled diallyl-phthalate cases. Their pins are gold-plated per MIL-G-45204, Type 2, Class 2. They are 0.040 inches (0.102 cm) in diameter.



5021 & 5025

PIN CONNECTIONS
1 ANALOG COMMON
2 ANALOG INPUT
3 MEMORY CAPACITOR
4 COMMAND INPUT
5 TRIM
6 $-V_S$
7 DIGITAL COMMON
8 $+V_S$
9 OUTPUT

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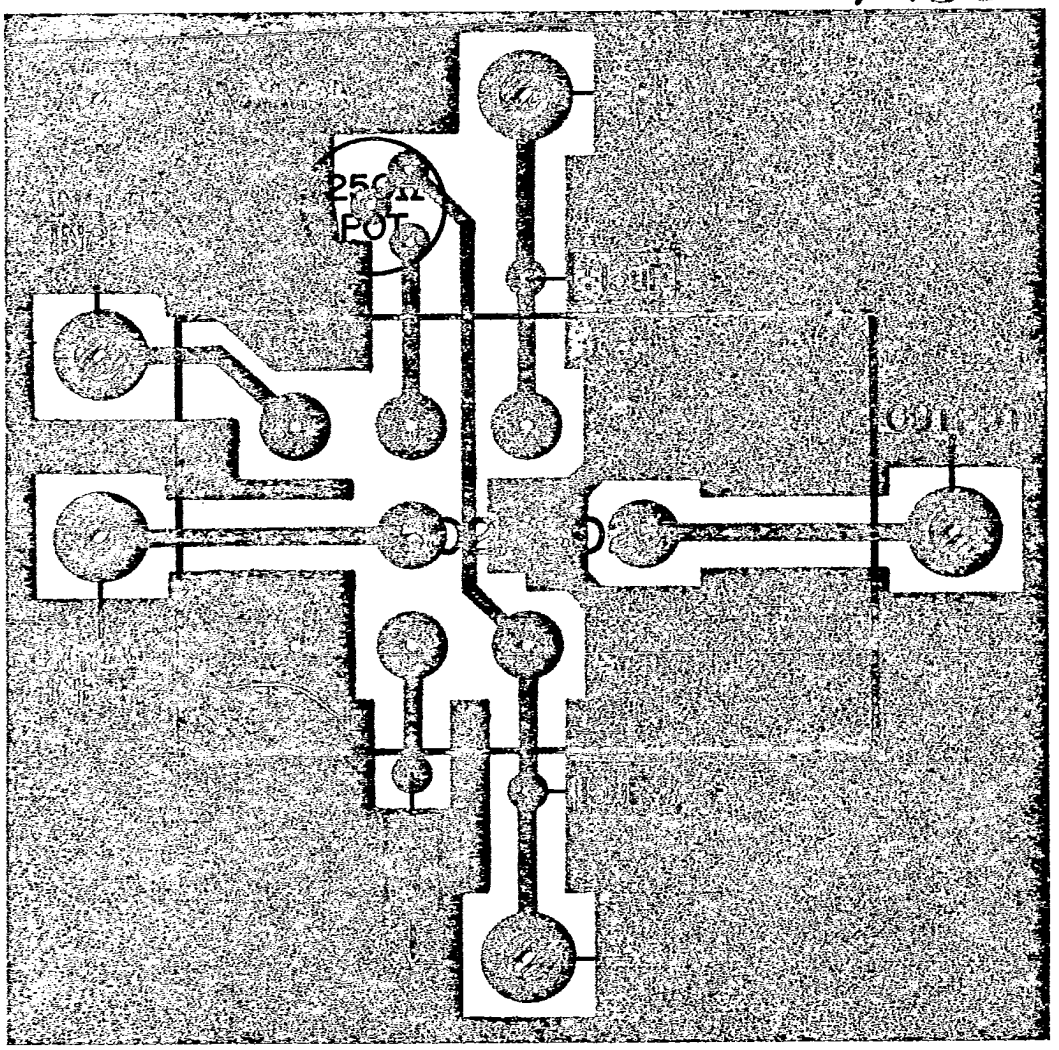

VIEW FROM THE PRINTED CIRCUIT SIDE

FIGURE 6 TYPICAL BOARD LAYOUT

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