525-832

LT1028

Ultra-Low Noise Precision High Speed Op Amp

FEATURES

- Voltage Noise 1.1nV/√Hz Max. at 1kHz; 0.85nV/√Hz Typ. at 1kHz; 1.0nV/√Hz Typ. at 10Hz; 35nVp-p Typ., 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product 50MHz Min.
- Slew Rate 11V/μs Min.
- Offset Voltage 40μV Max.
- Voltage Gain 7 Million Min.
- Drift with Temperature 0.8μV/°C Max.

APPLICATIONS

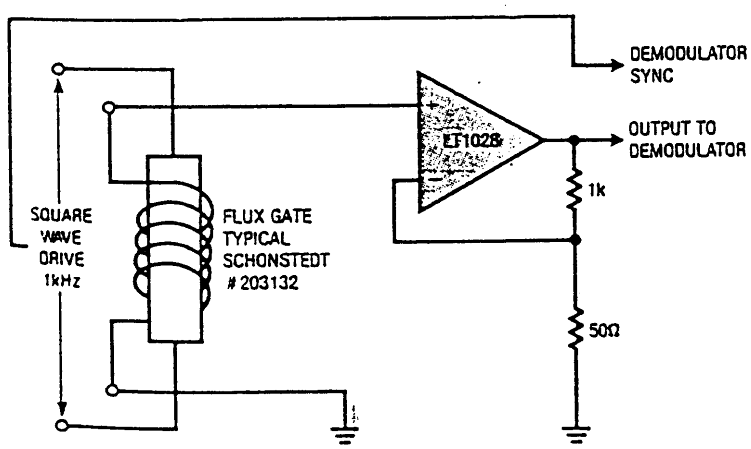
- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

DESCRIPTION

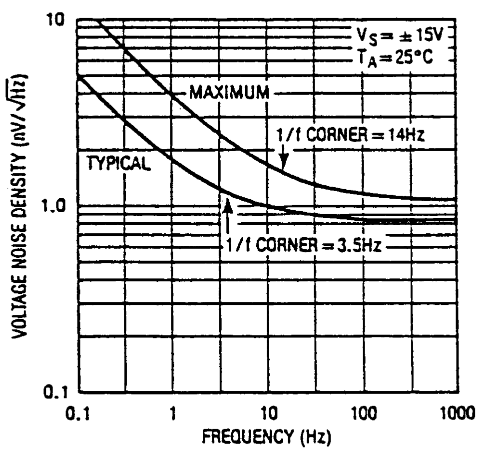
The LT1028 achieves a new standard of excellence in noise performance with 0.85nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz), distortion free output, and true precision parameters (0.1μV/°C drift, 10μV offset voltage, 30 million voltage gain). Although the LT1028 input stage operates at nearly 1mA of collector currents to achieve low voltage noise, input bias current is only 25nA.

The LT1028's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028's contribution to total system noise will be negligible.

Flux Gate Amplifier



Voltage Noise vs Frequency



ABSOLUTE MAXIMUM RATINGS

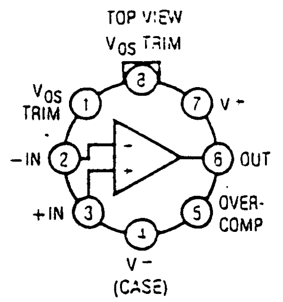
Supply Voltage
- −55°C to 105°C .... ±22V
- 105°C to 125°C .... ±16V

Differential Input Current (Note 8) .... ±25mA
Input Voltage ....Equal to Supply Voltage
Output Short Circuit Duration ....Indefinite
Operating Temperature Range
- LT1028AM, M .... −55°C to 125°C
- LT1028AC, C ....0°C to 70°C

Storage Temperature Range
- All Devices .... −65°C to 150°C

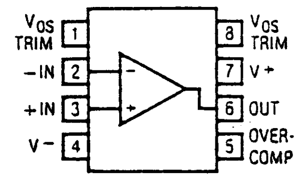
Lead Temperature (Soldering, 10 sec.) ....300°C

PACKAGE/ORDER INFORMATION



H8 PACKAGE TO-5 METAL CAN

ORDER PART NUMBER: LT1028AMH, LT1028MH, LT1028ACH, LT1028CH



J8 PACKAGE HERMETIC DIP
N8 PACKAGE PLASTIC DIP

ORDER PART NUMBER: LT1028AMJ8, LT1028MJ8, LT1028ACJ8, LT1028CJ8, LT1028ACN8, LT1028CN8

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028AM/AC MIN	LT1028AM/AC TYP	LT1028AM/AC MAX	LT1028M/C MIN	LT1028M/C TYP	LT1028M/C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		10	40		20	80	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Note 2)		0.3			0.3		μV/Mo
I_{OS}	Input Offset Current	$V_{CM} = 0V$		12	50		18	100	nA
I_B	Input Bias Current	$V_{CM} = 0V$		±25	±90		±30	±180	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		35	75		35	90	nVp-p
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 4) $f_o = 1000Hz$, 100% tested		1.0 0.85	1.7 1.1		1.0 0.9	1.9 1.2	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	$f_o = 10Hz$ (Notes 3 and 5) $f_o = 1000Hz$, 100% tested		4.7 1.0	10.0 1.6		4.7 1.0	12.0 1.8	pA/√Hz pA/√Hz
	Input Resistance Common-Mode Differential Mode			 300 20			 300 20		 MΩ kΩ
	Input Capacitance			5			5		pF
	Input Voltage Range		±11.0	±12.2		±11.0	±12.2		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm11V$	114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	117	133		110	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm12V$ $R_L \geq 1k\Omega$, $V_o = \pm10V$ $R_L \geq 600\Omega$, $V_o = \pm10V$	7.0 5.0 3.0	30.0 20.0 15.0		5.0 3.5 2.0	30.0 20.0 15.0		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.3 ±11.0	±13.0 ±12.2		±12.0 ±10.5	±13.0 ±12.2		V V
SR	Slew Rate	$A_{VCL} = -1$	11	15		11	15		V/μs
GBW	Gain-Bandwidth Product	$f_o = 20kHz$ (Note 6)	50	75		50	75		MHz
Z_o	Open Loop Output Impedance	$V_o = 0$, $I_o = 0$		80			80		Ω
I_S	Supply Current			7.4	9.5		7.6	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AM MIN	LT1028AM TYP	LT1028AM MAX	LT1028M MIN	LT1028M TYP	LT1028M MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		30	120		45	180	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	0.8		0.25	1.0	µV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		25	90		30	180	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±40	±150		±50	±300	nA
	Input Voltage Range		●	±10.3	±11.7		±10.3	±11.7		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm10.3V$	●	106	122		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm16V$	●	110	130		104	130		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_o = \pm10V$ $R_L \ge 1k\Omega$, $V_o = \pm10V$	●	3.0 2.0	14.0 10.0		2.0 1.5	14.0 10.0		V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±10.3	±11.6		±10.3	±11.6		V
I_S	Supply Current		●		8.7	11.5		9.0	13.0	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1028AC MIN	LT1028AC TYP	LT1028AC MAX	LT1028C MIN	LT1028C TYP	LT1028C MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		15	80		30	125	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.1	0.8		0.2	1.0	µV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		15	65		22	130	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±30	±120		±40	±240	nA
	Input Voltage Range		●	±10.5	±12.0		±10.5	±12.0		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm10.5V$	●	110	124		106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	●	114	132		107	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_o = \pm10V$ $R_L \ge 1k\Omega$, $V_o = \pm10V$	●	5.0 4.0	25.0 18.0		3.0 2.5	25.0 18.0		V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$ $R_L \ge 600\Omega$ (Note 9)	●	±11.5 ±9.5	±12.7 ±11.0		±11.5 ±9.0	±12.7 ±10.5		V V
I_S	Supply Current		●		8.0	10.5		8.2	11.5	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at $T_A = 25°C$, offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV.

Note 3: This parameter is tested on a sample basis only.

Note 4: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 5: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

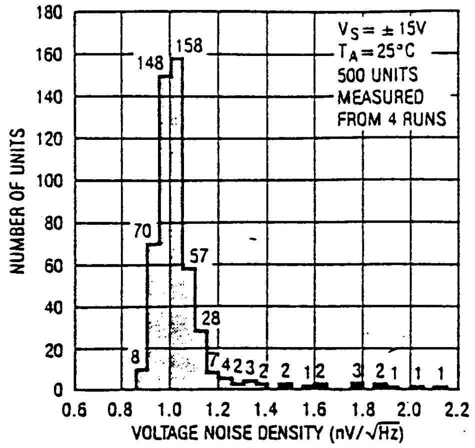
Note 7: This parameter is not 100% tested.

Note 8: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.8V, the input current should be limited to 25mA.

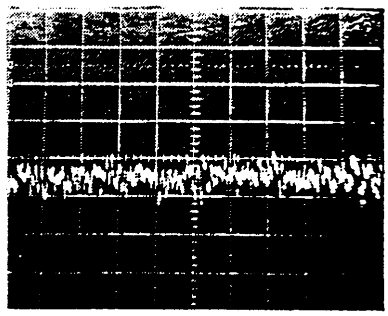
Note 9: This parameter guaranteed by design, fully warmed up at $T_A = 70°C$. It includes chip temperature increase due to supply and load currents.

TYPICAL PERFORMANCE CHARACTERISTICS

10Hz Voltage Noise Distribution

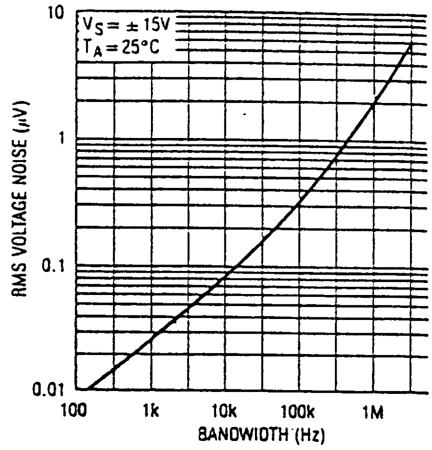


Wideband Noise, DC to 20kHz

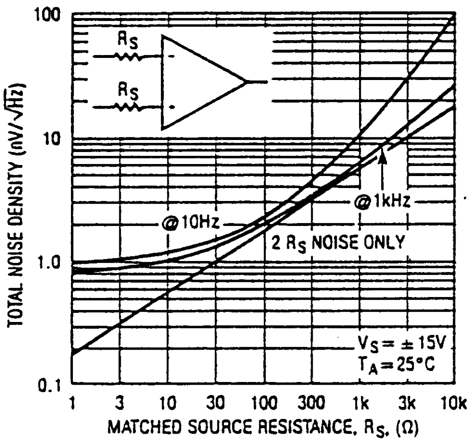


VERTICAL SCALE = 0.5μV/DIV
HORIZONTAL SCALE = 0.5ms/DIV

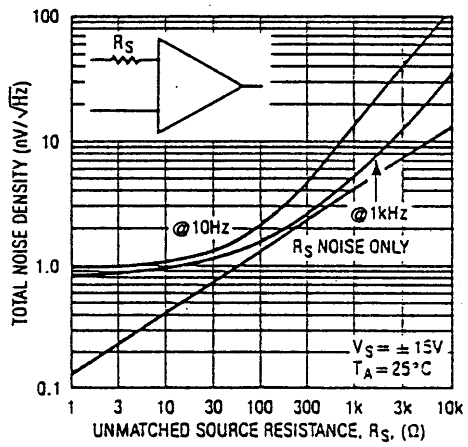
Wideband Voltage Noise (0.1Hz to Frequency Indicated)



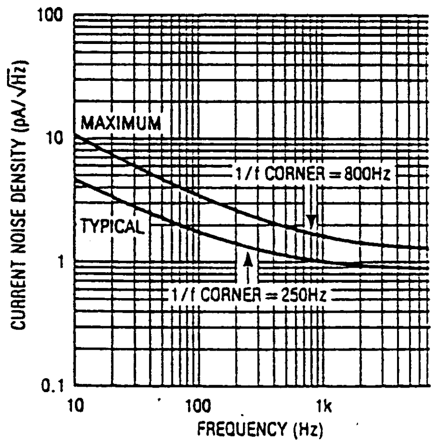
Total Noise vs Matched Source Resistance



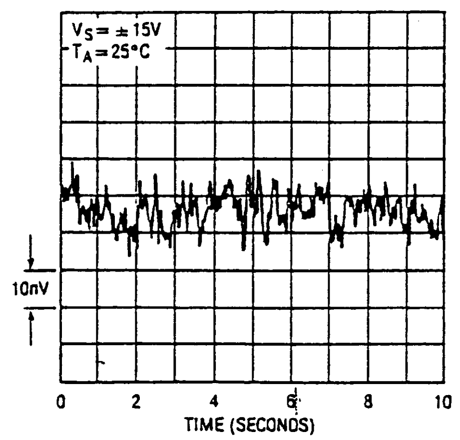
Total Noise vs Unmatched Source Resistance



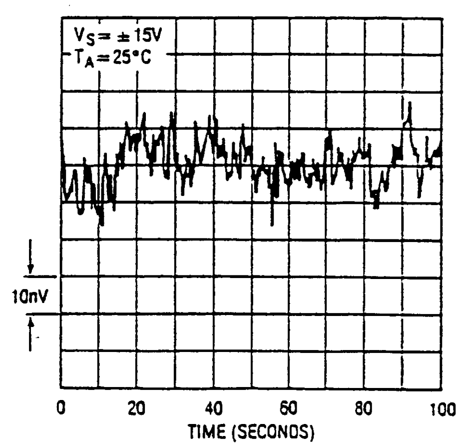
Current Noise Spectrum



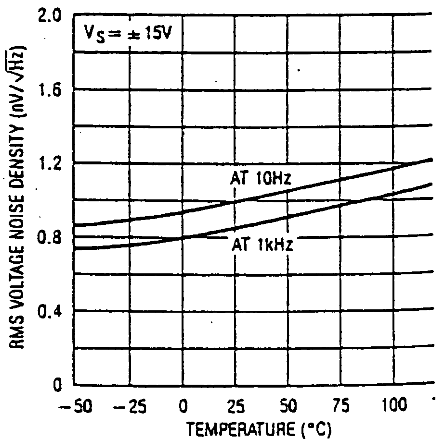
0.1Hz to 10Hz Voltage Noise



0.01Hz to 1Hz Voltage Noise

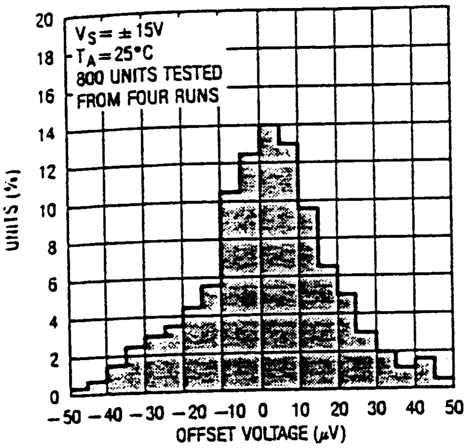


Voltage Noise vs Temperature

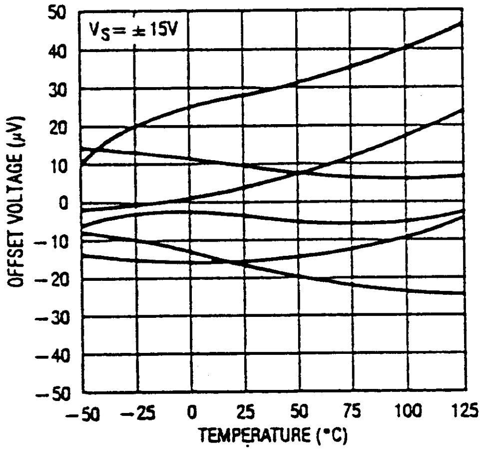


TYPICAL PERFORMANCE CHARACTERISTICS

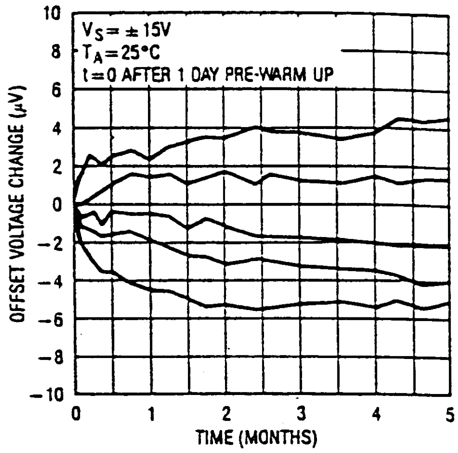
Distribution of Input Offset Voltage



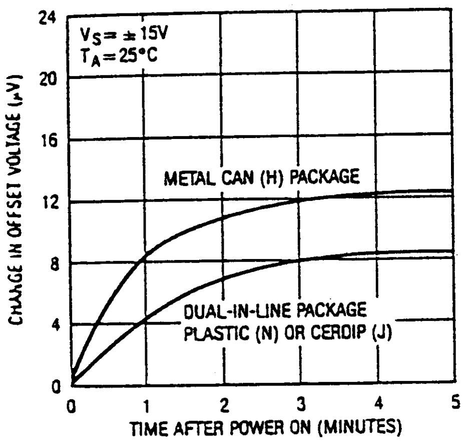
Offset Voltage Drift with Temperature of Representative Units



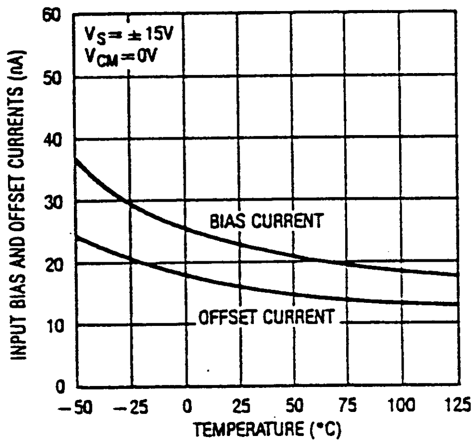
Long Term Stability of Five Representative Units



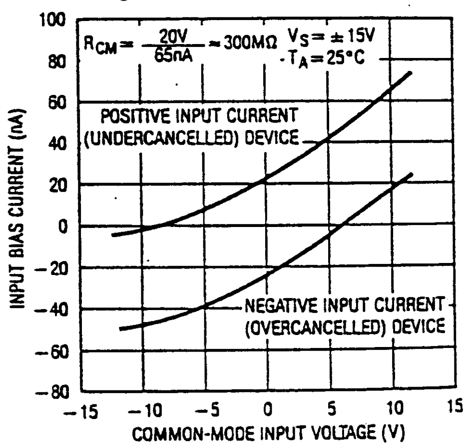
Warm-Up Drift



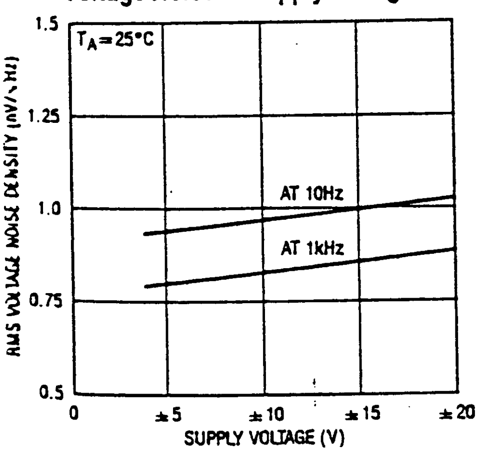
Input Bias and Offset Currents Over Temperature



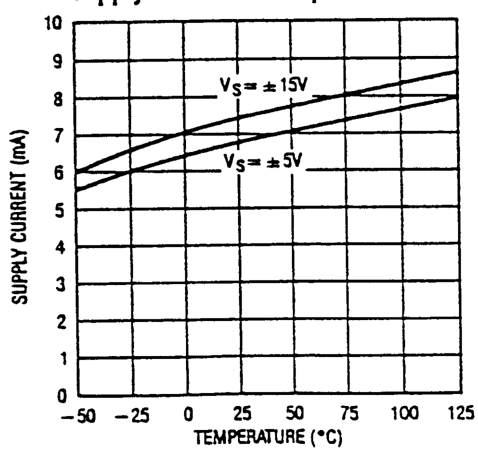
Bias Current Over the Common-Mode Range



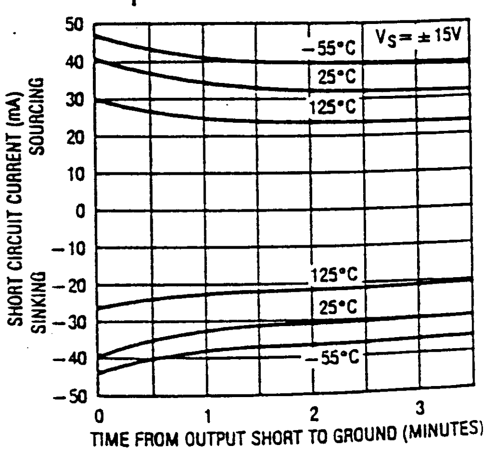
Voltage Noise vs Supply Voltage



Supply Current vs Temperature

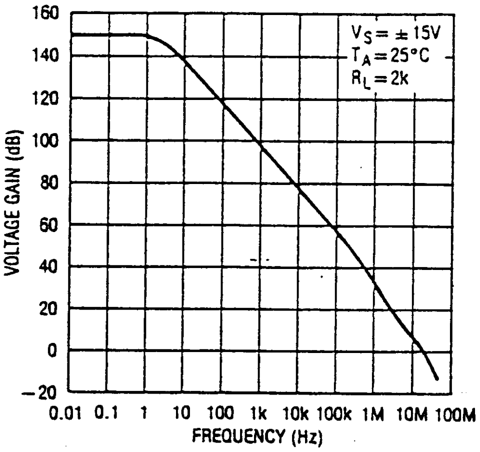


Output Short Circuit Current vs Time

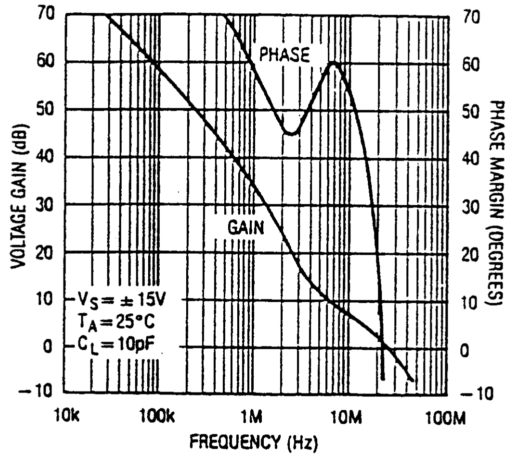


TYPICAL PERFORMANCE CHARACTERISTICS

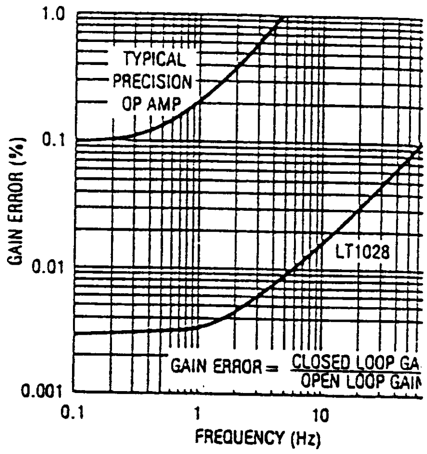
Voltage Gain vs Frequency



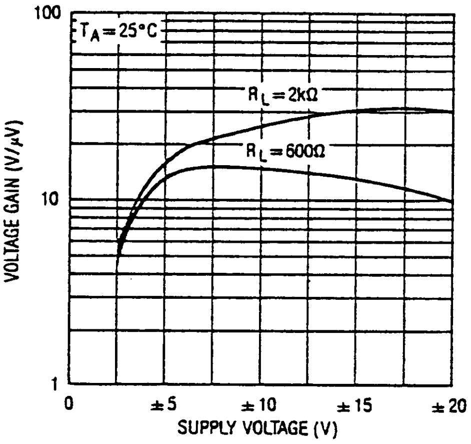
Gain, Phase vs Frequency



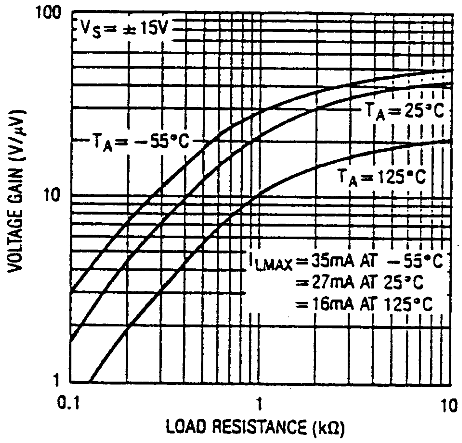
Gain Error vs Frequency
Closed Loop Gain = 1000



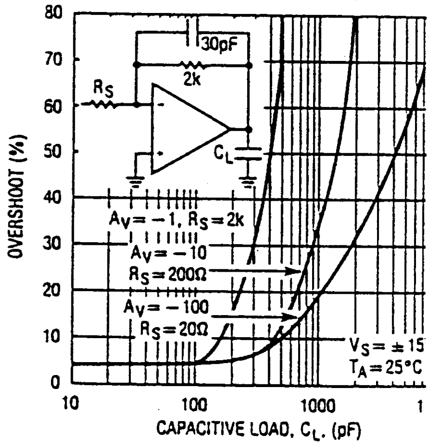
Voltage Gain vs Supply Voltage



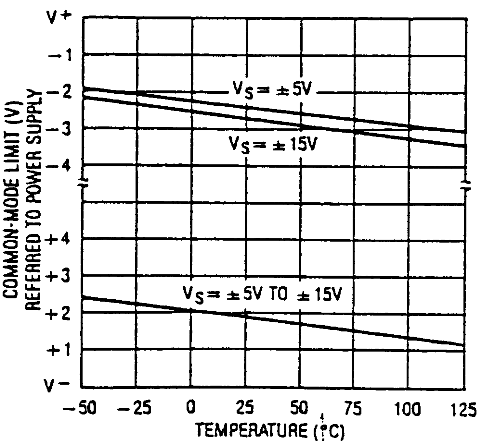
Voltage Gain vs Load Resistance



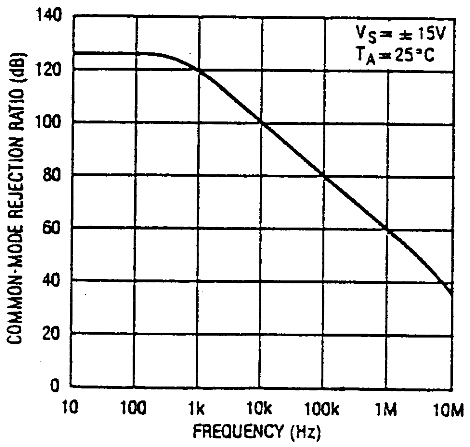
Capacitance Load Handling



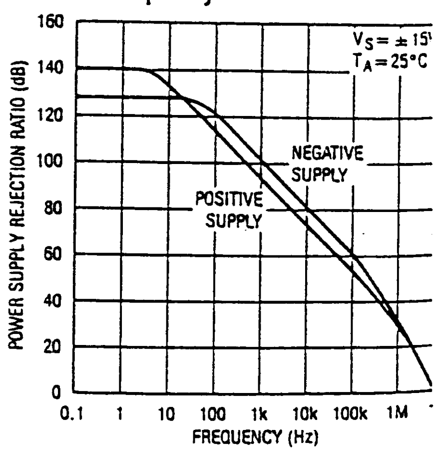
Common-Mode Limit Over Temperature



Common-Mode Rejection Ratio vs Frequency

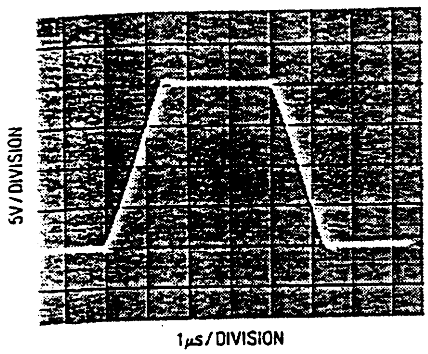


Power Supply Rejection Ratio vs Frequency



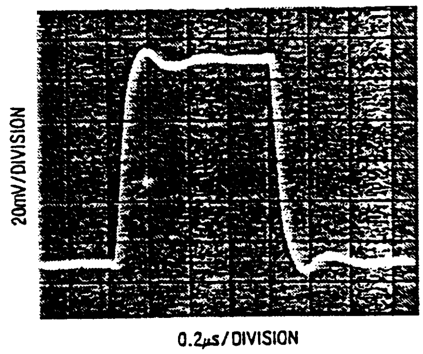
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Transient Response



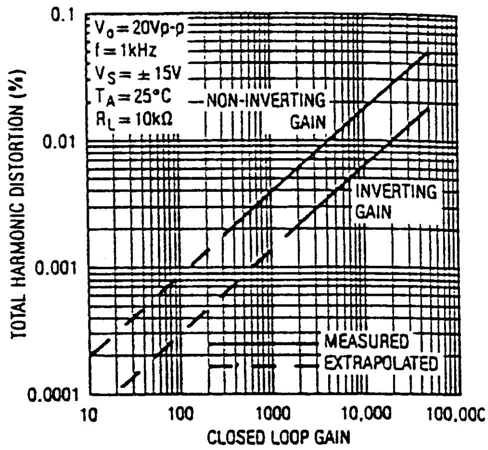
$A_V = -1$, $R_S = R_f = 2k$, $C_f = 30pF$

Small Signal Transient Response

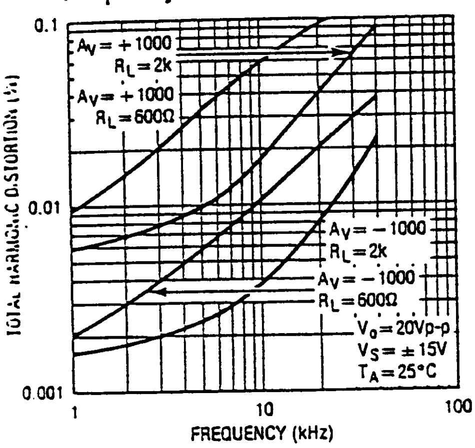


$A_V = -1$, $R_S = R_f = 2k\Omega$
$C_f = 30pF$, $C_L = 80pF$

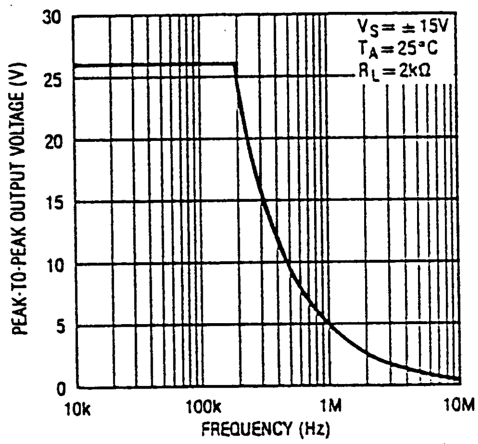
Total Harmonic Distortion vs Closed Loop Gain



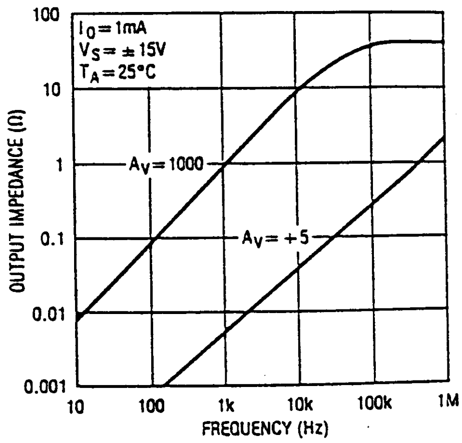
Total Harmonic Distortion vs Frequency and Load Resistance



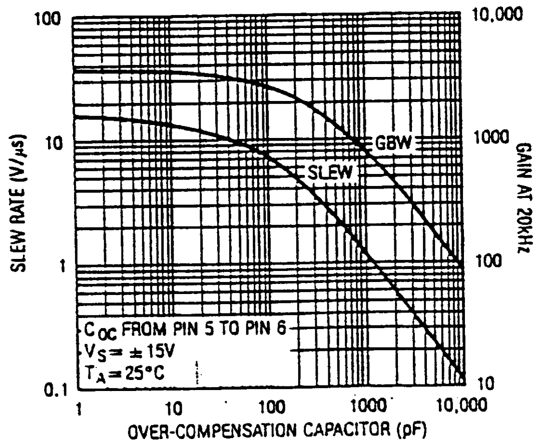
Maximum Undistorted Output vs Frequency



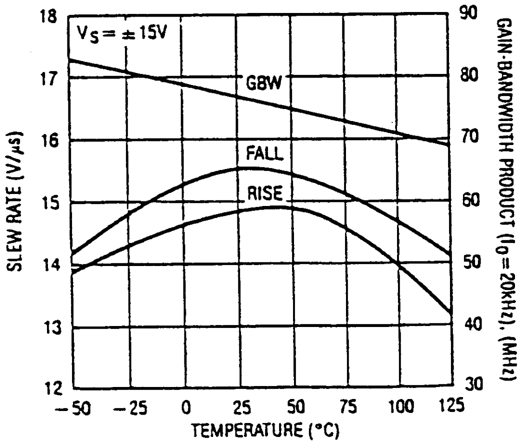
Closed Loop Output Impedance



Slew Rate, Gain-Bandwidth-Product vs Over-Compensation Capacitor



Slew Rate, Gain-Bandwidth Product Over Temperature



APPLICATIONS INFORMATION —NOISE

Voltage Noise vs Current Noise

The LT1028's less than $1nV/\sqrt{Hz}$ voltage noise is three times better than the lowest voltage noise heretofore available (on the LT1007/1037). A necessary condition for such low voltage noise is operating the input transistors at nearly 1mA of collector currents, because voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. Consequently, the LT1028's current noise is significantly higher than on most monolithic op amps.

Therefore, to realize truly low noise performance it is important to understand the interaction between voltage noise (e_n), current noise (i_n) and resistor noise (r_n).

Total Noise vs Source Resistance

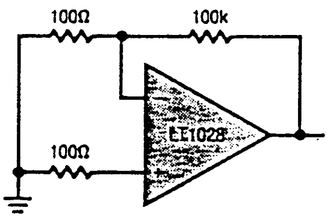
The total input referred noise of an op amp is given by

$$e_t = [e_n^2 + r_n^2 + (i_n R_{eq})^2]^{1/2}$$

where R_{eq} is the total equivalent source resistance at the two inputs

and $r_n = \sqrt{4kTR_{eq}} = 0.13\sqrt{R_{eq}}$ in $nV/\sqrt{Hz}$ at 25°C

As a numerical example, consider the total noise at 1kHz of the gain 1000 amplifier shown below.



$$R_{eq} = 100\Omega + 100\Omega \| 100k \approx 200\Omega$$
$$r_n = 0.13\sqrt{200} = 1.84nV/\sqrt{Hz}$$
$$e_n = 0.85nV/\sqrt{Hz}$$
$$i_n = 1.0pA/\sqrt{Hz}$$
$$e_t = [0.85^2 + 1.84^2 + (1.0 \times 0.2)^2]^{1/2} = 2.04nV/\sqrt{Hz}$$

output noise $= 1000\ e_t = 2.04\mu V/\sqrt{Hz}$

At very low source resistance ($R_{eq} < 40\Omega$) voltage noise dominates. As R_{eq} is increased resistor noise becomes the largest term—as in the example above—and the LT1028's voltage noise becomes negligible. As R_{eq} is further increased, current noise becomes important. At 1kHz, when R_{eq} is in excess of 20kΩ, the current noise component is larger than the resistor noise. The total noise versus matched source resistance plot illustrates the above calculations.

The plot also shows that current noise is more dominant at low frequencies, such as 10Hz. This is because resistor noise is flat with frequency, while the 1/f corner of current noise is typically at 250Hz. At 10Hz when $R_{eq} > 1k\Omega$, the current noise term will exceed the resistor noise.

When the source resistance is unmatched, the total noise versus unmatched source resistance plot should be consulted. Note that total noise is lower at source resistances below 1kΩ because the resistor noise contribution is less. When $R_S > 1k\Omega$ total noise is not improved, however. This is because bias current cancellation is used to reduce input bias current. The cancellation circuitry injects two correlated current noise components into the two inputs. With matched source resistors the injected current noise creates a common-mode voltage noise and gets rejected by the amplifier. With source resistance in one input only, the cancellation noise is added to the amplifier's inherent noise.

In summary, the LT1028 is the optimum amplifier for noise performance—provided that the source resistance is kept low. The following table depicts which op amp manufactured by Linear Technology should be used to minimize noise—as the source resistance is increased beyond the LT1028's level of usefulness.

Best Op Amp for Lowest Total Noise vs Source Resistance

SOURCE RESISTANCE (Note 1)	BEST OP AMP AT LOW FREQ (10Hz)	BEST OP AMP WIDEBAND (1kHz)
0 to 400Ω	LT1028	LT1028
400Ω to 4kΩ	LT1007/1037	LT1028
4kΩ to 40kΩ	LT1001	LT1007/1037
40kΩ to 500kΩ	LT1012	LT1001
500kΩ to 5MΩ	LT1012 or LT1055	LT1012
>5M	LT1055	LT1055

Note 1: Source resistance is defined as matched or unmatched, e.g., $R_S = 1k\Omega$ means: 1kΩ at each input, or 1kΩ at one input and zero at the other.

APPLICATIONS INFORMATION —NOISE

Noise Testing—Voltage Noise

The LT1028's RMS voltage noise density can be accurately measured using the Quan Tech Noise Analyzer, Model 5173 or an equivalent noise tester. Care should be taken, however, to subtract the noise of the source resistor used. Prefabricated test cards for the Model 5173 set the device under test in a closed loop gain of 31 with a 60Ω source resistor and a 1.8kΩ feedback resistor. The noise of this resistor combination is $0.13\sqrt{58} = 1.0\text{nV}/\sqrt{\text{Hz}}$. An LT1028 with $0.85\text{nV}/\sqrt{\text{Hz}}$ noise will read $(0.85^2 + 1.0^2)^{1/2} = 1.31\text{nV}/\sqrt{\text{Hz}}$. For better resolution, the resistors should be replaced with a 10Ω source and 300Ω feedback resistor. Even a 10Ω resistor will show an apparent noise which is 8-10% too high.

The 0.1Hz to 10Hz peak-to-peak noise of the LT1028 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 35nV peak-to-peak noise performance of the LT1028 requires special test precautions:

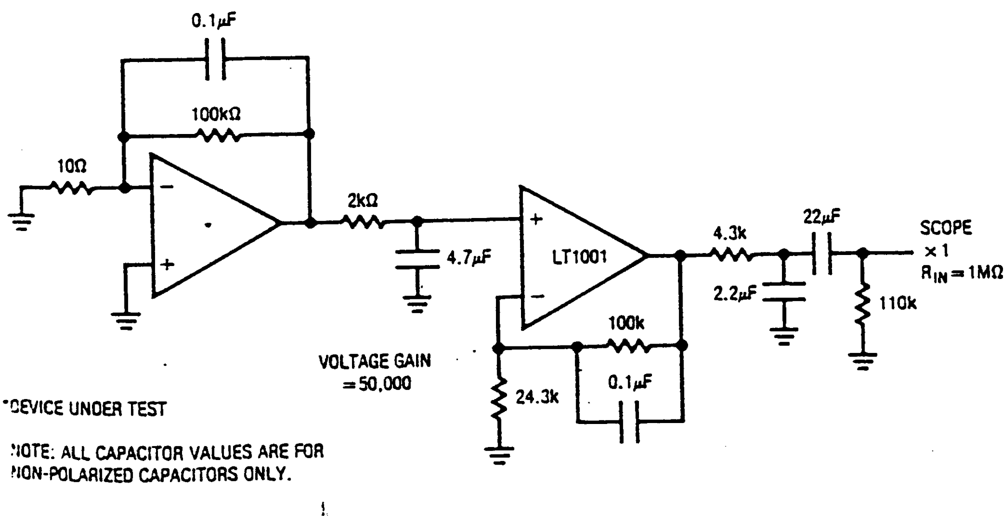
(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 10μV due to its chip temperature increasing 30°C to 40°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

(c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

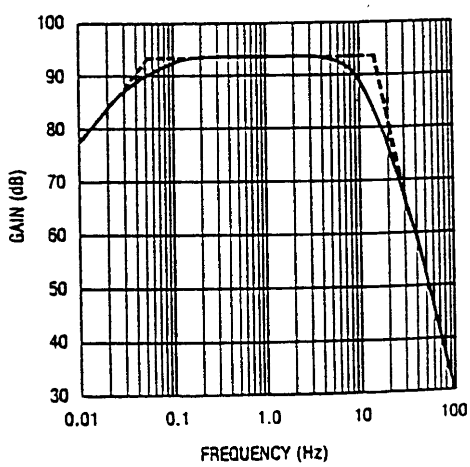
0.1Hz to 10Hz Noise Test Circuit



*DEVICE UNDER TEST

NOTE: ALL CAPACITOR VALUES ARE FOR NON-POLARIZED CAPACITORS ONLY.

0.1Hz to 10Hz p-p Noise Tester Frequency Response

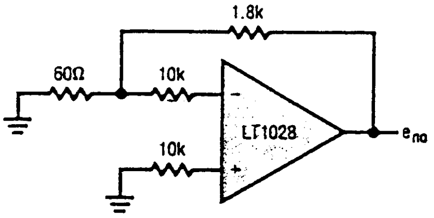


APPLICATIONS INFORMATION —NOISE

Noise Testing—Current Noise

Current noise density (i_n) is defined by the following formula, and can be measured in the circuit shown:

$$i_n = \frac{[e_{no}^2 - (31 \times 18.4nV/\sqrt{Hz})^2]^{1/2}}{20k \times 31}$$



If the Quan Tech Model 5173 is used, the noise reading is input-referred, therefore the result should not be divided by 31; the resistor noise should not be multiplied by 31.

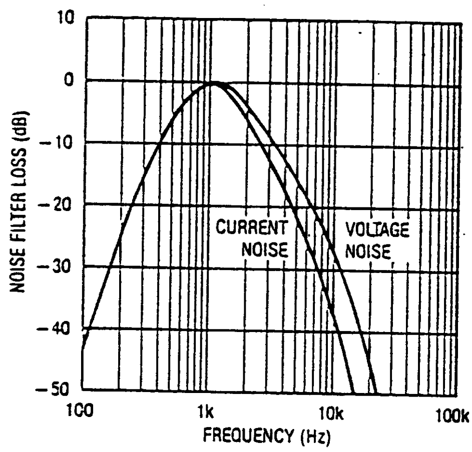
100% Noise Testing

The 1kHz voltage and current noise is 100% tested on the LT1028 as part of automated testing; the approximate frequency response of the filters is shown. The limits on the automated testing are established by extensive correlation tests on units measured with the Quan Tech Model 5173.

10Hz voltage noise density is sample tested on every lot. Devices 100% tested at 10Hz are available on request for an additional charge.

10Hz current noise is not tested on every lot but it can be inferred from 100% testing at 1kHz. A look at the current noise spectrum plot will substantiate this statement. The only way 10Hz current noise can exceed the guaranteed limits is if its 1/f corner is higher than 800Hz and/or its white noise is high. If that is the case then the 1kHz test will fail.

Automated Tester Noise Filter



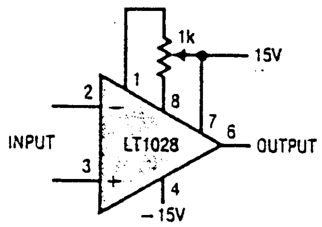
APPLICATIONS INFORMATION

General

The LT1028 series devices may be inserted directly into OP-07, OP-27, OP-37, LT1007 and LT1037 sockets with or without removal of external nulling components. In addition, the LT1028 may be fitted to 5534 sockets with the removal of external compensation components.

Offset Voltage Adjustment

The input offset voltage of the LT1028 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 1k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{OS}/300) μV/°C, e.g., if V_{OS} is adjusted to 300μV, the change in drift will be 1μV/°C.



The adjustment range with a 1k pot is approximately ±1.1mV.

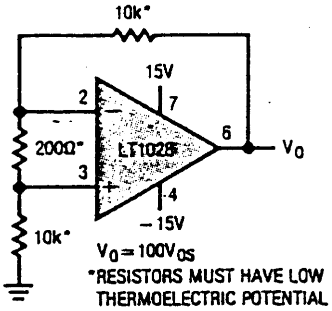
Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

APPLICATIONS INFORMATION

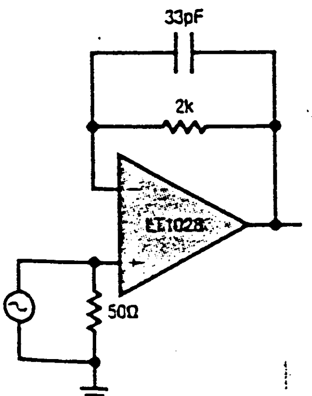
The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1028.

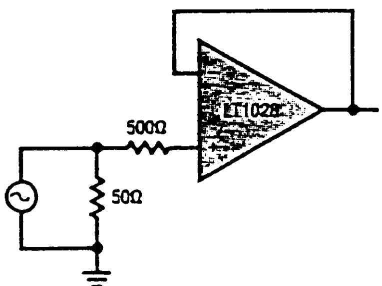
Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



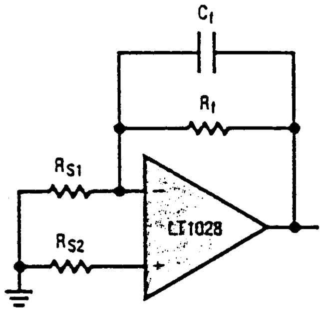
Frequency Response

The LT1028's Gain, Phase vs Frequency plot indicates that the device is stable in closed loop gains greater than +2 or −1 because phase margin is about 50° at an open loop gain of 6dB. In the voltage follower configuration phase margin seems inadequate. This is indeed true when the output is shorted to the inverting input and the non-inverting input is driven from a 50Ω source impedance. However, when feedback is through a parallel R-C network (provided $C_f < 68pF$), the LT1028 will be stable because of interaction between the input resistance and capacitance and the feedback network. Larger source resistance at the non-inverting input has a similar effect. The following voltage follower configurations are stable:



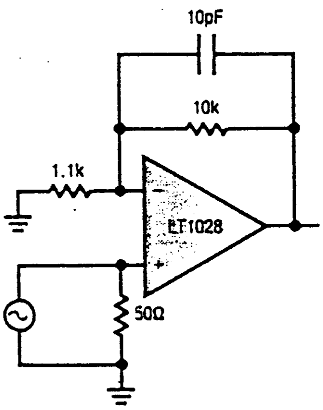


Another configuration which requires unity gain stabilit is shown below. When C_f is large enough to effectivel short the output to the input at 15MHz, oscillations can oc cur. The insertion of $R_{S2} \geq 500\Omega$ will prevent the LT102 from oscillating. When $R_{S1} \geq 500\Omega$, the additional nois contribution due to the presence of R_{S2} will be minimal When $R_{S1} \leq 100\Omega$, R_{S2} is not necessary, because R_{S1} repre sents a heavy load on the output through the C_f short When $100\Omega < R_{S1} < 500\Omega$, R_{S2} should match R_{S1}. For exam ple, $R_{S1} = R_{S2} = 300\Omega$ will be stable. The noise increase du to R_{S2} is 40%.



If C_f is only used to cut noise bandwidth, a similar effec can be achieved using the over-compensation terminal.

The Gain, Phase plot also shows that phase margin i about 45° at a gain of 10 (20dB). The following configur tion has a high (≈70%) overshoot without the 10p capacitor because of additional phaseshift caused by th feedback resistor—input capacitance pole. The presenc of the 10pF capacitor cancels this pole and reduces ove shoot to 5%.

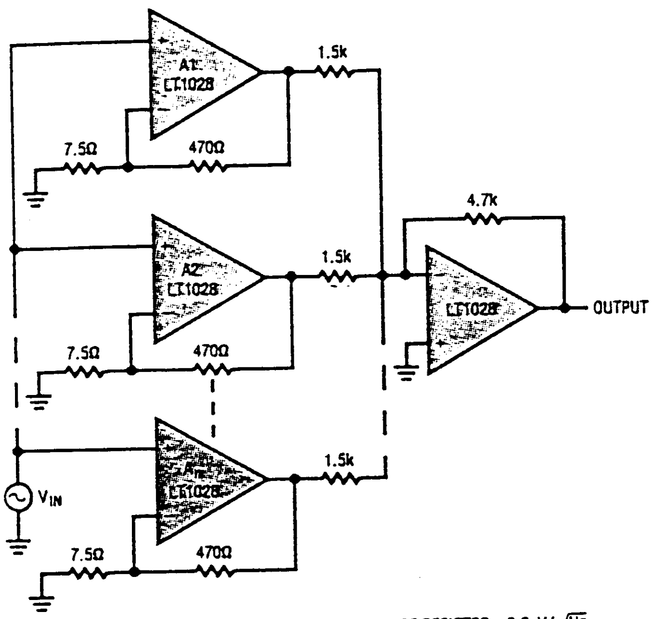


Over-Compensation

The LT1028 is equipped with a frequency over-compens tion terminal (pin 5). A capacitor connected between pin and the output will reduce noise bandwidth. Details ar shown on the Slew Rate, Gain-Bandwidth Product v Over-Compensation Capacitor plot. An additional benef is increased capacitive load handling capability.

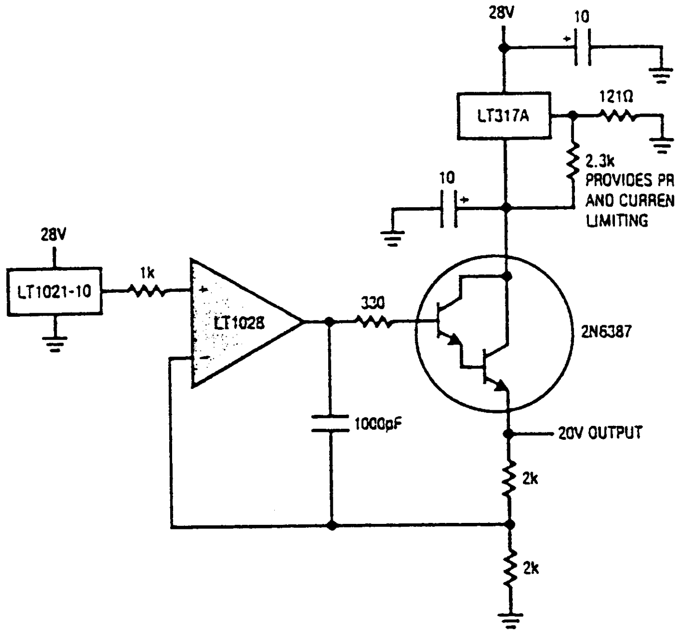
'PICAL APPLICATIONS

Paralleling Amplifiers to Reduce Voltage Noise

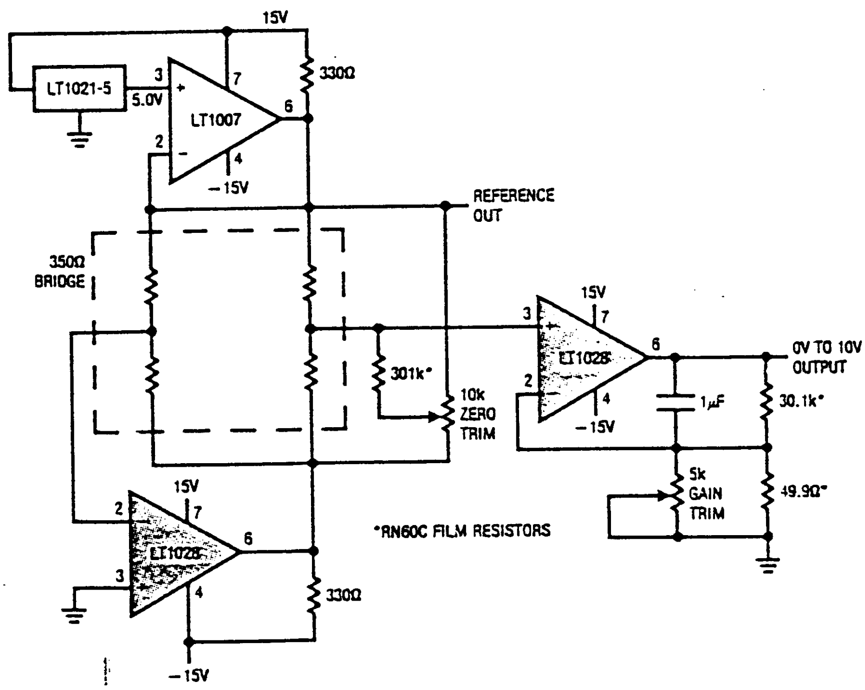


1. ASSUME VOLTAGE NOISE OF LT1028 AND 7.5Ω SOURCE RESISTOR = $0.9\text{nV}/\sqrt{\text{Hz}}$.
2. GAIN WITH n LT1028's IN PARALLEL = n × 200.
3. OUTPUT NOISE = $\sqrt{n} \times 200 \times 0.9\text{nV}/\sqrt{\text{Hz}}$.
4. INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \times 200} = \frac{0.9}{\sqrt{n}}$ $\text{nV}/\sqrt{\text{Hz}}$.
5. NOISE CURRENT AT INPUT INCREASES $\sqrt{n}$ TIMES.
6. IF n = 5, GAIN = 1000, BANDWIDTH = 1MHz, RMS NOISE, DC TO 1MHz, $= \frac{2\mu V}{\sqrt{5}} = 0.9\mu V$.

Low Noise Voltage Regulator



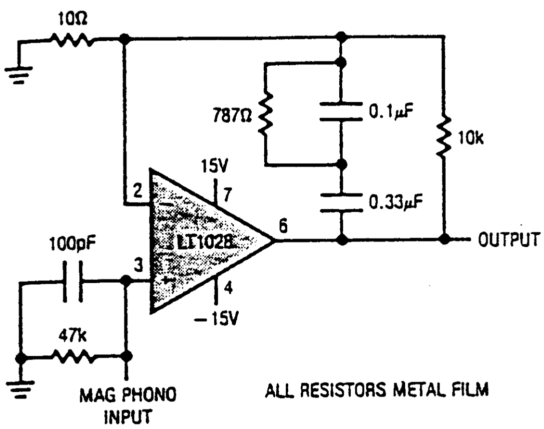
Strain Gauge Signal Conditioner with Bridge Excitation



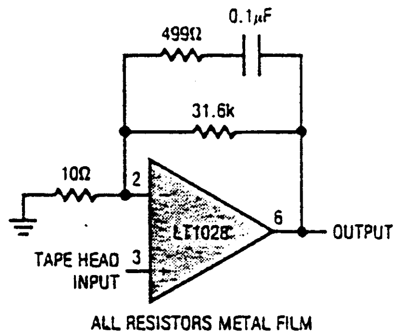
THE LT1028's NOISE CONTRIBUTION IS NEGLIGIBLE COMPARED TO THE BRIDGE NOISE.

TYPICAL APPLICATIONS

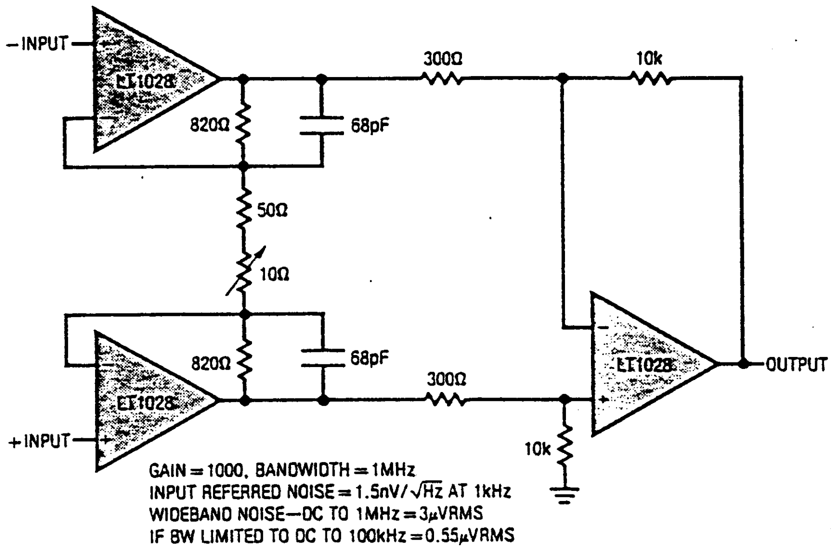
Phono Preamplifier



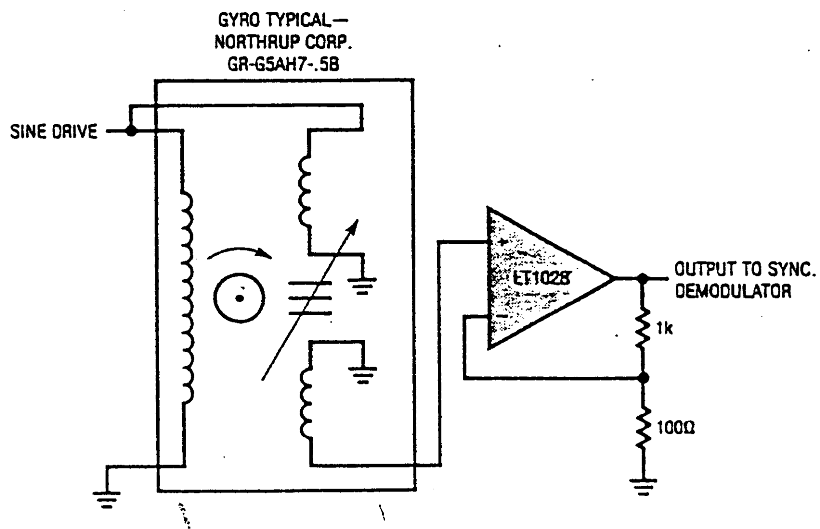
Tape Head Amplifier



Low Noise, Wide Bandwidth Instrumentation Amplifier

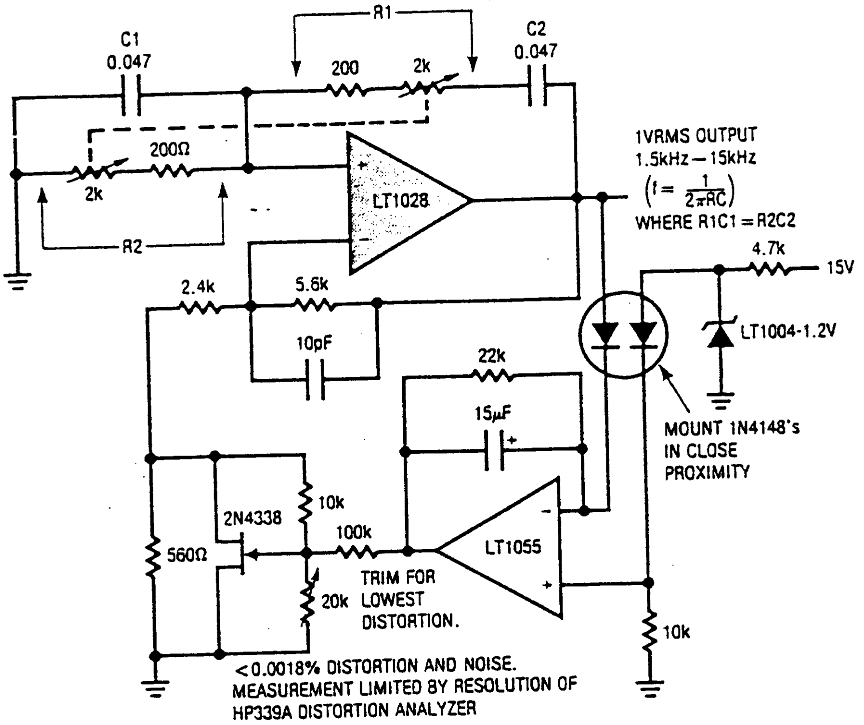


Gyro Pick-Off Amplifier

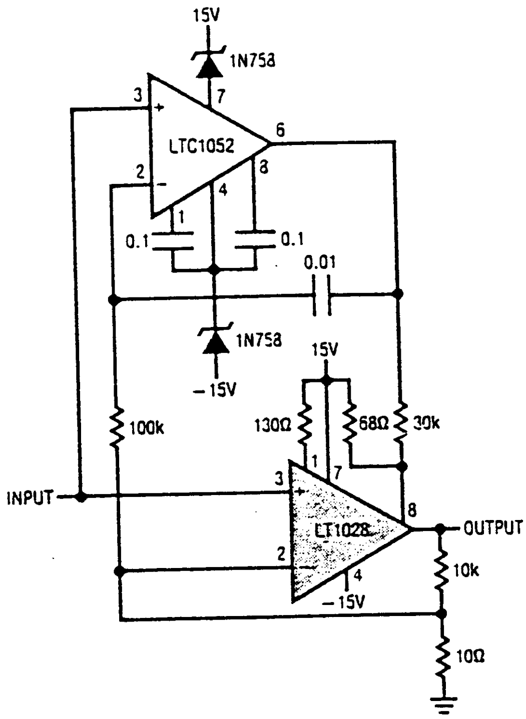


TYPICAL APPLICATIONS

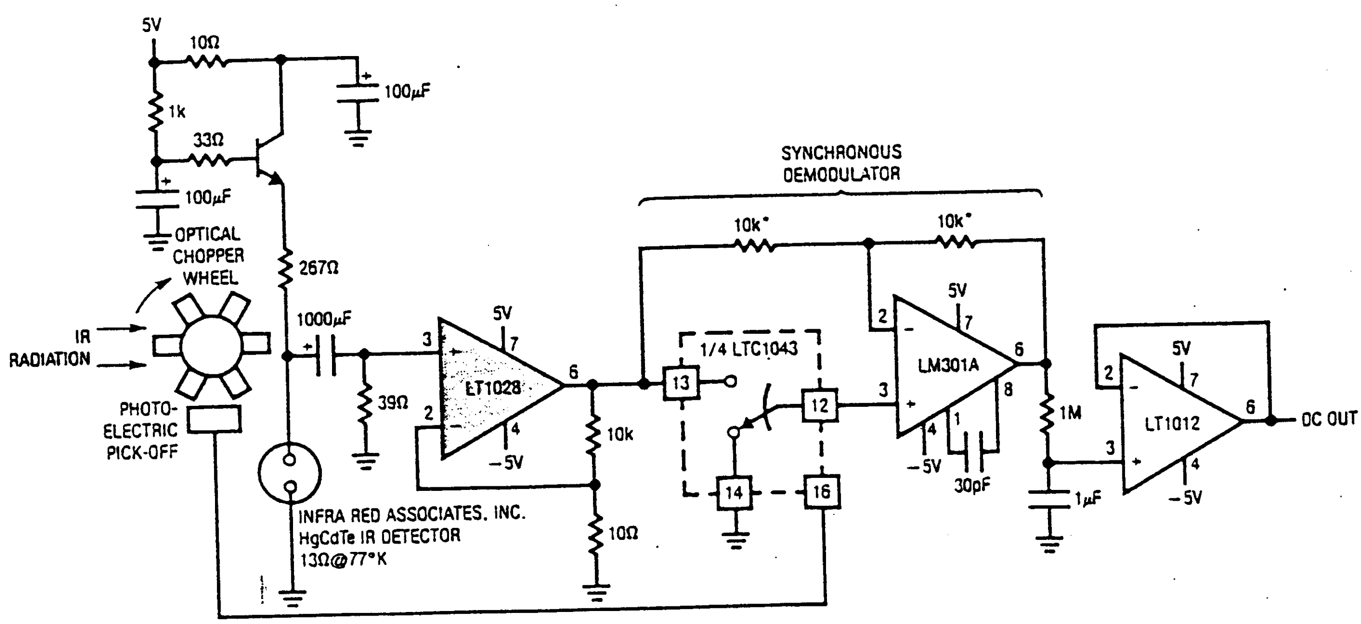
Super Low Distortion Variable Sine Wave Oscillator



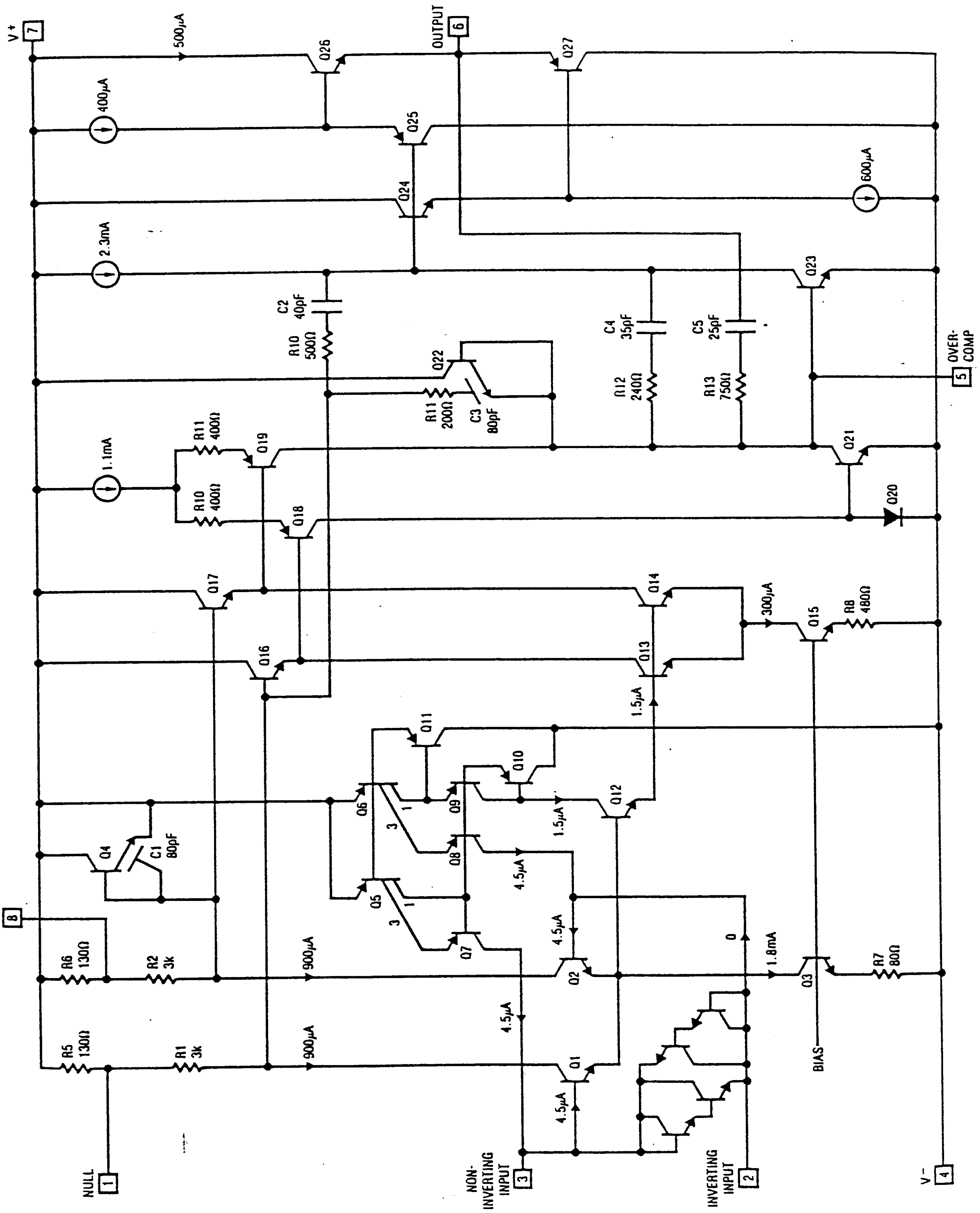
Chopper Stabilized Amplifier



Low Noise Infrared Detector



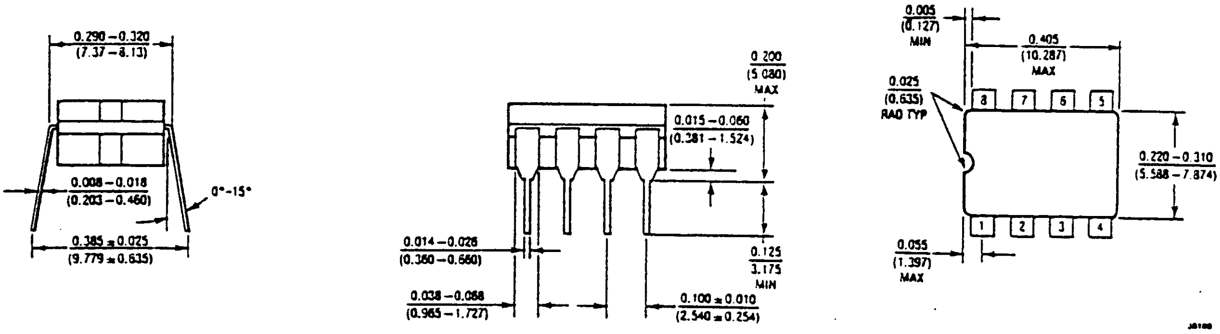
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTIONS

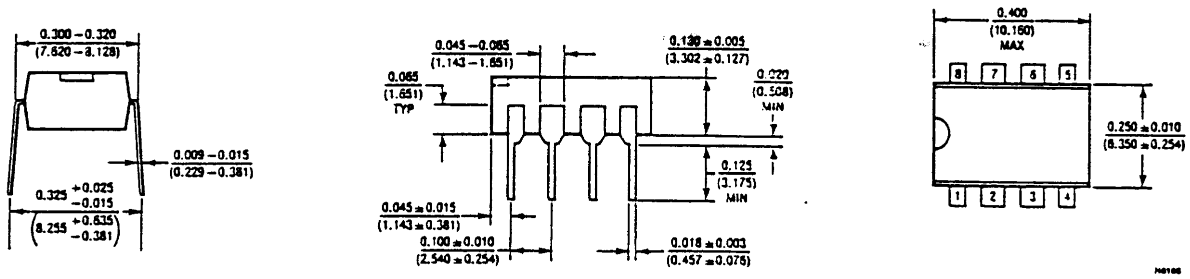
Dimensions in inches (millimeters) unless otherwise noted.

J Package
8-Lead Ceramic DIP



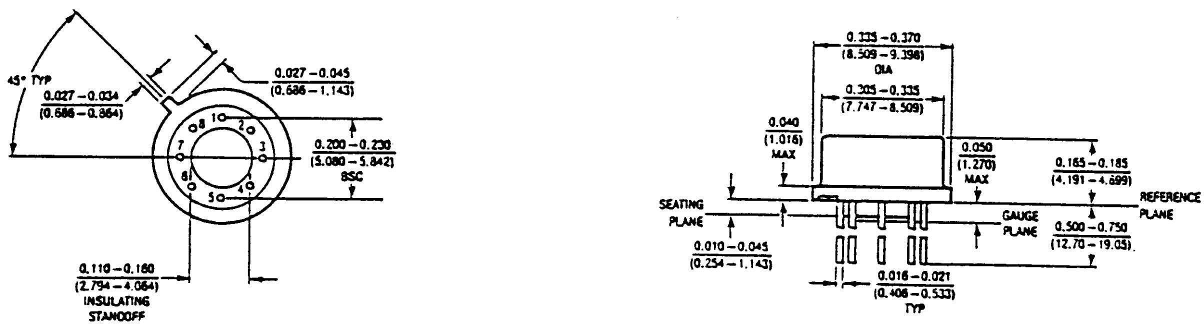
$T_j$max	θ_{ja}
165°C	100°C/W

N Package
8-Lead Plastic DIP



$T_j$max	θ_{ja}
115°C	130°C/W

H Package
8-Lead TO-5 Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

$T_j$max	θ_{ja}	θ_{jc}
175°C	140°C/W	40°C/W