

Transimpedance amplifier

5212A

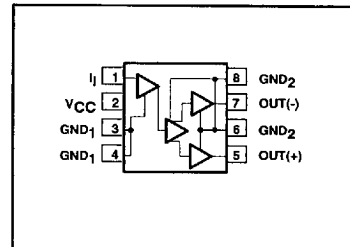
FEATURES

- Extremely Low Noise
- Single 5V Supply
- Large Bandwidth Differential Outputs
- Low Input/Output Impedances
- High Power Supply Rejection Ratio
- 14K Ω Differential Transresistance

APPLICATIONS

- Fiber-Optic Receivers
- Wideband Gain Block
- General Purpose
- Instrumentation
- Sensor Preamplifiers
- Single-Ended to Differential Conversion
- Low Noise RF Amplifiers

PIN CONFIGURATION



DESCRIPTION

The 5212A is a wide band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber-optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
8-Pin Ceramic DIP	5212A/BPA	GDIP1-T8

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_{amb}	Operating ambient temperature range	-55 to + 125	$^{\circ}\text{C}$
T_S	Operating junction temperature range	-55 to +150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-65 to + 150	$^{\circ}\text{C}$
V_{CC}	Power supply	6	V_{DC}
G-G	Ground differential	None allowed, short 4 ground pins together	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
T_{amb}	Ambient temperature	-55 to + 125	$^{\circ}\text{C}$
T_S	Junction temperature	-55 to +150	$^{\circ}\text{C}$
V_{CC}	Supply voltage	4.5 to 5.5	V_{DC}

DC ELECTRICAL CHARACTERISTICS

Min. and Max. limits apply over operating temperature range at $V_{CC} = 5V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_I	Input bias voltage	$I_{IN} = 0$	0.55	0.8	1.05	V
V_O	Output bias voltage	$I_{IN} = I_{OUT} = 0$	2.5	3.3	3.8	V
V_{OS}	Output offset voltages	$I_{IN} = I_{OUT} = 0$		0	120	mV
I_{CC}	Supply current	$I_{IN} = I_{OUT} = 0$	20	26	33	mA
I_{OMAX}	Output sink/source current	$\Delta V_{OUT} = \leq 100\text{mV}$	3	4		mA
I_B	Maximum input current (2% linearity)	$I_O = 0$	± 40	± 80		μA
I_{MAX}	Maximum input current overload threshold		± 60	± 120		μA

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AC ELECTRICAL CHARACTERISTICS¹Min. and Max. limits apply over operating temperature range at $V_{CC} = 5V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
R_T	Transresistance (Differential output)	Test Circuit 1 $F = 10MHz$, $R_L = inf.$ Note 5	9.0	14	19	$k\Omega$
R_O	Output resistance (Differential output)	Test Circuit 1 $F = 10MHz$ Note 4	14	30	46	Ω
R_T	Transresistance (Single-ended output)	Test Circuit 1 $F = 10MHz$, $R_L = inf.$ Note 4	4.5	7	9.5	$k\Omega$
R_O	Output resistance (Single-ended output)	Test circuit 1 $F = 10MHz$ Note 5	7	15	23	Ω
f_{3db}	Bandwidth (-3dB)	$T_{amb} = 25^\circ C$ Note 4	100	120		MHz
R_{IN}	Input resistance	Note 4	70	110	150	Ω
C_{IN}	Input capacitance	Note 4		10	18	pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	$\Delta V_{CC} = 5 \pm 0.5V$ Note 4		9.6		
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity			0.05		$\%/^\circ C$
I_N	Input RMS noise current spectral density	Test Circuit 2 $F = 10MHz$		2.5		pA/\sqrt{Hz}
I_T	Input RMS noise current	Test Circuit 2 $\Delta F = 100MHz$		30		nA
PSRR	Power supply rejection ratio	Test Circuit 3 $F = 0.1MHz$ Note 2, 3, 5	20	33		dB
PSRR	Power supply rejection ratio (ECL configuration)	Test Circuit 4 $F = 0.1MHz$ Note 2, 3		23		dB
V_{OMAX}	Max. output voltage swing differential	$R_L = \infty$	1.7	3.2		V_{p-p}
I_{PMAX}	Pulse distortion overload threshold			± 300		μA

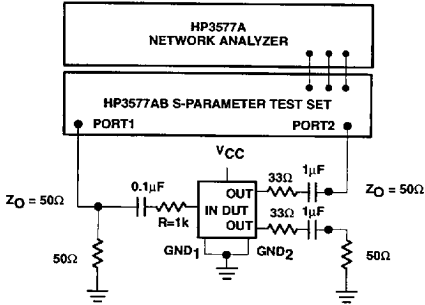
NOTES:

1. Typical data applies at $V_{CC} = 5V$ and $T_{amb} = 25^\circ C$.
2. Circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} lines.
3. Output referenced.
4. This parameter is guaranteed but not tested.
5. Due to test equipment limitations, actual tested conditions and/or limits may differ from those specified, however the specified test limits and conditions are guaranteed.

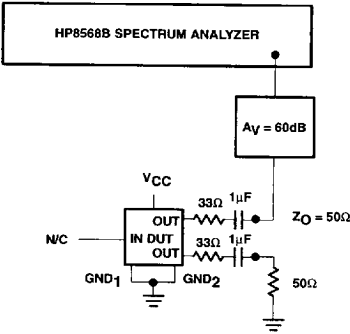
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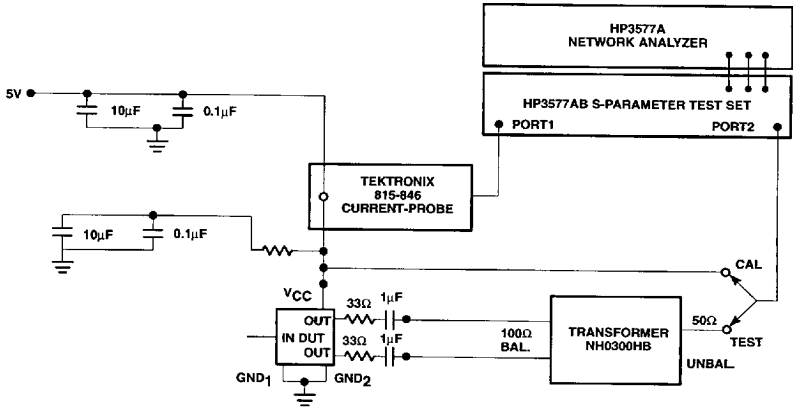
SINGLE-ENDED	DIFFERENTIAL
$R_t = \frac{V_{OUT}}{V_{IN}} \quad R = (2)(S_{21})(R)$	$R_t = \frac{V_{OUT}}{V_{IN}} \quad R = (4)(S_{21})(R)$
$R_O = Z_O \left[\frac{1 + S_{22}}{1 - S_{22}} \right] - 33$	$R_O = 2Z_O \left[\frac{1 + S_{22}}{1 - S_{22}} \right] - 66$



Test Circuit 1



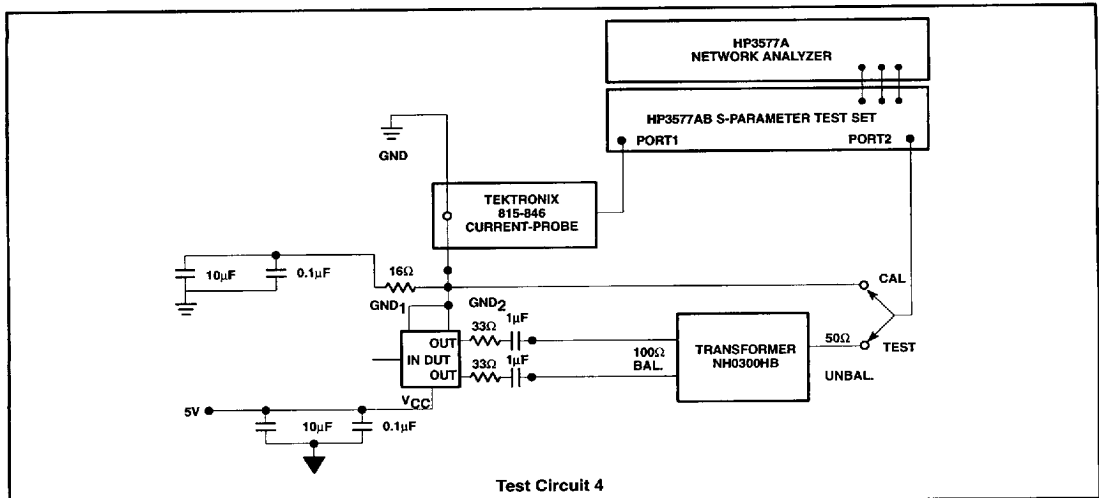
Test Circuit 2



Test Circuit 3

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DEFINITION OF TERMS

Symbol	Name and Function												
V_I	INPUT BIAS VOLTAGE: The Input Bias Level test measures the quiescent voltage on the input pin of the DUT, referenced to ground.												
V_O	OUTPUT BIAS VOLTAGE: The Output Bias Level tests measure the quiescent voltage level of the OUT(-) and OUT(+) pins referenced to ground.												
V_{OS}	OUTPUT OFFSET VOLTAGE: The V_{OS} test measures output offset voltage due to the mismatch of the output bias levels. A high impedance meter is connected across the two output pins and V_{OS} is measured directly.												
Output Sink/Source Current													
$I_{O\ MAX}$	ISOURCE: The ISOURCE test measures the DUT's output capability of forcing current to a load. A 3mA load is applied to the DUT. The change in the output bias level, from no load to loaded, is measured. The input has no signal applied during this test.												
$I_{O\ MAX}$	ISINK: The ISINK test measures the DUT's output capability of sinking current from a load. A 3mA load is applied to the DUT. The change in the output bias level, from no load to loaded, is measured. The input has no signal applied during this test.												
I_B	<p>MAXIMUM INPUT CURRENT (2% Linearity): The LINEARITY test measures the nonlinearity, of the transfer curve, of the DUT. Four points on the transfer curve of the DUT are measured. Specific DC currents forced at the input and the resulting output voltage is measured. The percent of nonlinearity is calculated as follows:</p> $+Linearity(\%) = \{1 - ABS(R/T+)\} \times 100$ $-Linearity(\%) = \{1 - ABS(R/T-)\} \times 100$ <p>Where</p> $R = (V4 - V6) / (I4 - I6)$ $T+ = (V3 - V5) / (I3 - I5)$ $T- = (V5 - V7) / (I5 - I7)$ <p>The forcing DC currents if $I_S = \pm 40\mu A$:</p> <table border="0"> <tbody> <tr> <td>$I1 = 130\mu A$</td><td>$I7 = -30\mu A$</td></tr> <tr> <td>$I2 = 100\mu A$</td><td>$I8 = -40\mu A$</td></tr> <tr> <td>$I3 = 60\mu A$</td><td>$I9 = -60\mu A$</td></tr> <tr> <td>$I4 = 40\mu A$</td><td>$I10 = -100\mu A$</td></tr> <tr> <td>$I5 = 30\mu A$</td><td>$I11 = 130\mu A$</td></tr> <tr> <td>$I6 = 0\mu A$</td><td></td></tr> </tbody> </table>	$I1 = 130\mu A$	$I7 = -30\mu A$	$I2 = 100\mu A$	$I8 = -40\mu A$	$I3 = 60\mu A$	$I9 = -60\mu A$	$I4 = 40\mu A$	$I10 = -100\mu A$	$I5 = 30\mu A$	$I11 = 130\mu A$	$I6 = 0\mu A$	
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$I6 = 0\mu A$													

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DEFINITION OF TERMS (Continued)

Symbol	Name and Function
I_{MAX}	<p>INPUT OVERLOAD CURRENT THRESHOLD: The input overload tests are used to guarantee that the knees of DUT's transfer curve are within spec. The ATE's meter is connected to the output pin being tested and ground; in the same manner as the OUTPUT BIAS test. The input is forced with a DC current. The output swing is then measured. This is done twice, once with 130μA and then with 80μA. The two readings are stored, and the results are calculated from the following:</p> $INPUT\ OVERLOAD = V_{OUT}(120\mu A) - V_{OUT}(50\mu A)$ <p>If the difference is greater than 50mV, the 50μA test point must be in the linear region.</p>
R_T	<p>TRANSRESISTANCE AT 10MHz: The Transresistance test measures the single-ended, midband gain of the DUT at 10MHz. The network analyzer is set to measure S21 for the DUT. The actual value displayed is calculated as follows:</p> $TRANSRESISTANCE = 2 \times S21 \times 1K\Omega$ <p>INPUT SERIES RESISTANCE, $R = 1K\Omega$</p>
R_o	<p>DIFFERENTIAL GAIN AT 10MHz (DIFFERENTIAL TRANSRESISTANCE): This test calculates the total gain of the DUT at 10MHz. The value displayed is the sum of the single-ended tests.</p>
R_o	<p>ROUT: the DC output resistance (ROUT) is calculated from the measurement in the ISOURCE test. The calculation is as follows:</p> $ROUT = 3mA / ISOURCE\ measurement$ <p>The AC output resistance as specified is similar to measurement made with a Network Analyzer.</p>
f_{3db}	<p>3dB BANDWIDTH: This test measures the -3dB bandwidth of the DUT relative to the midband gain.</p>
P_{SRR}	<p>PSRR: The PSRR test measures the effect that a changing V_{CC} has to V_{OS} test. The V_{CC}^7 is changed with a small delta (+/- 0.1 V). The change in V_{OS} is then measured. The two readings are stored and the PSRR results are calculated from the following:</p> $PSRR = 20 \times ABS(LOG(R))$ <p>WHERE</p> $R = \frac{V_{OS}(V_{CC} = 5.1V) - V_{OS}(V_{CC} = 4.9V)}{(0.20volts)}$
$V_{OUT\ MAX}$	<p>VOUT MAX: The VOUT MAX test measures the DUT's maximum output swing. The ATE's meter is connected across the output of the DUT in the same manner as the V_{OS} test. The input is forced with a DC current. The output swing is then measured. This is done twice, once with +130μA and then with -130μA. The two readings are stored. The VOUT MAX is calculated from the following:</p> $V_{OUT\ MAX} = V_{OUT}(+130\mu A) - V_{OUT}(-130\mu A)$
$I_{P\ MAX}$	<p>IPMAX: An Bipolar Square wave of frequency = 1MHz is applied to the input, via a 1KΩ Resistor. The I_p is the \pm current where the output duty cycle deviates by 10% from that of the input duty cycle.</p>