

AC573 • ACT573

NATIONAL SEMICONDUCTOR LOGIC D E D 6501122 0062602 6

54AC/74AC573 • 54ACT/74ACT573

Octal D-Type Latch With 3-State Outputs

T-46-07-11

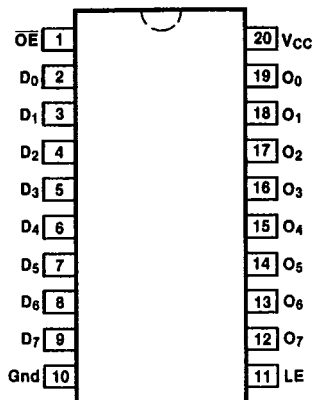
Description

The 'AC/'ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The 'AC/'ACT573 is functionally identical to the 'AC/'ACT373 but has Inputs and outputs on opposite sides.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to 'AC/'ACT373
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- 'ACT573 has TTL-Compatible Inputs

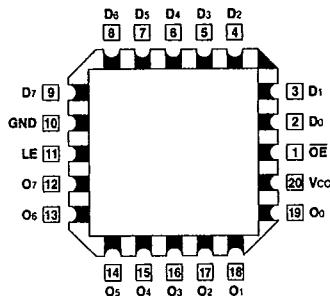
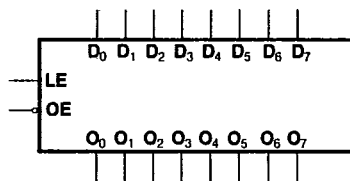
Connection Diagrams



Pin Assignment
for DIP, Flatpak and SOIC

Ordering Code: See Section 6

Logic Symbol



Pin Assignment
for LCC

Pin Names

- D0 - D7 Data Inputs
LE Latch Enable Input
 $\overline{OE}$ 3-State Output Enable Input
O0 - O7 3-State Latch Outputs

T-4607-11

Functional Description

The 'AC/ACT573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage

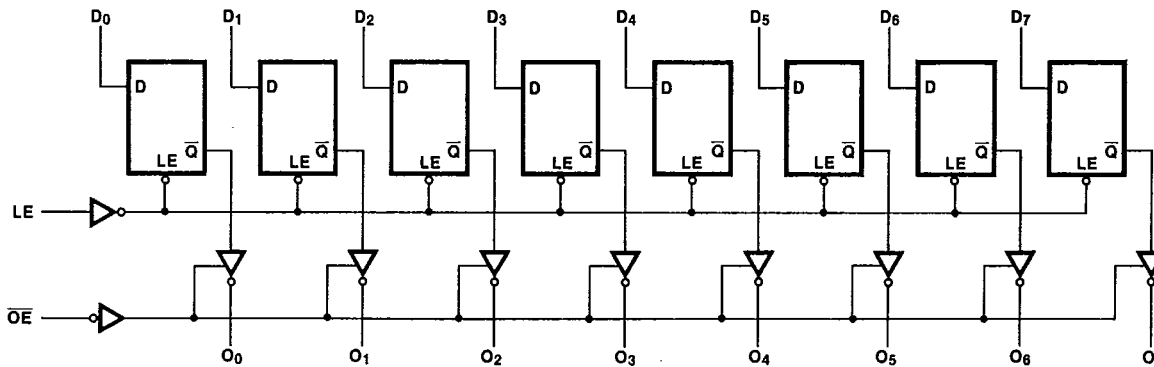
L = LOW Voltage

Z = High Impedance

X = Immaterial

 O_0 = Previous O_0 before LOW-to-HIGH Transition of Clock**Logic Diagram**

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC Characteristics (unless otherwise specified)

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Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input (ACT573)	1.6	1.5	mA	V _{IN} = V _{CC} - 2.1 V V _{CC} = 5.5 V, T _A = Worst Case

AC Characteristics

AC Characteristics											
Symbol	Parameter	V _{cc} * (V)	74AC			54AC		74AC		Units	Fig. No.
			T _A = + 25°C CL = 50 pF			T _A = - 55°C to + 125°C CL = 50 pF		T _A = - 40°C to + 85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0		9.0 6.0						ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0		9.0 6.0						ns	3-5
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0		9.0 6.0						ns	3-6
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0		8.0 5.5						ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0		7.0 5.5						ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0		7.5 5.5						ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0		8.5 6.5						ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0		6.5 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74AC	54AC	74AC	Units	Fig. No.
			TA = +25°C CL = 50 pF	TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum			
ts	Setup Time, HIGH or LOW Dn to LE	3.3 5.0	2.0 1.0			ns	3-9
th	Hold Time, HIGH or LOW Dn to LE	3.3 5.0	0 0			ns	3-9
tw	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

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Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = + 25°C CL = 50 pF			TA = – 55°C to + 125°C CL = 50 pF		TA = – 40°C to + 85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
tPLH	Propagation Delay Dn to On	5.0	1.0	6.0	10.5	1.0	13.5	1.0	12.0	ns	3-5
tPHL	Propagation Delay Dn to On	5.0	1.0	6.0	10.5	1.0	13.5	1.0	12.0	ns	3-5
tPLH	Propagation Delay LE to On	5.0	1.0	6.0	10.5	1.0	13.0	1.0	12.0	ns	3-6
tPHL	Propagation Delay LE to On	5.0	1.0	5.5	9.5	1.0	12.0	1.0	10.5	ns	3-6
tpZH	Output Enable Time	5.0	1.0	5.5	10.0	1.0	11.5	1.0	11.0	ns	3-7
tpZL	Output Enable Time	5.0	1.0	5.5	9.5	1.0	11.0	1.0	10.5	ns	3-8
tPHZ	Output Disable Time	5.0	1.0	6.5	11.0	1.0	13.5	1.0	12.5	ns	3-7
tPLZ	Output Disable Time	5.0	1.0	5.0	8.5	1.0	10.5	1.0	9.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Dn to LE	5.0	1.5	3.0	3.5	3.5	ns	3-9
th	Hold Time, HIGH or LOW Dn to LE	5.0	-1.5	0	0.5	0	ns	3-9
tw	LE Pulse Width, HIGH	5.0	2.0	3.5	5.0	4.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	5.0	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance	25.0	pF	Vcc = 5.5 V