



54ACT/74ACT1016 16 x 16 Parallel Multiplier

General Description

The 'ACT1016 is a high-speed, low power 16 x 16-bit parallel multiplier that is ideally suited for real-time digital signal processing applications. Fabricated using advanced FACTTM technology, the 'ACT1016 offers a very low power alternative and exceptional performance.

The 'ACT1016 is a pin and functional replacement for TRW's MPY016H; the 'ACT1016 operates from a single V_{CC} supply and is compatible with standard TTL logic levels.

The architecture of the 'ACT1016 features one 16-bit port dedicated to the X input registers (controlled by CLKX), one 16-bit I/O port used for loading the Y input registers (controlled by CLKY) and for displaying the Least Significant Product (LSP), and one 16-bit output port multiplexed between displaying the Least Significant Product (LSP) and the Most Significant Product (MSP). The I/O port direction is controlled by $\overline{OEL}$ and the output port TRI-STATE[®] control is controlled by $\overline{OEP}$. The result is registered if FT is LOW (controlled by CLKL for the LSP and CLKM for the MSP) and unregistered if FT is held HIGH.

Twos complement, unsigned magnitude and mixed mode multiplications are possible through the two's complement X

and Y mode controls, X_M and Y_M , respectively. These mode controls are registered, controlled by the input clocks CLKX and CLKY.

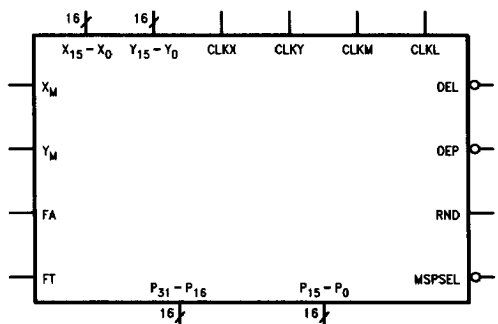
Result rounding is controlled by the registered RND signal (controlled by both CLKX and CLKY). Selection of one of the two rounding modes is determined by the FA signal.

Features

- 16 x 16 parallel multiplier
- Selectable rounding modes
- Twos complement, unsigned magnitude and mixed mode multiplication
- Pin and functionally compatible with TRW MPY016H
- Provides low voltage, high-speed operation
- Single V_{CC} supply
- $\pm 2000V$ ESD protection
- Outputs source/sink 8 mA
- TRI-STATE outputs
- 'ACT1016 has TTL-compatible inputs

Ordering Code: See Section 5

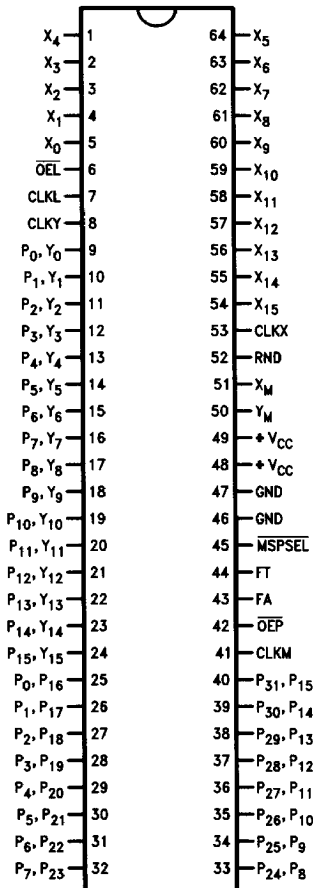
Logic Symbol



Pin Names	Description
$X_{15}-X_0$	Multiplicand Data Inputs
$Y_{15}-Y_0$	Multiplier Data Inputs
CLKX, CLKY	Input Clocks
CLKM	Input Clock, MSP
CLKL	Input Clock, LSP
X_M, Y_M	Mode Control Inputs
FA	Format Adjust Control
FT	Format Transparent Control
$\overline{OEL}$	TRI-STATE Enable, LSP Routing
$\overline{OEP}$	TRI-STATE Enable, Product
RND	Output Port
$\overline{MSPSEL}$	Round Control, MSP
$P_{31}-P_{16}$	MSP Select
$P_{15}-P_0$	MSP Outputs
	LSP Outputs

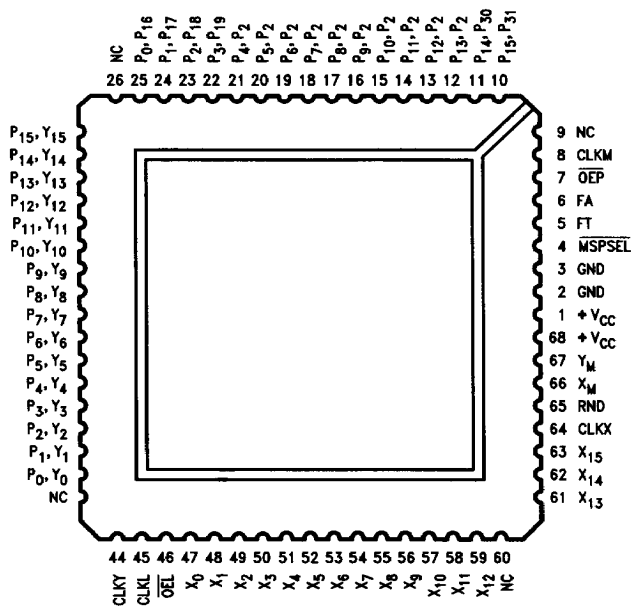
Connection Diagrams

Pin Assignment for DIP



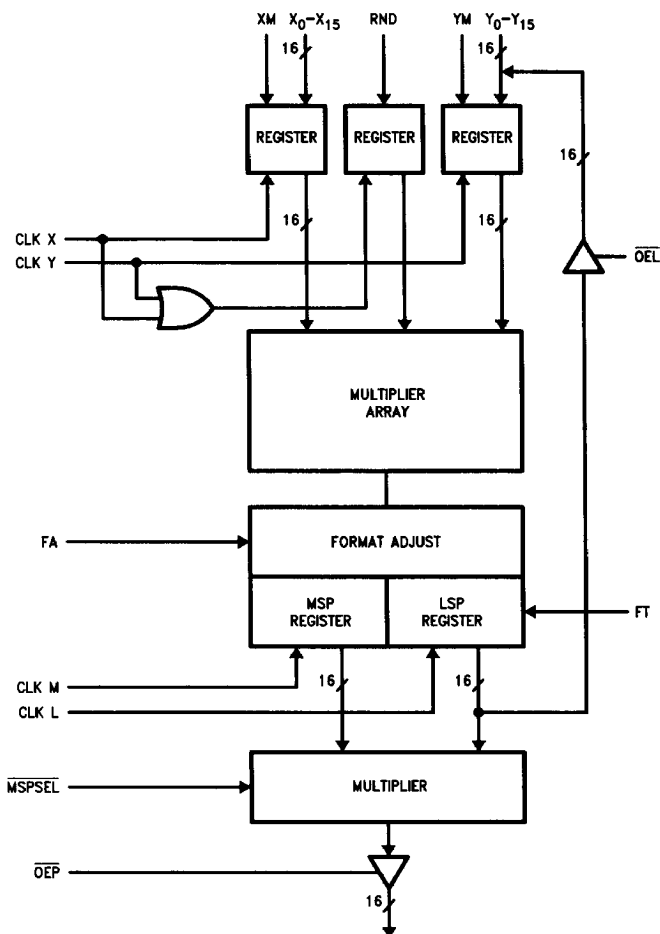
TL/F/10143-1

Pin Assignment for PCC



TL/F/10143-2

Logic Diagram



TL/F/10143-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

BINARY POINT

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X																Signal											
	Y ₁₅	Y ₁₄	Y ₁₃	Y ₁₂	Y ₁₁	Y ₁₀	Y ₉	Y ₈	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀	Digit Value										
	-20	2	-1	2	-2	-3	2	-4	-2	-5	2	-6	-2	-7	2	-8	-2	-10	2	-11	2	-12	-13	2	-14	2	-15

P ₃₁	P ₃₀	P ₂₉	P ₂₈	P ₂₇	P ₂₆	P ₂₅	P ₂₄	P ₂₃	P ₂₂	P ₂₁	P ₂₀	P ₁₉	P ₁₈	P ₁₇	P ₁₆	P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀	Signal														
-20	2	1	2	3	2	4	5	2	6	7	2	8	9	2	10	11	2	12	13	2	14	15	2	16	17	2	18	19	2	20	21	2	22	23	2	24	25	2	26	27	2	28	29	2	30	Digit Value

MSP										LSP										Signal																
P ₃₁	P ₃₀	P ₂₉	P ₂₈	P ₂₇	P ₂₆	P ₂₅	P ₂₄	P ₂₃	P ₂₂	P ₂₁	P ₂₀	P ₁₉	P ₁₈	P ₁₇	P ₁₆	P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀					
-31	-20	2	-12	-22	-32	-42	-52	-62	-72	-82	-92	-102	-112	-122	-132	-142	-152	-162	-172	-182	-192	-202	-212	-222	-232	-242	-252	-262	-272	-282	-292	-30				
Digit Value																																				
FA = 1																																				

FIGURE 1. Fractional Twos Complement Notation

BINARY POINT

X ₁₅	X ₁₄	X ₁₃	X ₁₂	X ₁₁	X ₁₀	X ₉	X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Signal												
2	-1	2	-2	-3	2	-4	-2	-5	2	-6	-2	-7	2	-8	-2	-10	2	-11	2	-12	-13	2	-14	2	-15	2	-16	Digit Value

Y ₁₅	Y ₁₄	Y ₁₃	Y ₁₂	Y ₁₁	Y ₁₀	Y ₉	Y ₈	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀	Signal												
2	-1	2	-2	-3	2	-4	-2	-5	2	-6	-2	-7	2	-8	-2	-10	2	-11	2	-12	-13	2	-14	2	-15	2	-16	Digit Value

P ₃₁	P ₃₀	P ₂₉	P ₂₈	P ₂₇	P ₂₆	P ₂₅	P ₂₄	P ₂₃	P ₂₂	P ₂₁	P ₂₀	P ₁₉	P ₁₈	P ₁₇	P ₁₆	P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀	Signal
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	Digit Value

FIGURE 2. Fractional Unsigned Magnitude Notation

*In this format an overflow occurs in the attempted multiplication of the two complement number 1000 ... 0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -230 in the integer case.

BINARY POINT

X ₁₅	X ₁₄	X ₁₃	X ₁₂	X ₁₁	X ₁₀	X ₉	X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Signal (Two's Complement) Digit Value
-2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	

Y ₁₅	Y ₁₄	Y ₁₃	Y ₁₂	Y ₁₁	Y ₁₀	Y ₉	Y ₈	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀	Signal (Unsigned Magnitude) Digit Value
2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶	

P ₃₁	P ₃₀	P ₂₉	P ₂₈	P ₂₇	P ₂₆	P ₂₅	P ₂₄	P ₂₃	P ₂₂	P ₂₁	P ₂₀	P ₁₉	P ₁₈	P ₁₇	P ₁₆	P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀	Signal
-2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶	2 ⁻¹⁷	2 ⁻¹⁸	2 ⁻¹⁹	2 ⁻²⁰	2 ⁻²¹	2 ⁻²²	2 ⁻²³	2 ⁻²⁴	2 ⁻²⁵	2 ⁻²⁶	2 ⁻²⁷	2 ⁻²⁸	2 ⁻²⁹	2 ⁻³⁰	2 ⁻³¹	

FA = 1

Mandatory

FIGURE 3. Fractional Mixed Mode Notation

BINARY POINT

X ₁₅	X ₁₄	X ₁₃	X ₁₂	X ₁₁	X ₁₀	X ₉	X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Signal
-2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	

Digit Value

Y ₁₅	Y ₁₄	Y ₁₃	Y ₁₂	Y ₁₁	Y ₁₀	Y ₉	Y ₈	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀	Signal
-2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	

Digit Value

P ₃₁	P ₃₀	P ₂₉	P ₂₈	P ₂₇	P ₂₆	P ₂₅	P ₂₄	P ₂₃	P ₂₂	P ₂₁	P ₂₀	P ₁₉	P ₁₈	P ₁₇	P ₁₆	P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀	Signal
-2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶	2 ¹⁵	-2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶	2 ¹⁵	

FA = 0

LSP

MSP

P ₃₁	P ₃₀	P ₂₉	P ₂₈	P ₂₇	P ₂₆	P ₂₅	P ₂₄	P ₂₃	P ₂₂	P ₂₁	P ₂₀	P ₁₉	P ₁₈	P ₁₇	P ₁₆	P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀	Signal
-2 ³¹	2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	

FA = 1

LSP

MSP

FIGURE 4. Integer Two's Complement Notation

BINARY POINT

X ₁₅	X ₁₄	X ₁₃	X ₁₂	X ₁₁	X ₁₀	X ₉	X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Signal
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	Digit Value

Y ₁₅	Y ₁₄	Y ₁₃	Y ₁₂	Y ₁₁	Y ₁₀	Y ₉	Y ₈	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀	Signal
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	Digit Value

P ₃₁	P ₃₀	P ₂₉	P ₂₈	P ₂₇	P ₂₆	P ₂₅	P ₂₄	P ₂₃	P ₂₂	P ₂₁	P ₂₀	P ₁₉	P ₁₈	P ₁₇	P ₁₆	P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀	Signal
2 ³¹	2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	Digit Value
MSP																LSP												Mandatory				FA = 1

FIGURE 5. Integer Unsigned Magnitude Notation

BINARY POINT

X ₁₅	X ₁₄	X ₁₃	X ₁₂	X ₁₁	X ₁₀	X ₉	X ₈	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Signal (Two's Complement) Digit Value
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	

Y ₁₅	Y ₁₄	Y ₁₃	Y ₁₂	Y ₁₁	Y ₁₀	Y ₉	Y ₈	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀	Signal (Unsigned Magnitude) Digit Value
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	

P ₃₁	P ₃₀	P ₂₉	P ₂₈	P ₂₇	P ₂₆	P ₂₅	P ₂₄	P ₂₃	P ₂₂	P ₂₁	P ₂₀	P ₁₉	P ₁₈	P ₁₇	P ₁₆	P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀	Signal
2 ³¹	2 ³⁰	2 ²⁹	2 ²⁸	2 ²⁷	2 ²⁶	2 ²⁵	2 ²⁴	2 ²³	2 ²²	2 ²¹	2 ²⁰	2 ¹⁹	2 ¹⁸	2 ¹⁷	2 ¹⁶	2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	Digit Value
MSP																LSP												Mandatory				FA = 1

FIGURE 6. Integer Mixed Mode Notation

*In this format an overflow occurs in the attempted multiplication of the two's complement number 1000 ... 0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2³⁰ in the integer case.

Signal Descriptions

Inputs

X_{IN} ($X_{15}-X_0$)

Sixteen multiplicand data inputs.

Y_{IN} ($Y_{15}-Y_0$)

Sixteen multiplier data inputs. This is also an output port for $P_{15}-P_0$.

Input Clocks

CLKX

The rising edge of this clock loads the $X_{15}-X_0$ data input register along with the X mode and round registers.

CLKY

The rising edge of this clock loads the $Y_{15}-Y_0$ data input register along with the Y mode and round registers.

CLKM

The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL

The rising edge of this clock loads the Least Significant Product (LSP) register.

Controls

X_M , Y_M

Mode control inputs for each data word. A LOW input designates an unsigned data input, and a HIGH input designates twos complement.

FA

When the Format Adjust (FA) Control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional twos complement applications (see multiplier input/output formats).

FT

When the Format Transparent (FT) Control is HIGH, both the MSP and LSP registers are transparent.

$\overline{OEL}$

The $\overline{OEL}$ input is the TRI-STATE enable for routing LSP through Y_{IN}/LSP_{OUT} port.

$\overline{OEP}$

The $\overline{OEP}$ is the TRI-STATE enable for the product output port.

RND

The Round control is used for the rounding of the MSP. When this control is HIGH, A '1' is added to the Most Significant Bit (MSB) of the LSP. Note that this bit depends on the state of the format adjust (FA) control.

If FA is LOW when RND is HIGH, a '1' will be added to the 2⁻¹⁶ bit (P_{14}). If FA is HIGH when RND is HIGH, a '1' will be added to the 2⁻¹⁵ bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH.

Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

$\overline{MPSEL}$

When $\overline{MPSEL}$ is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

Outputs

MSP ($P_{31}-P_{16}$)

The MSP is the Most Significant Product output.

LSP ($P_{15}-P_0$)

The LSP is the Least Significant Product output.

Y_{15-0}/LSP_{OUT} ($Y_{15}-Y_0$ or $P_{15}-P_0$)

This is the Least Significant Product (LSP) output available when $\overline{OEL}$ is LOW. It is also an input port for $Y_{15}-Y_0$.

Absolute Maximum Ratings*

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = 0.5$	-20 mA
$V_I = V_{CC} + 0.5$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current; per Output Pin	
$V_O = 0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC V_{CC} or Ground Current per Output Pin (I_{CC}) or (I_{GND})	± 20 mA
Storage Temperature (T_{STG})	-65°C to +150°C

*Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Supply Voltage (V_{CC}) (Unless Otherwise Specified)	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT	-40°C to +85°C
54ACT	-55°C to +125°C
Maximum Slew Rate (S_r) (except for Schmitt Inputs)	
V_{IN}	0.8V to 2.0V
V_{meas}	0.8V to 2.0V
V_{CC} @ 4.5V	10 ns
V_{CC} @ 5.5V	8 ns

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74ACT		74ACT	Units	Conditions
		Typ	Guaranteed Limit			
I _{IN}	Maximum Input Leakage Current		± 0.1	± 1.0	μA	V _{CC} = Max, V _{IN} = V _{CC} , GND
I _{OZ}	Maximum TRI-STATE Current		± 0.5	± 5.0	μA	High Z, V _{CC} = Max, V _{OUT} = V _{CC} , GND
I _{CCQ}	Supply Current, Quiescent	0.5	2.0	10.0	mA	V _{CC} = Max, V _{IN} = 0 V TSL, TSM, TSX = Max
I _{CCD}	Supply Current, 12.4 MHz Loaded	300		325	mA	V _{CC} = Max, f = 12.4 MHz Test Load: See Note 1
I _{CCD}	Supply Current, 20 MHz Loaded	325		350	mA	V _{CC} = Max, f = 20 MHz Test Load: See Note 1
V _{OH} *	Minimum HIGH Level Output	4.49	4.4	4.4	V	V _{IN} = V _{IL} or V _{IH} , I _{OUT} = − 50 μA, V _{CC} = 4.5V
		5.49	5.4	5.4		V _{IN} = V _{IL} or V _{IH} , I _{OUT} = − 50 μA, V _{CC} = 5.5V
			3.86	3.76	V	I _{OH} = − 8 mA, V _{CC} = 4.5V
			4.86	4.76	B	I _{OH} = − 8 mA, V _{CC} = 5.5V
V _{OL} *	Maximum HIGH Level Output	0.001	0.1	0.1	V	V _{IN} = V _{IL} or V _{IH} , I _{OUT} = 50 μA, V _{CC} = 4.5V
		0.001	0.1	0.1	V	V _{IN} = V _{IL} or V _{IH} , I _{OUT} = 50 μA, V _{CC} = 5.5V
			0.45	0.50	V	I _{OL} = 8 mA, V _{CC} = 4.5V
			0.45	0.50	B	I _{OL} = 8 mA, V _{CC} = 5.5V
I _{OLD}	Minimum Dynamic Output Current			32	mA	V _{CC} = 5.5V, V _{OLD} = 2.2V Max (Note 2)
I _{OHD}	Minimum Dynamic Output Current			−32	mA	V _{CC} = 5.5V, V _{OHD} = 3.3V Min (Note 2)
I _{CCT}	Maximum I _{CC} /Input	0.6		1.5	mA	V _{IN} = V _{CC} − 2.1V

Note 1: Test Load 50 pF, 500Ω to Ground.

Note 2: Only one output loaded at one time, maximum duration of test 2 ms.

*All outputs loaded.

AC Characteristics

Symbol	Parameter	74ACT				Units	Fig. No.
		T _A = −40°C to +85°C					
		1016-65		1016-55			
		Min	Max	Min	Max		
t _{MUC}	Unclocked Multiply Time		80.0		65.0	ns	2-3, -9
t _{MC}	Clocked Multiply Time		65.0		55.0	ns	2-3, -9, -10
t _{PDSEL}	MSPSEL to Product Out	1.5	13.0	1.5	13.0	ns	2-3, -9
t _{PDP}	Output Clock to P	1.5	20.0	1.5	20.0	ns	2-3, -9
t _{PDY}	Output Clock to Y	1.5	20.0	1.5	20.0	ns	2-3, -9
t _{ENA}	TRI-STATE Enable Time (Note 2)	1.5	10.0	1.5	10.0	ns	2-3, -8
t _{DIS}	TRI-STATE Disable Time (Note 2)	1.5	12.5	1.5	12.5	ns	2-3, -8
t _{HCL}	Clock LOW Hold Time CLKXY Relative to CLKML (Note 1)	0		0		ns	2-3, -9, -10
t _s	Setup Time X, Y, RND	5.5		5.5		ns	2-3, -7, -9
t _h	Hold Time X, Y, RND	1.0		1.0		ns	2-3, -7, -9
t _w	Clock Pulse Width HIGH or LOW	3.5		3.5		ns	2-3, -9

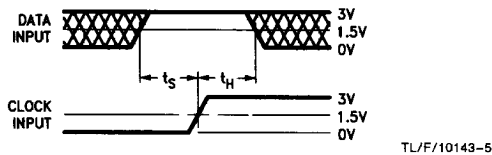
Note 1: To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

Note 2: Transition is measured to ± 500 mV from steady state voltage with loading specified in Figure 2-3.

Capacitance

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	5.0	pF	$V_{OUT} = 0V$

Timing Diagrams



Note: Diagram shown for HIGH data only. Output transition may be opposite sense.

FIGURE 7. Setup and Hold Time

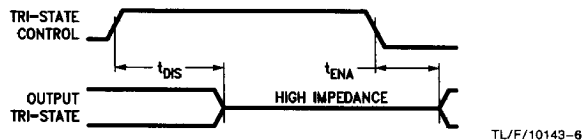


FIGURE 8. TRI-STATE Control Timing Diagram

Timing Diagrams (Continued)

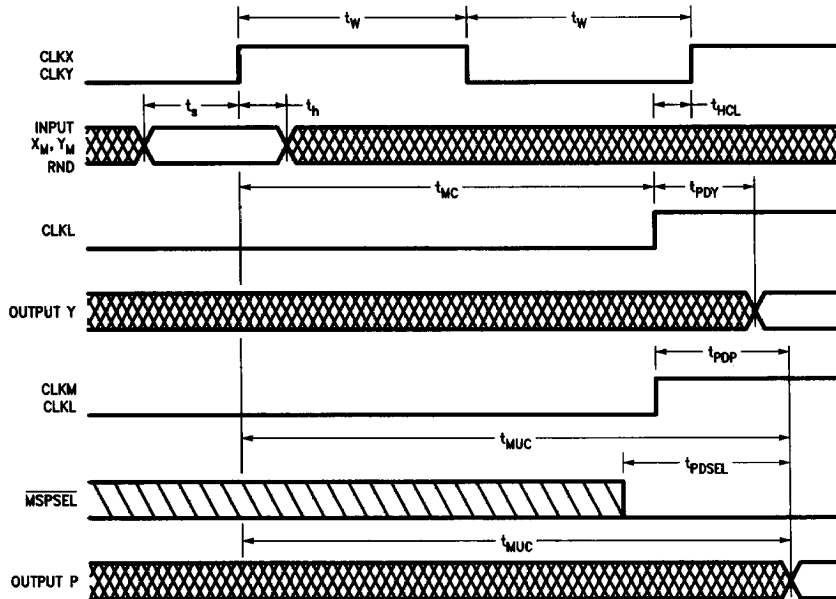


FIGURE 9. '1016 Timing Diagram

TL/F/10143-7

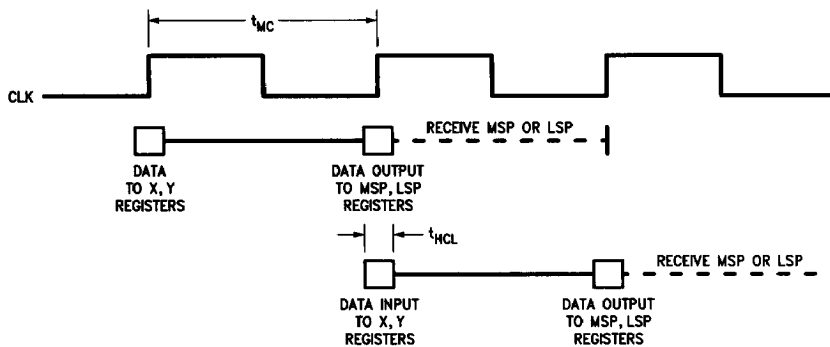


FIGURE 10. Simplified Timing Diagram—Typical Application

TL/F/10143-8