

T-52-31

54AC16953, 54ACT16953 74AC16953, 74ACT16953 16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TIO239—D3581, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16953 and 'ACT16953 are inverting 16-bit registered bus transceivers composed of two 8-bit transceiver sections with separate control signals.

Data flow in the A-to-B mode is controlled by output-enable ($\overline{1OEAB}$ and $\overline{2OEAB}$), clock-enable ($\overline{1CEAB}$ and $\overline{2CEAB}$), and clock ($\overline{1CLKAB}$ and $\overline{2CLKAB}$) inputs. When $\overline{1CEAB}$ (or $\overline{2CEAB}$) is high, data storage is inhibited and the registers retain their previous states. When $\overline{1CEAB}$ (or $\overline{2CEAB}$) is low, the inverse of the data present at the corresponding A inputs is stored in the device on a low-to-high transition of $\overline{1CLKAB}$ (or $\overline{2CLKAB}$). If $\overline{1OEAB}$ (or $\overline{2OEAB}$) is also low, this stored data appears on the corresponding B outputs; if $\overline{1OEAB}$ (or $\overline{2OEAB}$) is high, the corresponding B outputs are in the high-impedance state. $\overline{1OEAB}$ (or $\overline{2OEAB}$) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is controlled by $\overline{1OEBA}$ and $\overline{2OEBA}$, $\overline{1CEBA}$ and $\overline{2CEBA}$, and $\overline{1CLKBA}$ and $\overline{2CLKBA}$ in a manner analogous to that described above for A-to-B data flow.

54AC16953, 54ACT16953 ... WD PACKAGE
 74AC16953, 74ACT16953 ... DL PACKAGE
 (TOP VIEW)

$\overline{1OEAB}$	1	58	$\overline{1OEBA}$
$\overline{1CLKAB}$	2	55	$\overline{1CLKBA}$
$\overline{1CEAB}$	3	54	$\overline{1CEBA}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V _{CC}	7	50	V _{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V _{CC}	22	35	V _{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{2CEAB}$	26	31	$\overline{2CEBA}$
$\overline{2CLKAB}$	27	30	$\overline{2CLKBA}$
$\overline{2OEAB}$	28	29	$\overline{2OEBA}$

PRODUCT PREVIEW

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INSTRUMENTS

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16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3561, JUNE 1990—T10239

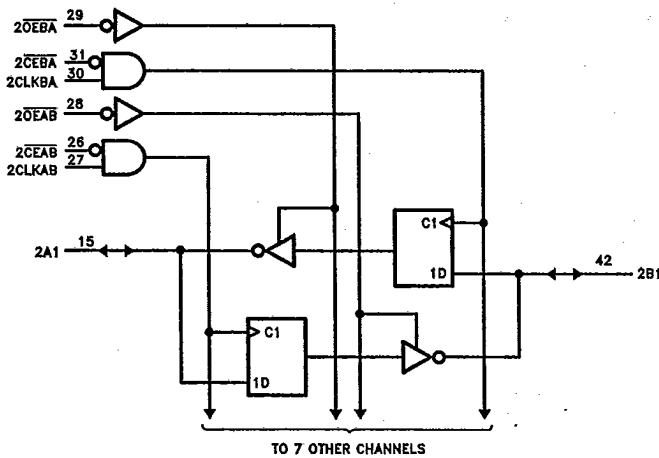
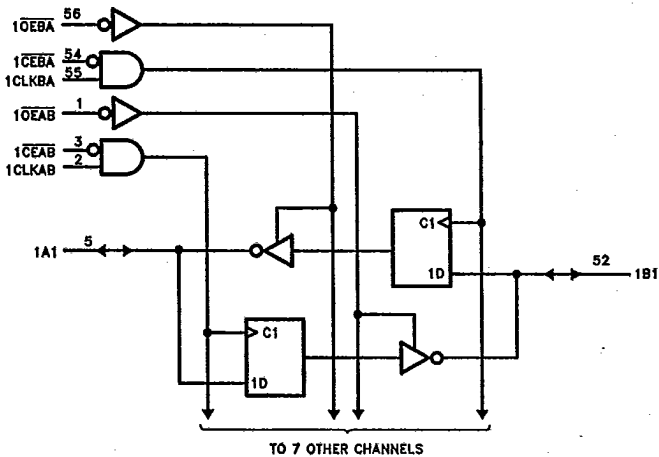
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The 74AC16953 and 74ACT16953 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16953 has CMOS-compatible input thresholds. The 'ACT16953 has TTL-compatible input thresholds.

The 54AC16953 and 54ACT16953 are characterized over the full military temperature range of -55°C to 125°C . The 74AC16953 and 74ACT16953 are characterized for operation from -40°C to 85°C .

logic diagram (positive logic)



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