54AC/74AC353 • 54ACT/74ACT353

Dual 4-Input Multiplexer With 3-State Outputs

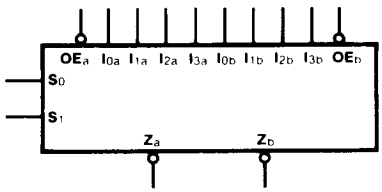
Description

The 'AC/'ACT353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus-oriented systems.

- **Inverted Version of the 'AC/'ACT253**
- **Multifunction Capability**
- **Separate Enables for Each Multiplexer**
- **Outputs Source/Sink 24 mA**
- **'ACT353 has TTL-Compatible Inputs**

Ordering Code: See Section 6

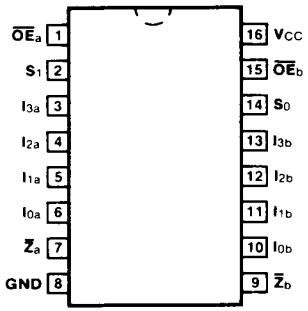
Logic Symbol



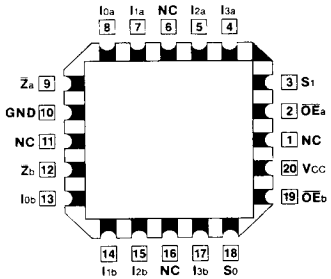
Pin Names

I_{0a} - I_{3a}	Side A Data Inputs
I_{0b} - I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
$\overline{Z}_a$, $\overline{Z}_b$	3-State Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC and PCC

Functional Description

The 'AC/'ACT353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

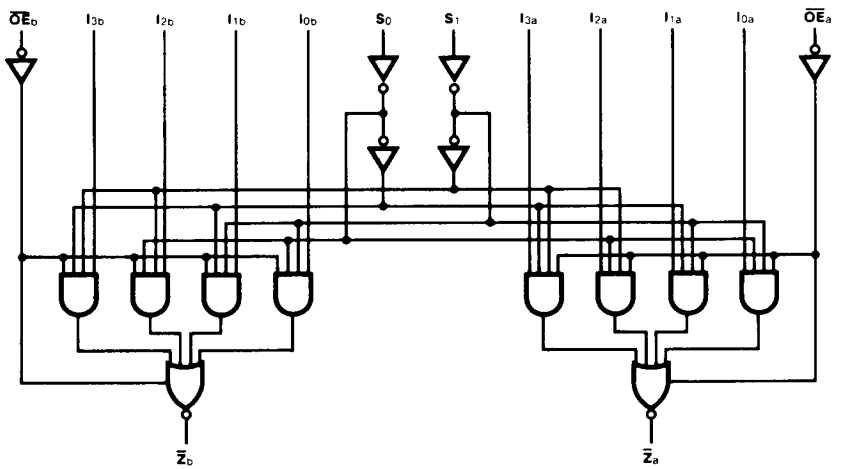
Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Address inputs S_0 and S_1 are common to both sections.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT353)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5						ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		6.5 5.0						ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		6.5 5.0						ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0		5.5 4.0						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.5						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.5						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.5 4.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0						ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0						ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0		5.5						ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0		5.5						ns	3-5
t_{PZH}	Output Enable Time	5.0		4.5						ns	3-7
t_{PZL}	Output Enable Time	5.0		5.0						ns	3-8
t_{PHZ}	Output Disable Time	5.0		6.0						ns	3-7
t_{PLZ}	Output Disable Time	5.0		4.5						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V