Military 54ALS574

Octal D-Type Flip-Flop With 3-State Outputs

ELECTRICALLY TESTED PER: MPG54ALS574

The 54ALS574 is a high-speed, low-power Octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The 54ALS574 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge Triggered Clock
- 3-State Output for Bus Interface
- Eight Latches in a Single Pack
- Hysteresis on Latch Enable
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

AVAILABLE AS:

1) JAN: N/A
2) SMD: 8400101
3) 883C: 54ALS574/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2
***Call Factory for latest update**

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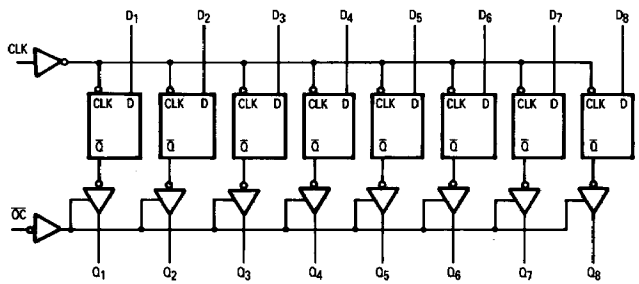
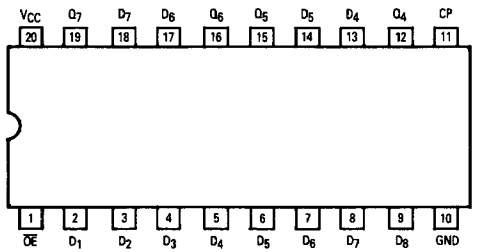
LOGIC DIAGRAM



CONNECTION DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{OE}$	1	1	1	V_{CC}
Q_0	2	2	2	V_{CC}
D_0	3	3	3	V_{CC}
D_1	4	4	4	V_{CC}
Q_1	5	5	5	V_{CC}
Q_2	6	6	6	V_{CC}
D_2	7	7	7	V_{CC}
D_3	8	8	8	V_{CC}
Q_3	9	9	9	V_{CC}
GND	10	10	10	GND
CP	11	11	11	V_{CC}
Q_4	12	12	12	OPEN
D_4	13	13	13	OPEN
D_5	14	14	14	OPEN
Q_5	15	15	15	OPEN
Q_6	16	16	16	OPEN
D_6	17	17	17	OPEN
D_7	18	18	18	OPEN
Q_7	19	19	19	OPEN
V_{CC}	20	20	20	V_{CC}

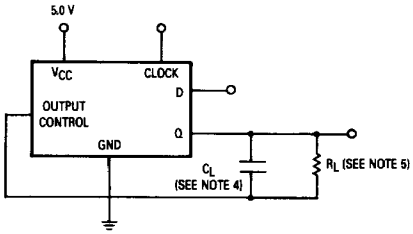
BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

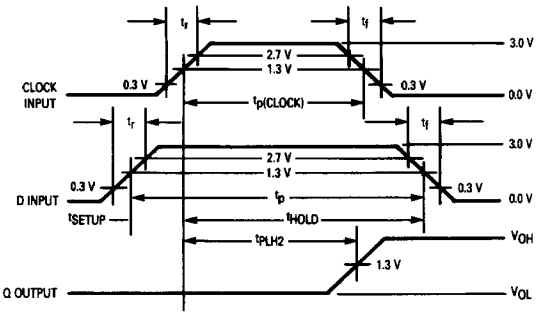
TRUTH TABLE

Inputs		Outputs	
D_n	CP	OE	Q_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

SYNCHRONOUS SWITCHING TEST CIRCUIT (HIGH LEVEL DATA) AND WAVEFORMS





NOTES:
1. Clock input pulse characteristics:
   $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{p(clock)} = 16.5$ ns, and PRR ≤ 1.0 MHz.
2. D input pulse characteristics:
   $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{setup} = 15$ ns, $t_{hold} = 4.0$ ns, $t_p = 19$ ns, and PRR is 50% of the clock PRR.
3. For f_{MAX}, the clock input pulse characteristics are as follows:
   $t_r = t_f = 3.0$ ns, $t_{p(clock)} = 16.5$ ns, PRR = 30 MHz.
4. $C_L = 50$ pF ± 10% (including jig and probe capacitance, without package in test fixture).
5. $R_L = 499\ \Omega \pm 1.0\%$.
6. Voltage measurements are to be made with respect to network ground terminal.

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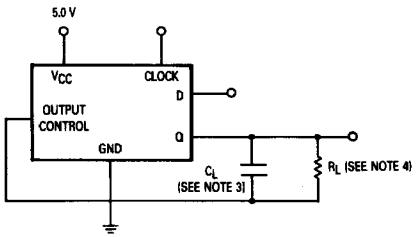
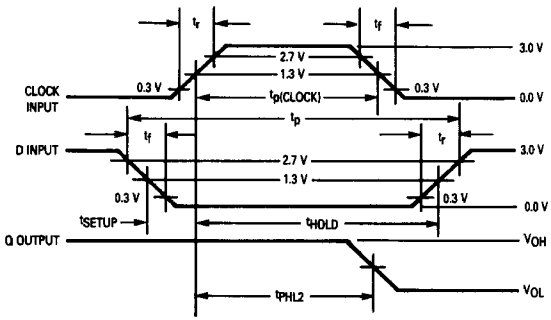
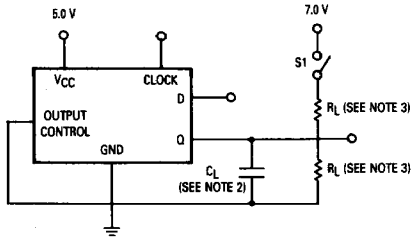
SYNCHRONOUS SWITCHING TEST CIRCUIT (LOW LEVEL DATA) AND WAVEFORMS





NOTES:
1. Clock input pulse characteristics:
   $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{p(clock)} = 16.5$ ns, and PRR ≤ 1.0 MHz.
2. D input pulse characteristics:
   $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{setup} = 15$ ns, $t_{hold} = 4.0$ ns, $t_p = 19$ ns, and PRR is 50% of the clock PRR.
3. $C_L = 50$ pF ± 10% (including jig and probe capacitance, without package in test fixture).
4. $R_L = 499\ \Omega \pm 1.0\%$
5. Voltage measurements are to be made with respect to network ground terminal.

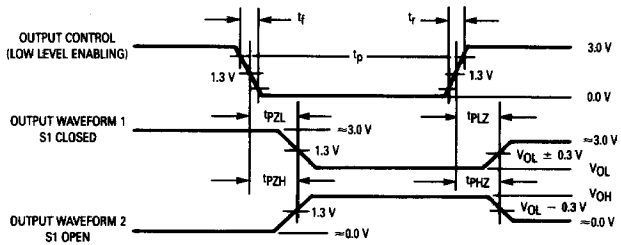
TRI-STATE SWITCHING TEST CIRCUIT AND WAVEFORMS



NOTES:
1. Output control input characteristics:
   $t_r = t_f = 6.0 \pm 1.5$ ns, $t_p = 200$ ns, and PRR ≤ 1.0 MHz.
2. $C_L = 50$ pF ± 10% (including jig and probe capacitance, without package in test fixture).
3. $R_L = 499\ \Omega \pm 1.0\%$
4. Voltage measurements are to be made with respect to network ground terminal.

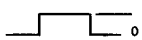
SWITCH POSITIONS

Symbol	S1
t_{PZH}	Open
t_{PZL}	Closed
t_{PLZ}	Closed
t_{PHZ}	Closed



Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, $\overline{OE}$ = 0.8 V, V_{IN} = 2.0 V, CP = (See Note 1), other inputs are open.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IL} = 0.8 V, CP = (See Note 1), other inputs are open.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_{IL}	Logical "0" Input Current	0	−200	0	−200	0	−200	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_O	Output Current	−15	−110	−15	−110	−15	−110	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open, V_{OUT} = 2.25 V, CP = (See Note 1), $\overline{OE}$ = GND.
I_{IOZH}	Output Off Current High		20		20		20	μA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other inputs are open, V_{OUT} = 2.7 V, $\overline{OE}$ = 5.0 V, CP = (See Note 1).
I_{IOZL}	Output Off Current Low		−20		−20		−20	mA	V_{CC} = 5.5 V, V_{IN} = 0.8 V, other inputs are open, V_{OUT} = 0.4 V, $\overline{OE}$ = 5.0 V, CP = (See Note 1).
I_{CCH}	Power Supply Current Off		17		17		17	mA	V_{CC} = 5.5 V, V_{IN} = 5.0 V (all inputs), $\overline{OE}$ = GND, CP = (See Note 1).
I_{CCL}	Power Supply Current Off		23		23		23	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), CP = (See Note 1).
I_{CCZ}	Power Supply Current Off		27		27		27	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), $\overline{OE}$ = 5.0 V, CP = (See Note 1).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTES:

1. Apply  3.0 V, 5.5 V pulse prior to test.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2}	Propagation Delay /Data-Output CLK to Qn	4.0	12	4.0	15	4.0	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output CLk to Qn	4.0	12	4.0	15	4.0	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLZ}	Propagation Delay /Data-Output $\overline{OE}$ to Qn	3.0	13	3.0	15	3.0	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHZ}	Propagation Delay /Data-Output $\overline{OE}$ to Qn	2.0	8.0	2.0	10	2.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PZL}	Propagation Delay /Data-Output $\overline{OE}$ to Qn	4.0	18	4.0	21	4.0	21	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PZH}	Propagation Delay /Data-Output $\overline{OE}$ to Qn	4.0	18	4.0	21	4.0	21	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
f_{MAX}	Maximum Clock Frequency	30		30		30		MHz	V_{CC} = 5.0 V, C_L = 50 pF, (See Note 1).

NOTE:
1. f_{MAX}, limit is the frequency of the input pulse. The output frequency shall be one half the input frequency.