



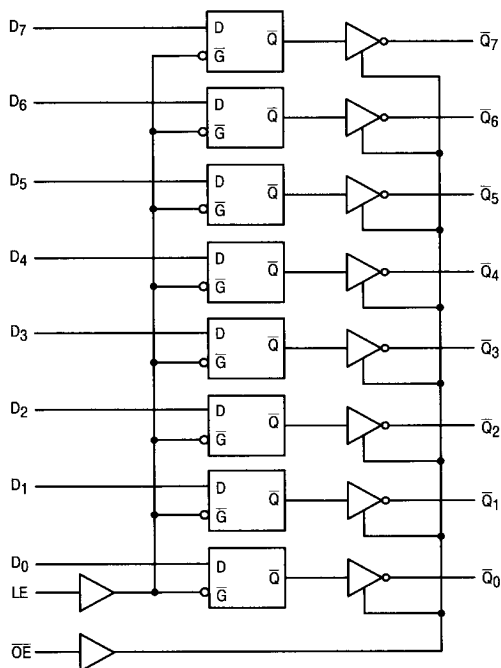
Octal D-Type Transparent Latch With Active Low Enable 3-State Inverted Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/34602

The 54F533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing

LOGIC DIAGRAM



Military 54F533



AVAILABLE AS:

- 1) JAN: JM38510/34602BXA
- 2) SMD: N/A
- 3) 883: 54F533/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

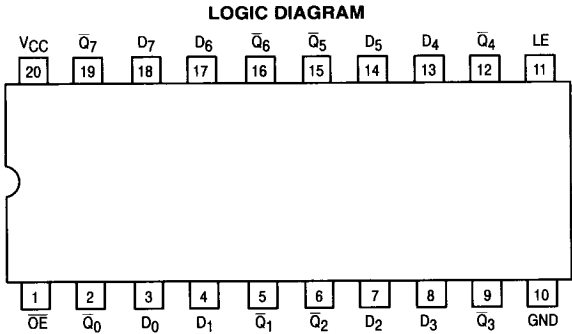
FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$\overline{OE}$	1	1	1	VCC
$\overline{Q_0}$	2	2	2	OPEN
D_0	3	3	3	VCC
D_1	4	4	4	VCC
$\overline{Q_1}$	5	5	5	OPEN
$\overline{Q_2}$	6	6	6	OPEN
D_2	7	7	7	VCC
D_3	8	8	8	VCC
$\overline{Q_3}$	9	9	9	OPEN
GND	10	10	10	GND
LE	11	11	11	VCC
$\overline{Q_4}$	12	12	12	OPEN
D_4	13	13	13	VCC
D_5	14	14	14	VCC
$\overline{Q_5}$	15	15	15	OPEN
$\overline{Q_6}$	16	16	16	OPEN
D_6	17	17	17	VCC
D_7	18	18	18	VCC
$\overline{Q_7}$	19	19	19	OPEN
VCC	20	20	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

54F533

TRUTH TABLE			
Inputs		Outputs	
D _n	LE	Q̄ _n	Q _n
H		L	H
L		L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

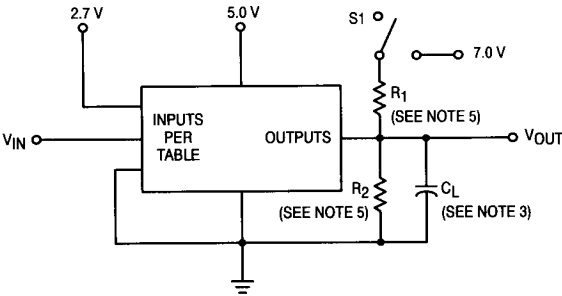


FUNCTIONAL DESCRIPTION

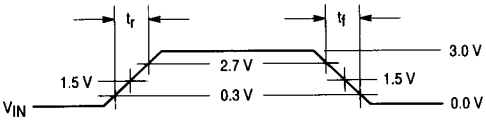
The 54F533 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enter the latches. In this condition the latches are transparent, i. e., a latch output will change state each time its D inputs at setup time preceding the HIGH-to-

LOW transition of LE. The 3-state buffers are controlled by the Output Enable (Q̄E) input. When Q̄E is LOW, the buffers are in the bi-state mode. When Q̄E is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

AC TEST CIRCUIT

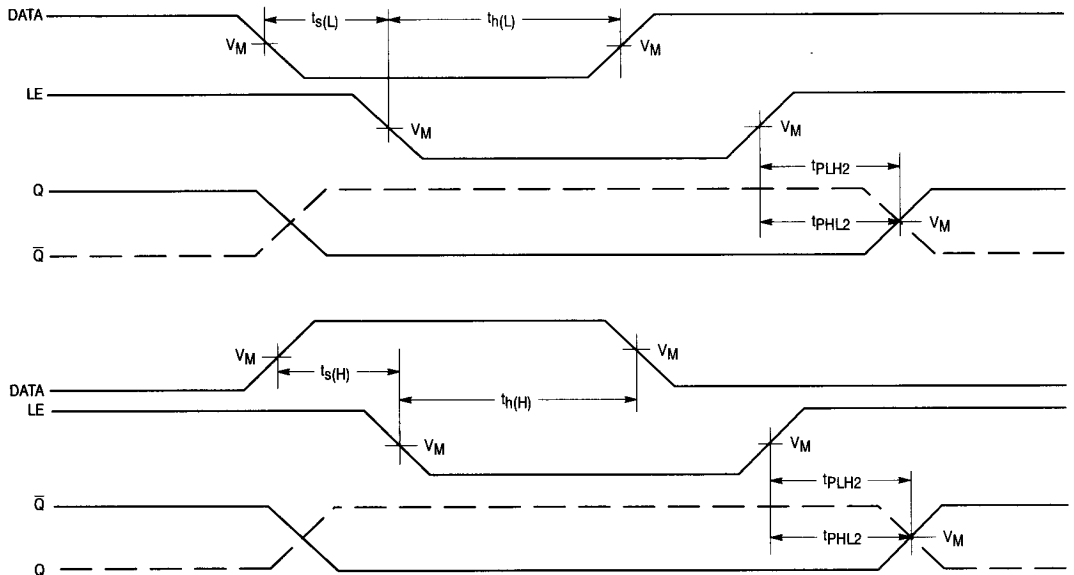
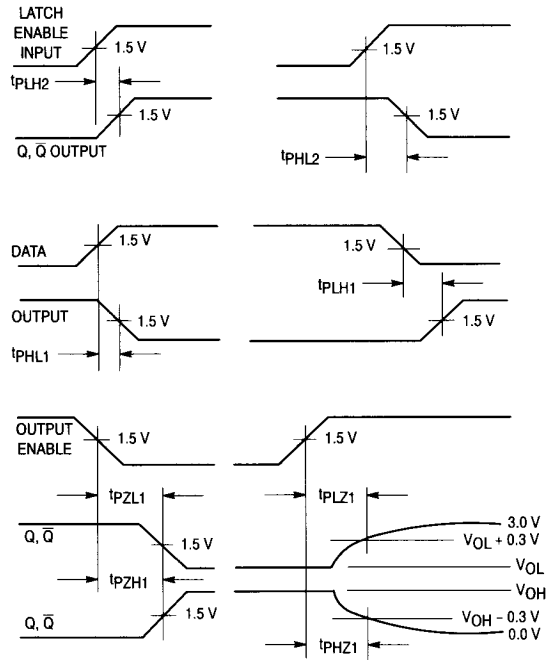


Test Type	S1
t _{PLH}	open
t _{PHL}	open
t _{PHZ}	open
t _{PZH}	open
t _{PLZ}	closed
t _{PZL}	closed



REFERENCE NOTES ON PAGE 4-214

54F533 WAVEFORMS



* $t_{s(H,L)} = 2.0 \text{ ns}$.

* $t_{h(H,L)} = 3.0 \text{ ns}$.

*Setup and Hold times are for information only. No testing required.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical “1” Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = –1.0 mA, V _{IL} = 0.8 V, other inputs are open, OE = 0.8 V, LE = 2.0 V.
V _{OL}	Logical “0” Output Voltage		0.5		0.5		0.5	V	V _{CC} = 4.5 V, I _{OL} = 20 mA, V _{IH} = 2.0 V, other inputs are open, LE = 2.0 V, OE = 0.8 V.
V _{IC}	Input Clamping Voltage		–1.2					V	V _{CC} = 4.5 V, I _{IN} = –18 mA, other inputs are open.
I _{IH}	Logical “1” Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical “1” Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs are open.
I _{OD}	Diode Current	35		35		35		mA	V _{CC} = 4.5 V, V _{IN} = 5.5 V, other inputs are open, LE = 5.5 V, OE = 0 V, V _{OUT} = 2.5 V.
I _{IL}	Logical “0” Input Current	–0.03	–0.6	–0.03	–0.6	–0.03	–0.6	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V, other inputs are open.
I _{OS}	Output Short Circuit Current	–60	–150	–60	–150	–60	–150	mA	V _{CC} = 5.5 V, V _{IN} = 0 V, other inputs are open, V _{OUT} = 0 V, LE = 5.5 V, OE = 0 V.
I _{IOZH}	Output Off Current High		50		50		50	μA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other inputs are open, V _{OUT} = 2.4 V, OE = 2.0 V, LE = 5.5 V.
I _{IOZL}	Output Off Current Low		–50		–50		–50	μA	V _{CC} = 5.5 V, V _{IN} = 0 V, other inputs are open, V _{OUT} = 0.5 V, OE = 2.0 V, LE = 5.5 V.
I _{CCH}	Power Supply Current Off		50		50		50	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs), LE = 5.5 V, OE = 0 V.
I _{CCL}	Power Supply Current Off		70		70		70	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs), LE = 5.5 V, OE = 0 V.
I _{CCZ}	Power Supply Current Off		61		61		61	mA	V _{CC} = 5.5 V, all inputs are open, LE & OE = 5.5 V.
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical “0” Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 4.5 V, (Repeat at) V _{CC} = 5.5 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1}	Propagation Delay /Data-Output D _n to $\overline{Q}_n$	3.0	7.0	3.0	9.0	3.0	9.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLH1}	Propagation Delay /Data-Output D _n to $\overline{Q}_n$	4.0	9.0	4.0	12	4.0	12	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PHL2}	Propagation Delay /Data-Output LE to $\overline{Q}_n$	3.0	7.0	3.0	9.0	3.0	9.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLH2}	Propagation Delay /Data-Output LE to $\overline{Q}_n$	5.0	11	4.0	14	4.0	14	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLZ1}	Output Disable Time, $\overline{OE}$ to $\overline{Q}_n$	2.0	5.5	2.0	7.5	2.0	7.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PHZ1}	Output Disable Time, $\overline{OE}$ to $\overline{Q}_n$	2.0	6.0	2.0	8.5	2.0	8.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PZL1}	Output Enable Time, $\overline{OE}$ to $\overline{Q}_n$	2.0	6.5	2.0	9.0	2.0	9.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PZH1}	Output Enable Time, $\overline{OE}$ to $\overline{Q}_n$	2.0	10	2.0	12.5	2.0	12.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.

NOTES:

1. Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, Z_{OUT} = 50 Ω.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF $\pm 10\%$ including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. R₁ = R₂ = 499 Ω $\pm 5.0\%$.