National Semiconductor

54F/74F545 Octal Bidirectional Transceiver with TRI-STATE® Outputs

General Description

The 'F545 is an 8-bit, TRI-STATE, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24 mA (20 mA Mil) bus drive capability on the A ports and 64 mA (48 mA Mil) bus drive capability on the B ports.

One input, Transmit/Receive ($T/\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a TRI-STATE condition.

Features

- Higher drive than 8304
- 8-bit bidirectional data flow reduces system package count
- TRI-STATE inputs/outputs for interfacing with bus-oriented systems
- 24 mA (20 mA Mil) and 64 mA (48 mA Mil) bus drive capability on A and B ports, respectively
- Transmit/Receive and Output Enable simplify control logic
- Guaranteed 4000V minimum ESD protection
- Pin for Pin compatible with Intel 8286

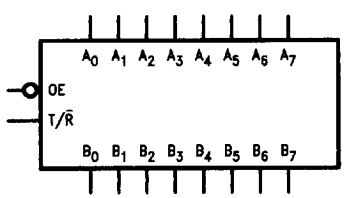
Ordering Code: See Section 11

Commercial	Military	Package Number	Package Description
74F545PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F545DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F545SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F545SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F545FM (Note 2)	W20A	20-Lead Cerpack
	54F545LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

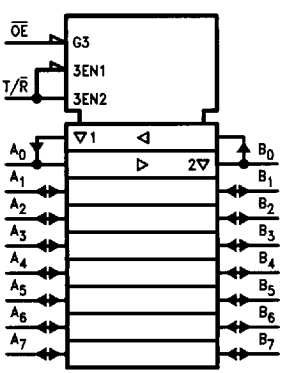
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols



TL/F/9556–3

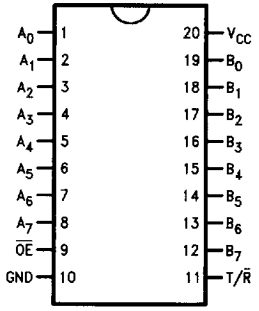
IEEE/IEC



TL/F/9556–5

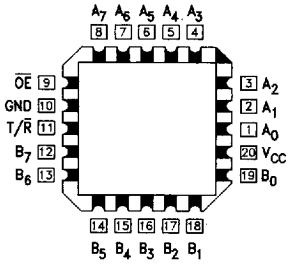
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9556–1

Pin Assignment for LCC



TL/F/9556–2

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20 μA/−1.2 mA
T/$\overline{R}$	Transmit/Receive Input	1.0/2.0	20 μA/−1.2 mA
A_0–A_7	Side A TRI-STATE Inputs or	3.5/1.083	70 μA/−650 μA
	TRI-STATE Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)
B_0–B_7	Side B TRI-STATE Inputs or	3.5/1.083	70 μA/−650 μA
	TRI-STATE Outputs	600/106.6 (80)	−12 mA/64 mA (48 mA)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA ($\overline{OE}$, T/$\overline{R}$)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (A_n)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_n)
		54F 10% V_{CC}	2.0					I_{OH} = −12 mA (B_n)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA (A_n)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_n)
		74F 10% V_{CC}	2.0					I_{OH} = −15 mA (B_n)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA (A_n)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (A_n)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (A_n)
		54F 10% V_{CC}			0.55			I_{OL} = 48 mA (B_n)
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA (A_n)
		74F 10% V_{CC}			0.55			I_{OL} = 64 mA (B_n)
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V ($\overline{OE}$, T/$\overline{R}$)
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V ($\overline{OE}$, T/$\overline{R}$)
		74F			7.0			
I_{BVIT}	Input HIGH Current Breakdown (I/O)	54F			1.0	mA	Max	V_{IN} = 5.5V (A_n, B_n)
		74F			0.5			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−1.2	mA	Max	V_{IN} = 0.5V ($\overline{OE}$, T/$\overline{R}$)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V (A_n)
			−100		−225			V_{OUT} = 0V (B_n)

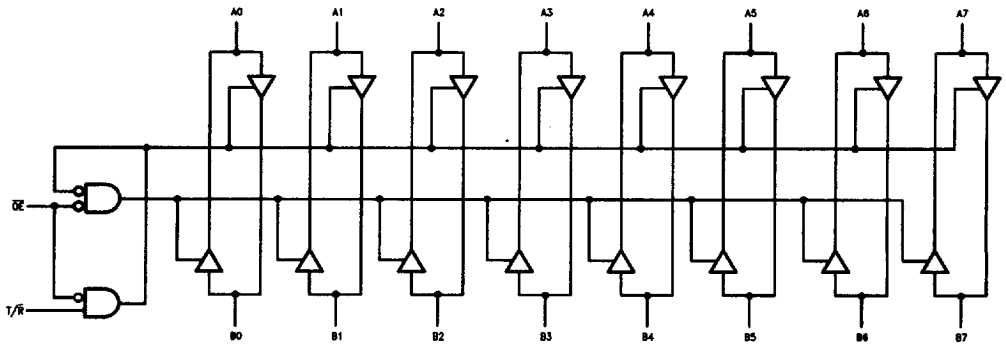
DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{ZZ}	Bus Drainage Test			500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		70	90	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		95	120	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		85	110	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			54F T_A, V_{CC} = Mil, C_L = 50 pF		74F T_A, V_{CC} = Com, C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.5	7.0	ns	2–3
t_{PHL}	A_n to B_n or B_n to A_n	2.5	4.6	6.0	2.0	7.5	2.5	7.0		
t_{PZH}	Output Enable Time	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns	2–5
t_{PZL}		3.5	6.0	8.0	3.0	10.0	3.5	9.0		
t_{PHZ}	Output Disable Time	3.0	5.0	6.5	2.5	9.0	3.0	7.5		
t_{PLZ}		2.0	5.0	6.5	2.0	10.0	2.0	7.5		

Logic Diagram



TL/F/9558–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.